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Implementation of OFDM Transmitter and Receiver System For FPGA

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Abstract
This overall project will focus on Orthogonal Frequency Division Multiplexing (OFDM) research, simulation, and efficient implementation. OFDM is especially suitable for high speed communication due to its resistance to ISI. This paper is mainly focused on the design and implementation of tranmitter & receiver system for FPGA. As communication systems increase their information transfer speed, the time for each transmission necessarily becomes shorter. Since the delay time caused by multipath remains constant, ISI becomes a limitation in high-data-rate communication. OFDM avoids this problem by sending many low speed transmissions simultaneously. The detailed simulation of the OFDM system with 16 QAM will be implemented .The transmitter and receiver will be implemented using FPGA. All Modules are designed using VHDL programming language.

Keywords: Orthogonal Frequency Division Multiplexing (OFDM), Field Programmable Gate Array(FPGA), Hardware Description Language (HDL),Modulator,Demodulator , Fast Fourier Transform (FFT),and Signal to Noise Ratio (SNR).

I. Introduction

In this paper we are designing and implementing OFDM Transmitter & receiver system for FPGA. In this section a more detailed explanation of the basic blocks in the OFDM system will be provided. The theory behind all the blocks will be briefly explained and in particular, focusing in the FFT algorithm.

Then, the configuration of the main blocks of the modulator and demodulator involving the FFT/IFFT blocks will be presented, explaining not only the internal configuration of the blocks but also the input and output that must be achieved.

1.1 OFDM Transmitter

The model considered for the implementation of the OFDM transmitter is theshown in the Fig. 3.1, and basically consist of the following blocks:

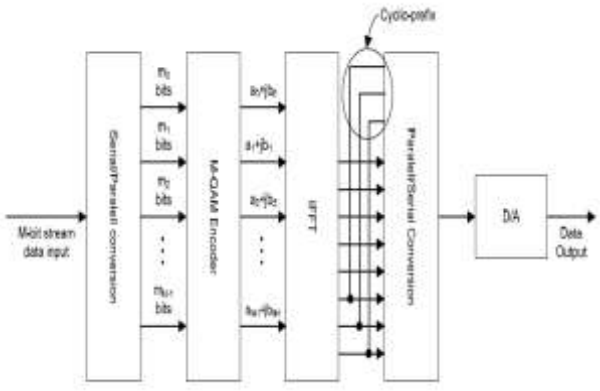


Fig. 1.1OFDM transmitter

The serial to parallel converter receive the M serial bits to be transmitted, andthose bits are divided into N sub-blocks of mn bits each sub-block. Those N sub-blocks will be mapped by the constellation modulator using Graycodification, this way an + jbn values are obtained in the constellation of themodulator.

The M-QAM encoder converts input data into complex valued constellation points, according to a given constellation, 4QAM, 16-QAM, 32-QAM and so on.The amount of data transmitted on each subcarrier depends

on theconstellation; 4QAM and 16QAM transmit two and four data bits per subcarrier,respectively. Which constellation to use depends on the quality of thecommunications channel. In a channel with high interference a small modulationscheme like BPSK is favorable, since the required signal to noise ratio (SNR) inthe receiver is low, whereas in a interference free channel a larger constellationis more beneficial due to the higher bit rate.

It is necessary to specify how the constellation will be mapped to implement thatblock. However, independently of the format of the constellation, the blockencoder can be made by consulting a conversion table, implemented with aLUT that exists in LCs of FPGAs.It is important to notice that in that mapping block, bits areconverted intocomplex symbols (phasors) having the information of the constellation in itsI, Qcomponents.The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain; an IFFT converts a number of complex data points, of length that is power of 2, into the same number of points but in the time domain. The number of subcarriers determines how many sub-bandsthe available spectrum is split into.

1.2 OFDM Receiver

The blocks of the OFDM Receiver are shown in the Fig. 4.1,and those blocksare:

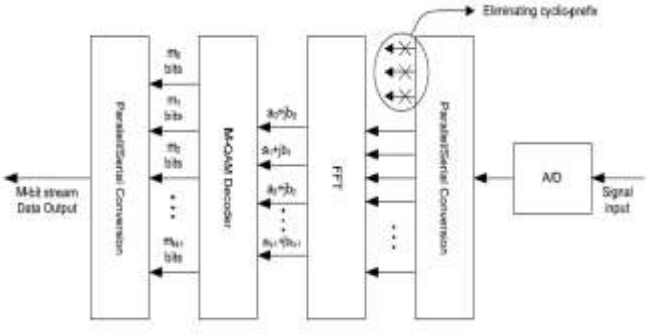


Fig. 1.2 OFDM receiver

The demodulation can be made by DFT, or better, by FFT, that is it efficient implementation that can be used reducing the time of processing and the usedhardware. FFT calculates DFT with a great reduction in the amount ofoperations, leaving several existent redundancies in the direct calculation ofDFT.At the decoder, a mapped symbol (point) of the transmitted constellation mayhave changed due to the additive noise in the communications channel, amis-adjustment in the sampling time at the receiver, or several other unwantedcauses.

Therefore, it is necessary to define a threshold to facilitate the decision makingin the receiver constellation. That is the function of the M-QAM decoder.

II. Random bit generator

The first block of the OFDM system is the random bit generator, this block generates the serial binary data that will arrive to the serial to parallel converter, in other words, this block generates the data with which all the system will work.

2.1 S/P & P/S converters

The aim of the serial to parallel converter is to receive the data that is going to be transmitted. The serial to parallel converter receive the M serial bits to be transmitted, and those bits will be divided into N sub-blocks of m_n bits each sub-block called symbols. The amount of bit of each channel can be different Those N sub-blocks will be mapped by the constellation modulator using Gray codification, this way $a_n + jb_n$ values are obtained in the constellation of the modulator.

The serial to parallel converter at the receiver has the function to receive the data that is going to be demodulated, with the same structure as it was at the transmitter.

To store the M bits a buffer that will contain all the input data into different memory positions is needed. To obtain the M data bits at the output we'll need the buffer to stop reading data, another option is that the amount of data stored at the buffer is 2M, this way is not necessary to stop the reading, this way can read continuously.

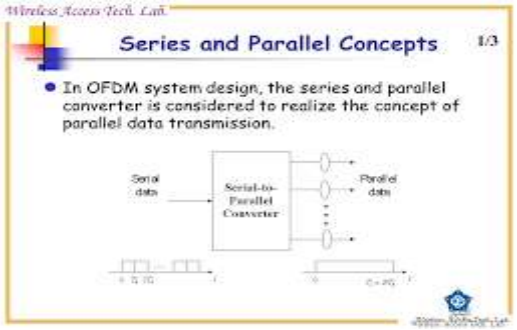


Fig. 2.1 S/P and P/S converters

The parallel to serial converter is only the opposite function of the serial to parallel converter, and it is placed just before sending the data through the channel by the digital to analog converter, at the transmitter, and just the last block before obtaining the final data at the receiver.

III. Constellation mapper (encoder)

The encoder of the constellation maps the M bits of the channel in a point a + jb in the constellation of the modulator. The decoding block receives that IQ symbol and demaps it obtaining the original m transmitted bits.

3.1 Constellation encoder

It is important to notice that in that mapping we only perform a conversion of bits for the phasor that acts. However, nor modulation is performed, asin the case of QAM, because that as shown, it is done by IFFT.

It is necessary to specify how the constellation will be to be mapped, to implement this block. However, independently of the format of the constellation, the block encoder can be made through a consultation at a conversion table, implemented by LUT that exists in LCs of FPGAs.

As we have explained previously, a constellation mapper takes a serial bit stream as its input and segments the stream into N-bit symbols, which are mapped to coordinates in the signal constellation. The coordinates of each point in a two-dimensional signal constellation represents the baseband in-phase and quadrature (I-Q) components that modulate the orthogonal IF carrier signals. Because the constellation mapper defines the shape and dimension of the signal constellation, it defines the modulation scheme that is implemented. Attempt that the entrance of the encoder a binary number of m bits, and that the exit generates two binary numbers, one in phase, the, and other in quadrature, b, whose size is defined by IFFT.

The modulations taken into account for this project are BPSK, 4-QAM, 16-QAM,

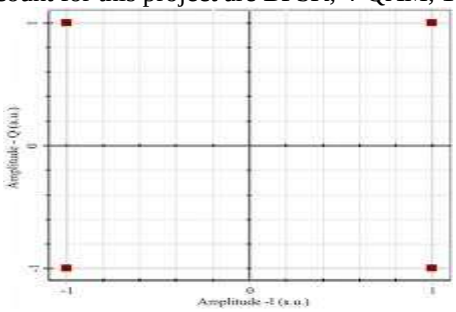


Fig. 3.1 QAM constellation

In Fig 3.1 is shown the constellation of a 16-QAM modulation. In this project the implementation of the constellation has been done, as commented previously, using LUT's, tables with the hardcoded values of the output modulation depending on the values of the N input bits, these tables has been written into VHDL code.

3.2 Constellation decoder

In the receiver, the point of the constellation transmitted it can have changed due to the noises of the transmission channel, mistake in the time of sampling of the receiver and several other causes. Therefore it is necessary to define a threshold so that it can be made the decision on which point in the constellation the received sign is acting. That is the function of the decoder. The demodulated I-Q coordinates may no longer correspond to the exact location of a signal point in the original constellation.

IV. (I)FFT

The OFDM modulation can be obtained through an IDFT. The fast implementation of IDFT, IFFT, can be used reducing the time of processing and the used hardware. The demodulation, in the same way, can be made by DFT, or better, by FFT, that is it efficient implementation.FFT calculates DFT with a great reduction in the amount of operations, leaving several existent redundancies in the direct calculation of DFT. The only limitation of this algorithm is that is only valid for sequences of length 2^N otherwise modified algorithms with less efficiency are needed.

The FFT algorithms can be classified depending on the domains in which are calculated, that can be made in both time domain and frequency domain, we have discussed ahead. If the length of the sequence is a 2^N value, the algorithm applied is called Radix-2. Other more efficient algorithms also exist, for instance the Radix-4, which can be applied when the input sequence length is a 4^N value.

4.1 The FFT algorithm

As we previously said, it is possible to divide the input of FFT successively generating small sequence in the domain of the time that action is named time decimation, TD. It is also possible to separate the sequence at the exit of FFT successively, instead of dividing the entrance. That implementation is called frequency decimation, FD. There is no difference at all between both decimations, so the decision to take one or another depends only on the programmer. The decimation can be used so much for FFT as for IFFT.

The next part shows the previous decomposition of the input time samples of the DFT into odds and evens samples (N/2 samples for each one), for the case of N=8. Thanks to this decomposition the input samples remain tidy since the first sample to the last sample at the frequency response.As previously said, the N/2 DFT's can be decimated into N/4 DFT's and so on, this way is possible to repeat the process until reaching the possible maximum level of division. In that point the basic block decimation is generated so it will be used in the whole FFT (called butterfly). An example of the butterfly of the FFT radix-2 TD and FD is in the following illustration.

In the same way that the decimation in the time generates a butterfly, the decimation in the frequency generates a corresponding butterfly. However the alteration in the flow of data will have to be done in the exit, and no more at the input.

4.2 Implementation scheme (System Generator)

We used the synthesized FFT block in Altera Quartus-II. During this section the configuration of the FFT block for the modulation and demodulation of the OFDM system will be explained.

The FFT is a computationally efficient algorithm for computing a Discrete Fourier Transform (DFT) of sample sizes that are a positive integer power of 2. Fig. 3.15 shows the block interface used for the modulation and demodulation of the OFDM signal.

4.3 Modulator/Demodulator

This section will show the implementation of the OFDM modulation and demodulation schemes done with System Generator simulation tool. Two schemes have been taken into account:

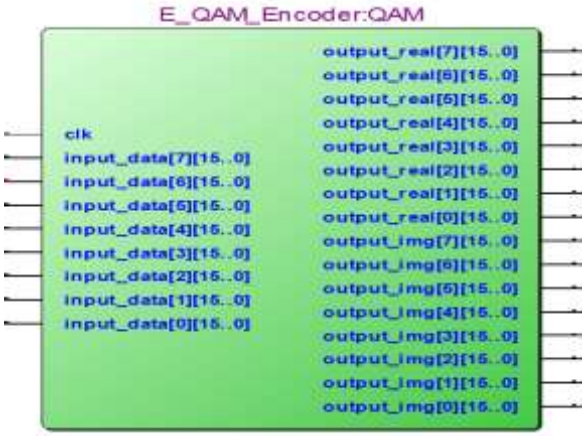
- Modulation and demodulation of a 4-QAM input signal.
- Modulation and demodulation for different input signals.

The difference between both schemes is that in the scheme which has different input signals an M-QAM signal generator has been included. The insertion of the M-QAM signal generator means that a more complex QAM demapper must be placed at the output of the FFT block. Basically the modulation and demodulation schemes of the OFDM system, as previously commented, consist of the concatenation of the IFFT and FFT blocks (the same block with different configurations), but this of course is not as easy as it sounds. Next sections will show how the implementation of these schemes has been done.

V. 16-QAM mod/demod

The 16-QAM scheme for the modulation and demodulation of the OFDM signal has been implemented in this project.

First of all the input in the form of binary data is given to the transmitter, this input is mapped into a 16-QAM constellation symbols. The output of the mapper can be converted to a certain number of bits if needed because depending on the number of bits at the input of the IFFT block the Output will also have different output sizes. Fig 3.17 shows the blocks for the random signal generator, 16-QAM mapper, and the adaptation of the output to be a correct input for the block IFF:



This way the IQ components that will go directly to the IFFT block for the modulation, are obtained.

The output of the IFFT block must be converted to a lower number of bits because the input of FFT block to which will be connected this output has a maximum bit size which otherwise will be exceeded.Previously to the bit conversion, the output signal from the IFFT must be decimated; otherwise the FFT block will overflow.

VI. Result & Discussion

The expected results for each component in an OFDM uplink/downlink system will be shown using VHDL simulator and implemented using FPGA.Serial to parallel converter is used to convert the data from the serial form to the parallel form to introduce it to IFFT and programmed using VHDL language. In the receiver the inverse blocks for those of the transmitter will be obtained.

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