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Multicarrier modulation for new Diode Clamped Multilevel Inverter

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ABSTRACT:
The conventional diode clamped MLI suffers from a practical problem such as dc link unbalancing, indirect clamping of inner devices, series association of the clamping diodes. This paper presents a solution by using new diode clamped multilevel inverter. For both conventional and new DCMLI, Common Mode Voltage (CMV) & THD comparison is presented using different multicarrier based Sinusoidal pulse width modulation techniques, respective output are shown in this literature.

Keywords*:* Common Mode Voltage, Sinusoidal pulse width modulation, Diode Clamped Multilevel Inverter, multicarrier modulation, THD,

I. INTRODUCTION

Multilevel inverters have become necessarily required in high power conversion technology in today's power grid, transportation system and industrial motor drives. Multilevel inverters invented with the specific aim of overcoming the voltage limit capability of power devices. These inverters offer advantages compared to two level inverter; its features include good power quality, low switching losses, high voltage capability and low dv/dt. With the availability of high power rating semiconductor switches, multilevel inverter is attractive for high power applications. Multilevel inverter includes an array of power devices and dc capacitor voltages. It generates output voltage in stepped waveform with low distortion and lower dv/dt. It can operate with low switching frequency. It involves high number of switching states which decreases harmonics at low frequency, thereby reduces switching losses further dv/dt rating is lowered due to reduced leakage current. In multilevel inverter, CMV is reduced; voltage stress in motor bearing is reduced. It avoids bearing failure due to CMV stress. Three most popular topologies in multilevel inverter are diode clamped MLI, capacitor clamped (flying capacitor) MLI and cascaded multicell with separate dc sources. An m-level diode clamped multilevel inverter consists of (m-1) capacitors on dc bus, voltage across each capacitor becomes $V_{dc}/(m-1)$ and generates m-level synthesized staircase output of phase voltage. With increase in number of levels, harmonic content reduces and filters are avoided. But with increasing number of levels, excess clamping diodes are required. In capacitor clamped DCMLI, (m-1)(m-2)/2 clamping capacitors are needed in addition to (m-1) main dc bus capacitors to produce m-level output. Greater number of storage capacitors arise problems of packaging and bulky weight. The second topology flying capacitor multilevel inverter is similar to the structure of Diode clamped multilevel inverter. The capacitor clamped inverter has series connection of capacitor clamped switching cell.

An m-level of flying capacitor multilevel inverter will require (m-1)(m-2)/2 clamping capacitor per phase leg in addition to (m-1) main dc bus capacitor. The connection of capacitor of FCMI assure that voltage stress across each main switch is same and equal to Vdc/(m-1) for m level inverter. The main drawback of FCMI is that it involves most number of capacitor comparative to other multilevel inverter topology. The main drawback of FCMI is that it involves most number of capacitor comparative to other multilevel inverter topology. Another multilevel topology is cascaded multicell inverter. Number of series cell connected gives output voltage which is the sum of voltage generated by each cell. If m-cells are connected in series gives output voltage level (2m+1). Multicell cascaded inverter has simplest structure require less number of component comparative to other type of multilevel topologies.Modulation methods used in MLI can be classified according to switching frequency. Several modulation and control strategies have been developed, includes sinusoidal

pulse width modulation (SPWM), multilevel selective harmonic elimination, and space vector modulation (SVM). A very popular method in industrial applications is the carrier based SPWM that uses phase shifting technique to reduce the harmonics in the output voltage. SVM technique work with low switching frequency and perform one or two commutation of power devices during one cycle of output voltage generating a staircase waveform. In this paper, a multicarrier based modulation for DCMLI is presented. A comparison of 5-Level conventional DCMLI & 5-Level New DCMLI is given. MATLAB simulation is done on five level DCMLI. Results give common mode voltage analysis for different carrier based modulation techniques (Phase Disposition, Phase Opposition Disposition & Alternative Phase Opposition Disposition).

II. DIODE CLAMPED MULTILEVEL INVERTER

The most commonly used topology is the diode clamped multilevel inverter. It gives the stepped output voltage with the use of clamping diode. Voltage stress across power devices decreases with the use of diodes. An m-level DCMLI requires (m-1) voltage source dc bus capacitors, 2(m-1) switching device, (m-1)(m-2) clamping diodes. DCMLI output voltage is in the form of staircase waveform with increase in levels and came closer to the sinusoidal waveform. Magnitude of the harmonic is lowered and at low switching frequency THD is less, low switching losses, low dv/dt rating, reduced CMV and DCMLI[1].In Conventional 5-Level Inverter, DC-bus consists of 4 capacitor, for bus voltage across each dc bus capacitor is $V_{dc}/4$ & each device voltage stress is limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes as shown in fig 1 (a). The numbering sequence of the switches for phase a is Sa_1, Sa_2, Sa_3, Sa_4, Sa_5, Sa_6, Sa_7, Sa_8. Table 1 gives the switching table for 5-level DCMLI. State of switch 1 is means switch is ON and State of switch 0 means switch is OFF.

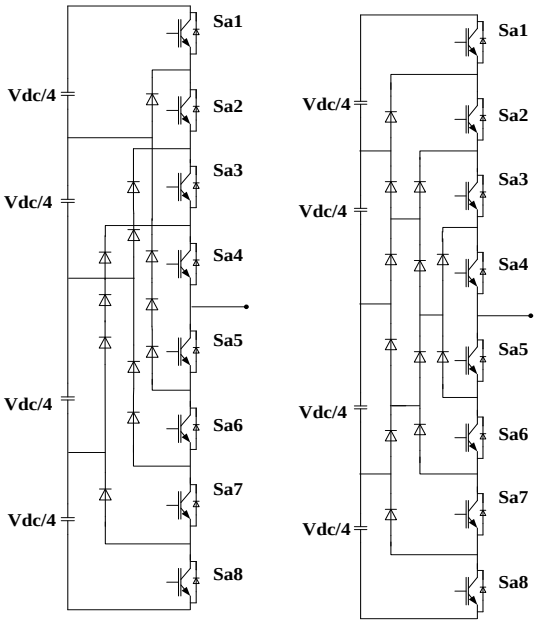
a. For V_{AN} = 0 switches Sa_3, Sa_4, Sa_5, Sa_6 are kept ON and other switches are kept OFF.[8]

b. For V_{AN} = Vdc/4 Switches Sa_2, Sa_3, Sa_4, Sa_5 are kept ON and other switches are kept OFF.

c. For V_{AN} = Vdc/2 Switches Sa_1, Sa_2, Sa_3, Sa_4 are kept ON and other switches are kept OFF.

d. For V_{AN} = -Vdc/4 Switches Sa_5, Sa_6, Sa_7, Sa_8 are kept ON and other switches are kept OFF.

e. For V_{AN} = -Vdc/2 Switches Sa_4, Sa_5, Sa_6, Sa_7 are kept ON and other switches are kept OFF.



5-Level Conventional DCMLI **5-Level New DCMLI**

5 – Level DCMLI switching table								
S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	V_{AN}
1	1	1	1	0	0	0	0	Vdc/2
0	1	1	1	1	0	0	0	Vdc/4
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	--Vdc/2
0	0	0	0	1	1	1	1	-Vdc/4

Table No.1 Switching state of 5-Level DCMLI

New Diode Clamped Multilevel Inverter:-

STRUCTURE:-The proposed Diode Clamped Multi Level inverter is shown in fig. 1 (b), for 5-Level total twelve diode and eight switches are shown with equal voltage rating as conventional DCMLI. Structure of New DCMLI extensible to any level. An m-Level of inverter requires (m-1) voltage source, (m-1) (m-2) diode, 2(m-1) power switches are required[2].

OPERATION:-Following Switching rule are governed for 5-Level new Diode Clamped Multi Level Inverter [8].

a. For any movement, there must be (N-1) neighbouring switching are kept ON.

b. For each two neighbouring switches, the outer switch can only be turn on when inner switch is ON.

c. For each two neighbouring switches, the inner switch can only be turn off when outer switch is OFF.

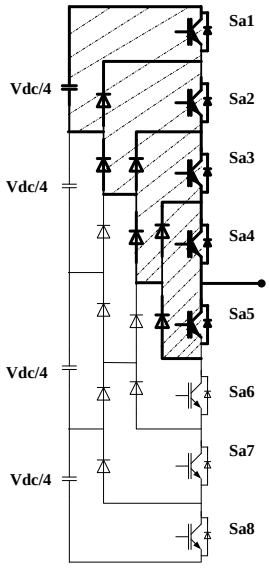


Fig. 3(a) Switching Cell

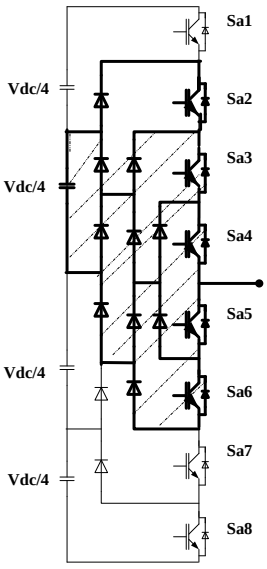


Fig. 3(b) Switching Cell

In New DCMLI for operation purposes an 5-level inverter can be decomposed into (5-1) switching cell as shown in fig. 3(a), 3(b), 3(c), and 3(d). In switching cell (a), switch S_{a2}, S_{a3}, S_{a4} are always kept ON while switch S_{a1} and S_{a5} work alternately connecting inverter output Vdc/2 to Vdc/4. Similarly in cell (b) switch S_{a3}, S_{a4}, S_{a5} are kept ON while S_{a2} and S_{a6} are work alternately and connect inverter output Vdc/2 to 0. In cell (c) S_{a3} and S_{a7} work alternately and S_{a4}, S_{a5}, S_{a6} are kept ON, connect output 0 to -Vdc/2. Similarly in cell (d) Sa4 and Sa8 work alternately and switch S_{a5}, S_{a6} and S_{a7} are kept ON, connect output -Vdc/2 to -Vdc/4.Advantage of New Diode clamped multilevel inverter [8]:- a. The diode series problem of Conventional diode clamped multilevel inverter is solved in new diode clamped multilevel inverter.

b. In New diode clamped multilevel inverter not only power switches are clamped but also diodes are also clamped themselves.

c. The requirement for large RC network for series connection of diode in conventional inverter is solved in new DCMLI.

d. The adding an auxiliary clamping network unequal voltage distribution problem resulted from indirect clamping is expected to be mitigated.

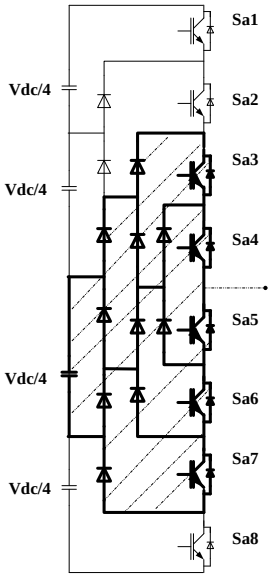


Fig.3(c) Switching Cell

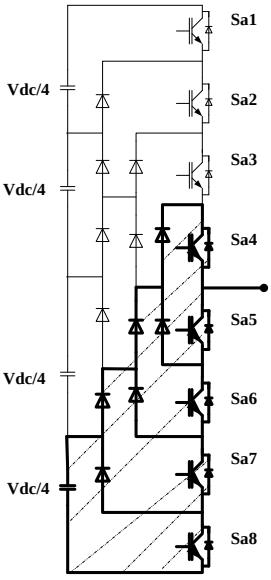


Fig.3(d) Switching Cell

1. Phase Disposition SPWM strategy (PD SPWM).

IV. CARRIER BASED MOLULATION TECHNIQUES

In multicarrier SPWM strategies, several triangular carrier signals are compared with one sinusoidal modulating signal. To get m-level multilevel inverter output, (m-1) triangular carrier signals are compared with modulating sine wave. All the carrier signals are of same A_c and same f_c and reference sine wave has A_m and frequency f_m. Each carrier signal is compared with reference sine wave, pulse is generated when reference signal is greater than the carrier signal.In this modulation strategy, (m-1) carriers are compared with modulating sine wave of frequency f_m to generate m-level output. All the (m-1) carrier signals are of same frequency f_c and same amplitude A_c and all are in same phase. Fig 2 (a) shows APOD modulation strategy generated SPWM pulses. The SPWM pulses is generated in MATLAB simulation.

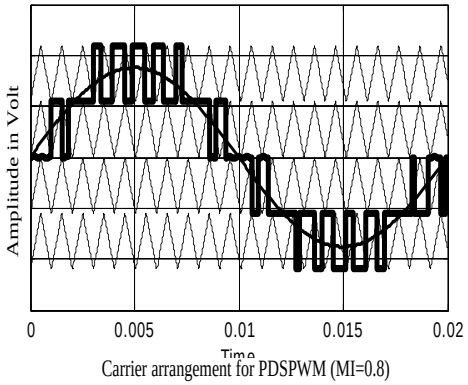


Fig. 2(a) PD SPWM

2. Phase Opposition Disposition PWM strategy (POD SPWM).

In this SPWM POD strategy, the carrier waveforms above the zero reference are in same phase and carrier signals below are also in phase, but are 180 degrees phase shifted from those above zero. Fig shows (m-1) carrier signals to generate m-level multilevel output. Fig 2 (b) shows MATLAB simulated POD SPWM pulses.

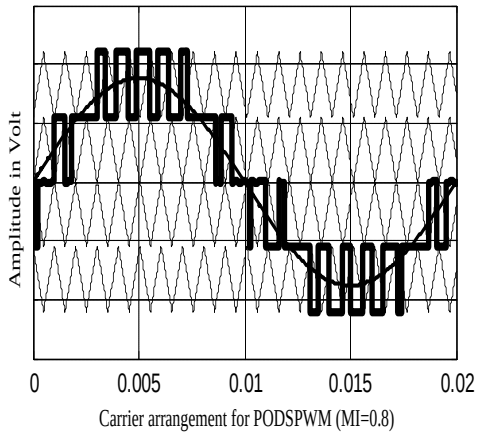


Fig. 2(b) POD SPWM

3. Alternate Phase Opposition Disposition PWM strategy (APOD SPWM)

In APOD strategy the carriers of same amplitude are phase displaced from each other by 180 degrees from its adjacent carriers. The carrier arrangement is shown in Fig. 2(c). For m-level output, (m-1) carrier signals are phase displaced by 180 degrees to its adjacent carrier signal.

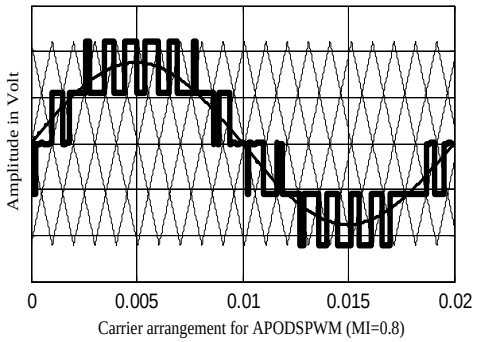


Fig.2(c) APOD SPWM

IV. SIMULATION RESULT AND CMV COMPARISON:

MATLAb simulation of 5-level conventional and new DCMLI is presented. The input DC voltage is 440 V. Fig. 3 (a) shows output leg voltages of conventional DCMLI along with CMV.

Fig. 3 (b) shows output leg voltages of new DCMLI along with CMV. The simulation output gives a conclusion that by employing POD-SPWM technique we can reduce the CMV or eliminate the CMV. The CMV comparison of 5-Level conventional DCMLI and New 5-Level DCMIL is shown in table no.2.

DCMLI	PD		POD		APOD	
	CMV	THD	CMV	THD	CMV	THD
5-L DCMLI	**39.98 V**	**13.91%**	**18.97 V**	**26.67%**	**30.56 V**	**22.44%**
5-L NEW DCMLI	**39.54 V**	**15.69%**	**18.98 V**	**26.38%**	**30.86 V**	**27.51%**

Table No. 2 Comparison of CMV & THD in

Conventional 5-Level DCMLI and New 5-Level DCMLI

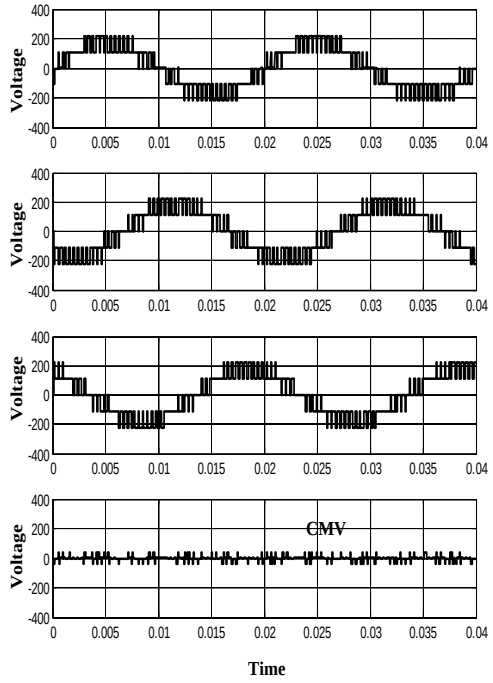


Fig. 3(a) 3 phase output Voltage and CMV of 5-Level Conventional DCMLI (Phase Opposition Disposition)

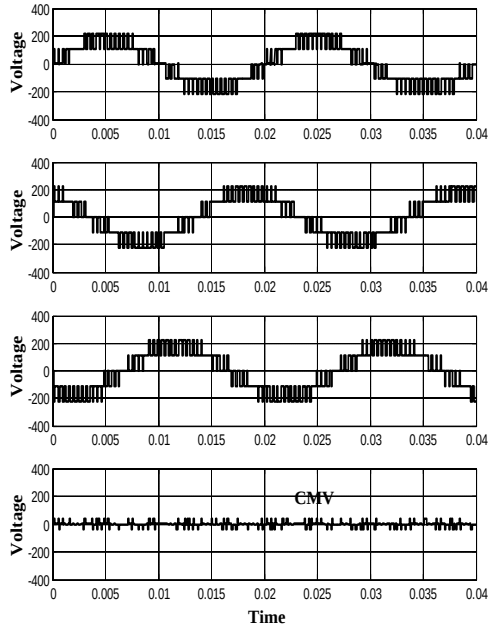


Fig. 3(b) 3 phase output voltage 7 CMV of 5-Level New DCMLI (Phase Opposition Disposition)

V. CONCLUSION:-

This paper presented a comparison of Common Mode Voltage & THD in conventional 5-level DCMIL and New 5-level DCMLI. MATLAB simulation results show that in Phase Opposition Disposition SPWM technique, CMV found to be much less than as compared to other SPWM technique (PD/APOD).

REFERENCES:

[1] Mohan M Renge, Hiralal M Suryawanshi, "Five-Level Diode Clamped Inverter to Eliminate Common Mode Voltage and Reduce dv/dt in Medium Voltage Rating Induction Motor Drives", IEEE trans. on Power Electronics, vol. 23, no. 4, pp 1598-1606, July 2008.

[2] Mohan M Renge, Hiralal M Suryawanshi, "Three-Dimensional Space-Vector Modulation to Reduce Common-Mode Voltage for Multilevel Inverter", IEEE Trans on Ind. Electronics, vol. 57, no. 7, pp 2324-2331, July 2010.

[3] M. M. Renge and H. M. Suryawanshi, "Multilevel inverter to eliminate common mode voltage in induction motor drives," in Proc. IEEE Conf. Ind. Technol. (ICIT'06), Dec. 2006, pp. 2354–2358.

[4] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[5] Jose Rodriguez, Steffen Bernet, Peter K. Steimer, and Ignacio E. Lizama, "A Survey on Neutral-Point-Clamped Inverters", IEEE Trans on Ind. Electronics, vol. 57, no. 7, pp 2219-2230, July 2010.

[6] Haoran Zhang, Member, IEEE, Annette von Jouanne, Senior Member, IEEE, and Shaoan Dai, Student Member, IEEE, "A Reduced-Switch Dual-Bridge Inverter Topology for the Mitigation of Bearing Currents, EMI, and DC-Link Voltage Variations", IEEE Transactions On Industry Applications, Vol. 37, No. 5, September/October 2001.

[7] M. M. Renge, and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," IEEE Trans Power Electron., Vol. 23, No. 4, pp. 1598-1607, Jul. 2008.

[8] X. Yuan and I. Barbi, "A New Diode Clamping Multilevel Inverter," IEEE Trans. Power Electron., vol. 15,no. 4, pp. 711-718, Jul. 2000.

[9] McGrath, B.P.; Holmes, D.G.; "Multicarrier PWM strategies for multilevel inverters," Industrial Electronics, IEEE Transactions on, vol.49, no.4, pp. 858- 867, Aug 2002 doi: 10.1109/TIE.2002.801073

[10] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[11] X. Yuan and I. Barbi, "ARCPI resonant snubber for the neutral-pointclamped inverter," *IEEE Trans. Ind. Applicat.*, vol. 36, pp. 585–595, Mar./Apr. 2000.

[12] Yoshihiro Murai, Takehiko Kubota, and Yoshiriro Kawase, "Leakage current reduction for a high-frequency carrier inverter feeding an induction motor," IEEE Trans. Ind. Appl., Vol. 28. No. 4, pp. 858-863, Jul./Aug. 1992.

[13] Chenggang Mei, Juan Carlos Balda, and William P. Waite, "Cancellation of common-mode voltages for induction motor drives using active method," IEEE Trans. Energy Conversion, Vol. 21, No. 2, pp. 380-386, Jun. 2006.