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An Innovative Design solution for minimizing Power Dissipation in SRAM Cell

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ABSTRACT
Over the years, the development of the logic on the chip is increased. To sustain and drive the logic flow, various techniques and SRAM cell designs have been implemented. The basic element of memory design is 6T SRAM cell. But while dealing with this 6T SRAM cell there are some issues with the parametric analysis on the performance of the cell. This paper presents an innovative design idea of new 8T RAM cell with various parametric analysis. The proposed cell is compared with the standard cell in terms of different parameters such as area, speed and power consumption along with the loading effect with the increase in load capacitance on the cell. The structure is designed with CMOS 45 nm Technology with BSIM 4 MOS modelling using Microwind 3.5 software tool.
Keywords - 8T SRAM, Parametric analysis, BSIM4, read/write operation

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I. INTRODUCTION

In modern VLSI design, the most important consideration is the power consumption of the design. The power consumption gets increased due to the high integration and the speed of processor. Designer are more concerned about the power issues in the design rather than the speed and area of the design. Different design implementation present different power optimization opportunities [1].

In modern microprocessors, cell accesses contribute ~30-60% of the total dissipated power. A significant fraction of the cell energy is dissipated in driving the bit-lines, which are heavily loaded with multiple storage cells. This led circuit designers to put more emphasis on the reduction of power dissipation in memory cells [2].

This proposed work provides a new approach towards the memory design and its modelling. In this paper, we propose an improved design on an SRAM cell, which contains two extra tail transistors in the pull down paths of the respective inverters to avoid charging of the bit lines.

In conventional SRAM cell design, the selection lines WL concern all the cells of one row. The bit lines BL and ~BL concern all the cells of one column. Because of this structure, in the Nano scale technologies, the structure becomes quite leaky and the speed and power of the design increases. On the top of it, the loading effect also increases [2]. This can be overcome by using the new approach of design over the conventional 6T RAM cell by adding two more transistor which will provide the faster discharge leading to low power and high speed of operation.

II. DESIGN METHODOLOGY

A. Conventional 6T RAM

The basic conventional SRAM cell consists of 6 transistors. It uses six transistors as shown in figure 1 to store and access one bit. Out of these 6 transistors, four transistors in the center form two cross-coupled inverters. Because of the feedback structure, a low logic value on the first inverter will generate a high logic value on the second inverter, which stores the low value on the second inverter. Similarly, a high logic input value on the first inverter will generate a low logic input value on the second inverter, which feeds back the low input value onto the first inverter. Therefore, the two inverters will store their current logical value [2].

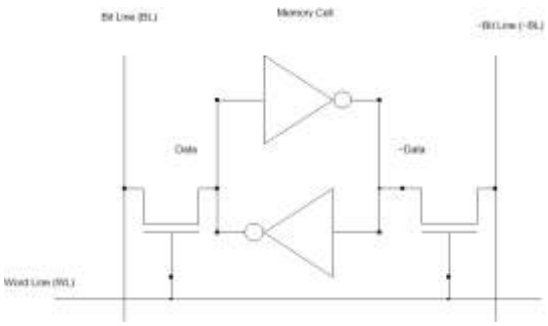

Figure 1: Logic Circuit- 6T RAM

The figure 1 shows the schematic diagram for the static 6T RAM cell. Basically it consists of 6 transistor. Out of these 6 transistors, four transistors in the centre form two cross-coupled inverters. Because of the feedback structure, a low logic value on the first inverter will generate a high logic value on the second inverter, which stores the low value on the second inverter.

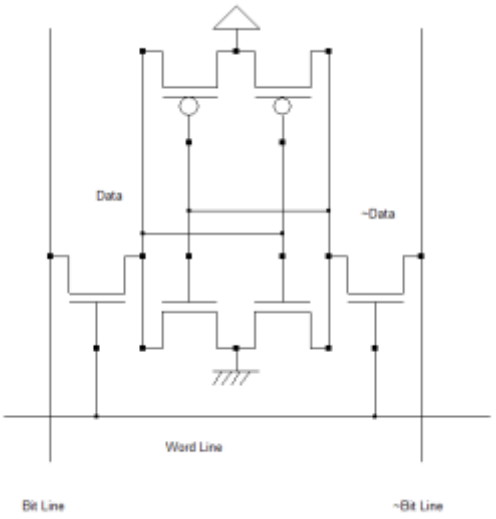

Figure 2: Schematic design - 6T RAM Cell

SRAM uses two stable latch circuitry to store each bit. Each bit is stored in two cross-coupled inverters, formed by four transistors. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistor control the access to the storage cell during read and write operations. The physical design of the conventional 6T RAM cell is shown in figure 3.

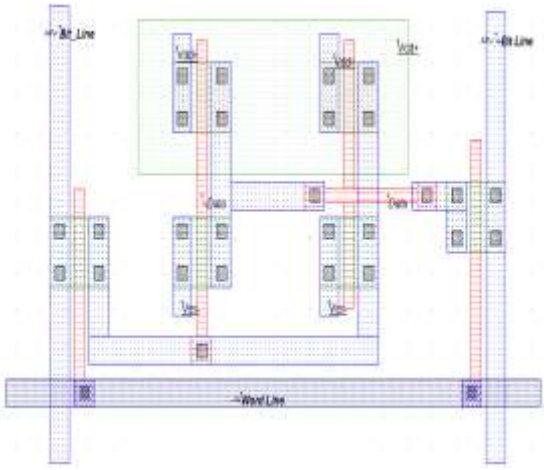

Figure 3: Physical design of 6T RAM

B. Proposed 8T RAM Cell.

In the proposed design, we are improving the power and speed, which contains two extra tail transistors in the pull down paths of the respective inverters to avoid charging of the bit lines. During write or read mode at least one of the tail transistors will be turned off to disconnect the driving path of respective inverters. Microwind 3.5 EDA tool is used for the physical design and DSCH 3.5 is used for the schematic design. The tool is used to analyse the performance of the proposed structure with 32 m Technology. The schematic of the proposed 8T SRAM cell is shown in Figure 4.

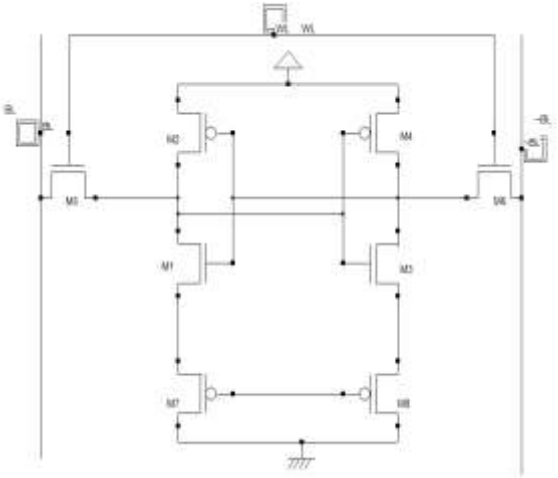

Figure 4: Proposed 8 T RAM design

This cell uses the same 6T SRAM structure for the writing operation. During write, the PMOS and NMOS transistors of the inverters can be maintained at the minimum width as the read operation is separated. The physical design of the proposed 8T SRAM cell is shown in Figure 5.

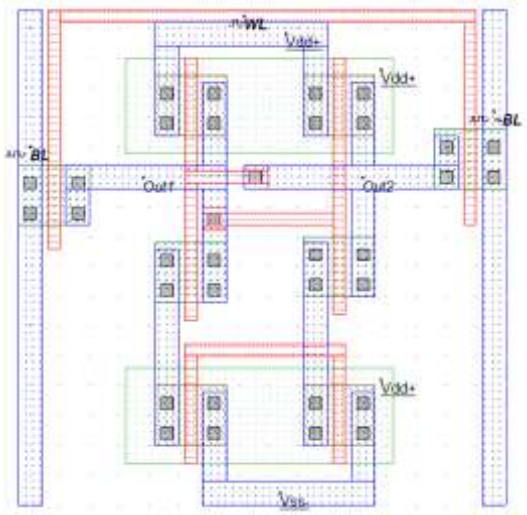

Figure 5: Physical design of 8T RAM cell

III. RESULT AND DISCUSSION:

For WRITE MODE

In conventional SRAM cell, the bit lines consume more power because of long lengths with large capacitances.

Write “1” mode: To write “1”, bit line BL is set to “0” and the word line is enabled
Values 1 or 0 must be placed on Bit Line, and the data inverted value on ~Bit Line. Then the selection Word Line goes to 1. When the selection Word Line returns to 0, the RAM is in a memory state.
Write “0” mode: To write “0”, bit line BL is set to VDD and word line is enabled.

SIMULATION.

The simulation parameters correspond to the read and write cycle in the RAM. The simulation steps proposed in figure below consist in writing a 0, a 1, and then reading the 1. In a second phase, we write a 1, a 0, and read the 0. The Bit Line and ~Bit Line signals are controlled by pulses. The floating state is obtained by inserting the letter "x" instead of 1 or 0 in the description of the signal.

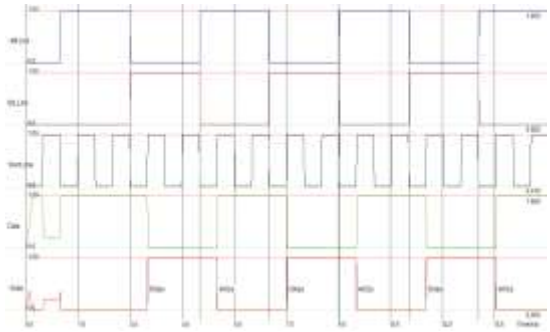

Figure 6: Simulation result of 6T RAM cell

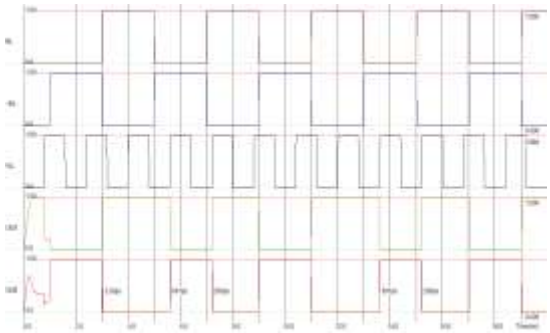

Figure 7: Simulation result of proposed 8T RAM cell

For finding out the effect of increase of VDD on the RAM cell, the parametric analysis is done on both the cells. Parametric Analysis for 6T and 8T RAM cell design is shown below;

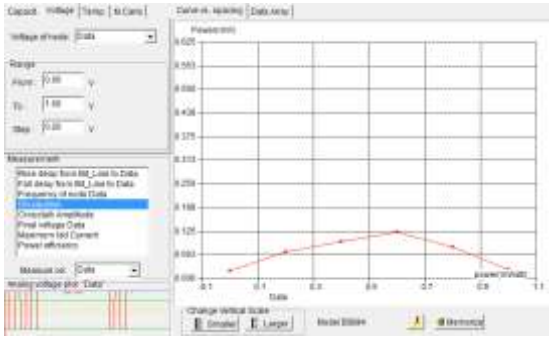

Figure 8: Parametric analysis- power dissipation for 6T RAM

The figure 8 above shows the parametric analysis for 6T conventional 6T RAM cell.

Here the voltage applied to the cell is increasing in step by step from 0v to 1 V in the step of 0.20V. The cell consume maximum power dissipation of 0.123 mW. It means that while increasing the voltage to a cell form lower voltage the higher voltages, the cell consumes more power in case of conventional 6T RAM.

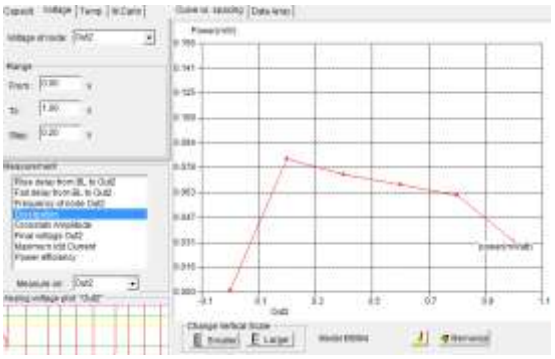

Figure 9: Parametric analysis-power dissipation (8T RAM_proposed design)

Here in the figure 9, the voltage applied to the cell is increasing in step by step from 0v to 1V in the step of 0.20V. The cell consume maximum power dissipation of 0.084 mW. It means that while increasing the voltage to a cell form lower voltage to the higher voltages, the cell consumes more power in case of conventional 6T RAM.

The comparison form the simulation result is provided with the table below. Here we can easily understand the change in voltage with the power dissipation of the cell.

TABLE I : The power dissipation of the Ram cell.

6T RAM Cell		**Proposed 8T RAM Cell**	
vdd(V)	**power(mWatt)**	**vdd(V)**	**power(mWatt)**
0.000	0.021	0.000	0.001
0.200	0.071	0.200	0.084
0.400	0.097	0.400	0.074

0.600	0.123	0.600	0.067
0.800	0.083	0.800	0.061
1.000	0.024	1.000	0.032

TABLE II. The power utilization of the Ram cell.

Power Dissipation - 6T RAM	**Power Dissipation - proposed 8T RAM**
3.609 uW	1.470 uW

TABLE III. Area utilization of the Ram cell.

Area for 6T RAM	**Area for proposed 8T RAM**
2.7um2	2.8um2

The area for the desgining is almost same as compared to the conventional 6 T RAM design.

IV. CONCLUSION

We have proposed a new design of SRAM cell to reduce the power dissipation during write operation by introducing two tail transistors. Due to these tail transistors, the proposed 8T SRAM cell provides less power consumption in comparison to 6T conventional SRAM cell. The results are verified by performing parametric analysis on the proposed cell.

The proposed design consumes less power dissipation as compared to the conventional 6T RAM cell design.

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