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Design and Implementation of Five Port Router for Mesh Network

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ABSTRACT: These days with technological progression huge number of electronic gadgets can be incorporated in a solitary framework and such frameworks are constrained by single chip called system on chip (SoC).The system on chip coordinates numerous innovation Centres (IP Centres) on a solitary chip. Due to complexity in integration of IPs on Framework on Chip (SoC). The Network on chip (NoC) is the innovation used to give lossless correspondence between these IP centres. In this paper we present the design and synthesis of router for Network on chip utilizing system Verilogcode using modelSim 10.4a softwarewhich bolsters five parallel communication in the meantime. It utilizes store and forward sort of stream control and FSM controller deterministic directing which improves the execution of router. Unit is focused to Spartan-6 XC6SLX45 FPGA design platform and synthesized in vivado software.

Index terms: FIFO-first in first out, FSM-finite state machine,Mesh Router, Mesh Topology, Network-On-Chip, Routerblock.

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I. INTRODUCTION

The system on chip is a coordinated circuit that incorporates all the electronic gadgets on a solitary chip. In this framework on chip (Soc) various Intellectual property (IP) centers are incorporated, which makes the chip high complexity. Henceforth the serious issue is to give the correspondence between these numerous IP centers. The on-chip physical interconnections (buses) will prompt vitality utilization and high delay. It is required to give legitimate on chip correspondence to these parts. Network on chip (NoC) is a way to deal with plan correspondence subsystem between postulations protected innovation centres. The bus transports can give the communication between the assets, yet this won't give any adaptability. Each time the bus structure must be modified when the design is adjusted, this lessens the gadget time to showcase subsequently NOC approach can be utilized. NoC technique better backings the coordination of SoC comprising of on switch packets exchanged system. These centers on SoC get and forward the data packets originating from various system.

Router is the essential unit of Noc which gets the approaching data packets from various centers on SoCand forward them to explicit destination dependent on the location contained on the header of information. The proposed five port router has local port used for communication between the processing element and the router through the network interface. But for the router communication we are not consider this port. And other four yield ports from which the data packets are driven out. The router in the NOC ought to be adaptable and bolsters parallel associations in the meantime. It utilizes store and forward system. It doesn't hold any dedicated channels subsequently the system traffic can be kept away from.

The routers are utilized to beat the traffic and interchanges bottleneck. The router underpins four port parallel associations in the meantime to give better execution to NoC, It utilizes store and forward sort of control which diminishes the information misfortune amid the bundle forward from source to destination. In packet switching the information moves as data packets between participating switches and the choices on course of the packets are taken freely. At whatever point the information originates from the source to the information port on the switch the switch holds the information and checks the location data on the information and send to specific yield port. In this proposed switch also known as router the plan comprises of three main blocks.

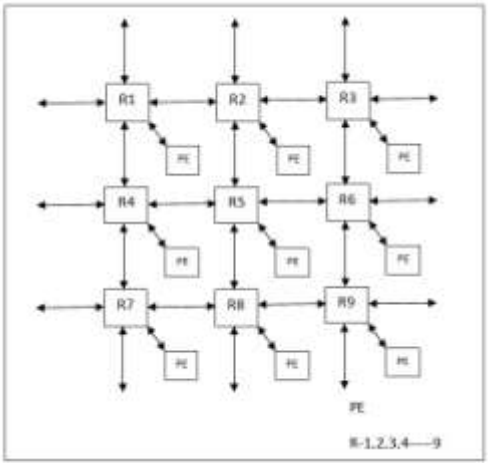
The router utilizes a register to hold the approaching information and FSM controls the tasks to be performed by the routers and the four FIFOs are utilized to hold the information to be driven out at the yield ports. The router gets 8-bit of data packet of information pursued by the header and 8-bits of information data and the parity

information toward the end of the packet to decide the achievement of data packets got at the destination ports. The router can stack 64 bytes of information data. The length of the information data is estimated assistants of payload which decide the quantity of information bytes in the packets.

II. ROUTER AND NETWORK BACKGROUND

Network topology gives the interconnection of different components (network, hubs, and so on.) of a system. Structure of NoC router design relies on the network topology. The mesh topology is a standout among the most well-known network topology to use. Two-dimensional mesh topology will be utilized to communicate the five port routers on the network. It is one of the most effortless topologies to actualize on a chip, as a result of its flat configuration. 2D mesh network comprises of m rows and n columns. The routers are arranged in the crossing points of two or more than two interconnections (ports) and the computational resources are nearby routers. Addresses of routers and resources can be effectively characterized by x-y routing algorithm in mesh. Mesh topology trouble free to design as all resources are in identical interspace as appeared in Figure 1 .

The router is the most significant part in a system on chip. It is the correspondence spine of a NoC framework. So it ought to be structured with most extreme efficiency. Routers are utilized on a system for guiding the traffic from the source to the destination. It organizes the information flow which is extremely significant in correspondence systems. Routers are smart gadgets that get approaching information packets, investigate their destination and figure out the best way for the information to move from source to destination. A router is worked by the OSI model of system on chip. Each layer plays out its own specific capacities. Fig 2 is the focal router R5 in Mesh topology of fig 1 is appeared. The focal router has 5 in/out port. One specific port in used to interface the processing element (PE) and remaining four ports are for associating with corresponding routers. Hence the five port router is also known as meh router.



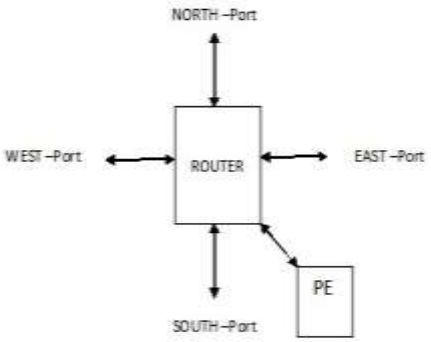


Figure 1: TypicalNoC structure in a mesh topology
Figure 2: Fiveport router (mesh router)

III. PRAPOSED WORK

The proposed router structure comprise of five main blocks i.e. register, demultiplexer, FIFO, controller and scheduler. The register is like the buffer which stores the data packets. Demultiplexer gives the channel which sends the data packets to the suitable destination port. FIFO is a first in first out memory acts as output buffers usedto controls read and write activities. The controller depends on Fsm deterministic logic which improves the execution of router. Scheduler drives the data packets from all four ports to appropriate destination port. The router which we configuration is a five port router. Router acknowledges the information as data packets. Packet contains three sections. They are Header, information and frame check arrangement. Packet width is 8 bits and the length of the packets between I to 63 bytes. The router drives the packets to separate ports dependent on the address of the packets. Figure.3 demonstrates the outline of the router block. This router block is utilized to design the focal router of Mesh topology having five input and five output ports as appeared in Figure.2.

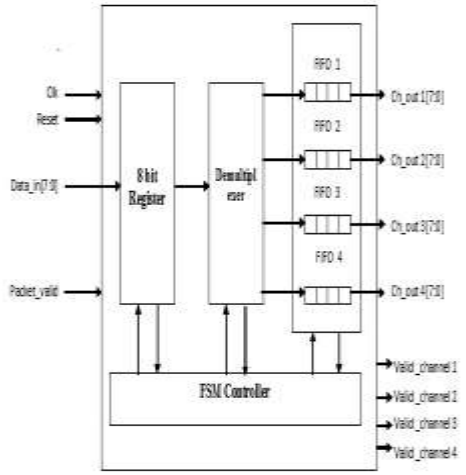


Figure 3: proposed router block

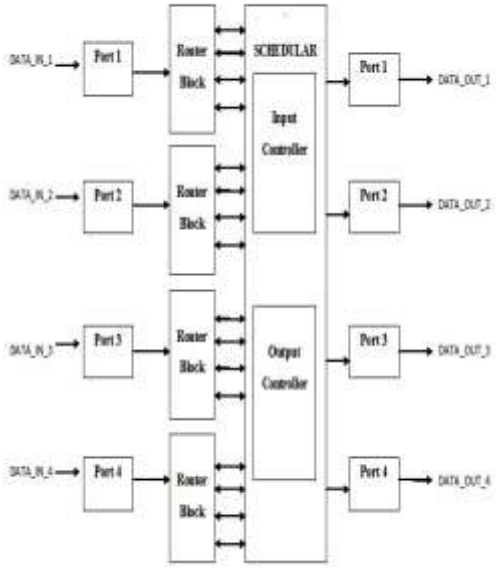


Figure 4: proposed five port router (mesh router)

1. Register

The 8 bit register is designed having clock, reset and enable. At the posedge of the clock, reset ought to be low and enable ought to be high at that point the present input data is stored in the register. At the point when enable become low, the register retrieves previous data. The register output is the input of the demultiplexer. The register is used has input buffer It stores the data transiently. the register designed is based on store and forward technique the packets was forwards only when the condition is satisfied. The usage of store and forward methods reduces the traffic

2. demultiplexer

We design the 1:4 bit demultiplexer to characterize the four output ports. The last two bits of the information goes about as a select flag which demonstrates to select one port among four. Table I Shows the output port with respect to last two bits.

TABLE 1
Identification of ports

Last two bits of data	Destination ports
00	Port 1
01	Port 2
10	Port 3
11	Port 4

Demultiplexer exchanges the data packets originating from the register block to the suitable destination port. As per the last two bits define in the table. The demultiplexer likewise has an enable. At the point when enable is high then the demultiplexer guides the data packets to the send through that port in the meantime relating write enable signal should high. And other output ports and composed write enable signals stay zero. The output of the each demultiplexerport is associated with the individual FIFO unit.

3. FIFO

We design the the FIFO having 8 bit width and memory array of 0 to 15. Here there are four fifo's to store the information originating from individual output ports of demultiplexer, It exhibits read and write operations throughFifo have fifo_full and fifo_empty control signals. Here for read and write task we utilize the synchronous clock. Writeoperation is done at the posedge of the clock when the reset is low, write enable signal is one and fifo is not full. In this condition data is write into the memory of the fifo. Read task is done at the rising edge of the clock, when reset is low and simultaneously the read enable signal is one and fifo is not empty then data packet is read from the memory of the fifo. At the point when the fifojull flag is high, it shows that every areas inside the fifo has been full and it is unfit to write the information into the memory of fifo.Also when the fifo_empty flag is high, it demonstrates that every areas inside the fifo has been unfilled and it is unfit to read the information from the memory of the fifo. For four fifo blocks there are four fifo_full signals and fifo_empty signals which is the input signals to the controller.

4. FSM controller

The controller module produces all the control signals when new data is going to the router. These control signals are utilized by different blocks to send data at output port. As the

demultiplexers output is associated with the controller, the information of the each port is acknowledged by the controller when the separate port enable signal is high just as packet_valid signal is high. At the posedge of the clock when resetn is low then only the data can be received. Fifofull and fifo_empty signals are additionally handled by the controller. There are four FIFO's with respect to four outputports. Controller checks which fifo is full, which FIFO is unfilled and as indicated by the port location it offers sign to write the information into the particular FIFO when signal of controller is high. Whenfifo_full signal turns out to be high then read from the individual FIFO and send to the particular output port of the controller. When read process is finished the data is prepared to transmit. There are four valid _ Chanel for the four output ports of the controller.if any one of the Chanel is zero, it assumes asChanel is engaged and respective fifo_empty signal is high. It means the data is ready to write into the present fifo. The suspend_data signal generated by controller is used to indicate the acceptance of the data packets from demux output port to the FIFO when suspend data signal is low. Write enable pin is generated from controller for writing the data into present FIFO.

5.Scheduler

The scheduler design as shown in fig 4 is utilized a round robin scheduling method. Scheduler is most important block which communicates directly to the all four ports it assign data packets from router block to output ports. It expect that all data are similarly valid for choice. The data at each fifo blocks are generated to scheduler block in round robin form and datais received at the output port based on the priority through the scheduler. The scheduler is partitioned into two parts.

Input scheduler: Scheduler used cross bar switch technique to assign the data packets to the appropriate destination output ports .main function of input scheduler is selection the data packets from the fifo blocks to send through cross bar switch form in order to win the output port and also where the data packets should store in the fifo block before it send to output port

Output scheduler:output scheduler assign the data packets to the output ports from the input scheduler block through cross bar switch arbitration.it selects which 4 packets will send to four output ports from the input scheduler among 16 data packets.

IV. IMPLEMENTATION OF ROUTER DESIGN TO MESH NETWORK

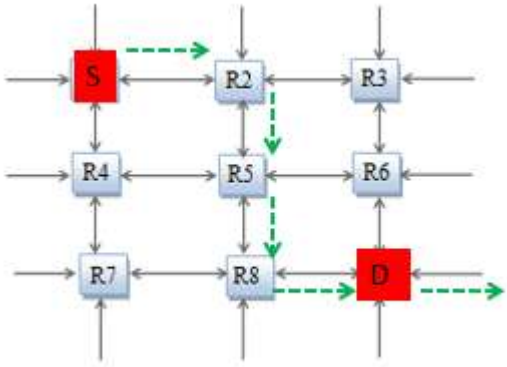


Figure 5:3×3 mesh network design

The router is implemented on mesh network as shown in figure 5.here R1 to R9 are 9 individual routers from 1 to 9with four ports for four directions. The data packet in single router can communicates through any of four ports.It uses x-y algorithm to transfer the data packets from one router to corresponding router the data packets should move in x direction or y direction only.A network organize topology comprises of m section and n lines. The router are arranged in the interconnection of two wires and processing element is close to router. Addresses of router and resource can determined freely from x and y paths. Here the communication is done from source router R1 to destination router R9.Datapackets from router one R1 is transferred to the router 2 through east port of R2.Then data packet goes to router five from the south port of R2 and received to router R5 through its north. After that the data packets transferred to the router 8 from the south port of R5 through the North port of router R8.finally the data packet is received at destination router R9 from the east port of router R8.

V. SIMULATION RESULT

Figure 6 shows the simulation of router block simulated in modelSim 10.4a software.Router block accept the data packets at input port at the posedge of clock when resn signal is low, respective read enable pin is high and suspend_data signal is zeroas well as register and demux enable pin also high. As the input packet 8'h0e it indicates the data should get at port 3.when fifo get full, controller send signal and data is get at ch_out3.

Figure 7shows the simulation of five port router the four input packets of the size 8 bit data is send through the four input ports and those four data packets was received through that router output ports i.e. the input data 8'h0b is send through the port of north and that data is received at

the west port similarly the input data 8'h0c is send through the port of east and received at the north port, the input data 8'h0d is send through the port of south and received at the east port and the input data 8'h0e is send through the port of west and received at the south port after every clock cycles. The data received at destination port is based on the last two bits of the 8 bit data for last 2 bit 00 the output port is north similarly for 01 the output port is east and for 10 the output port is east and lastly for 11 the output port is west. Here packet valid signal indicates that input port accept the valid_data by indicating 1 and 0 if not valid. And valid_chanel signal indicates that output port is ready to transmit when data is get at output port by indicating 1 and 0 if no data at output port.

Figure 8 shows the simulation result of mesh network. The data packets from source R1 to destination router R9 is flows through the intermediate routers. The output data packet 8'hc8 of 8 bits is input through north input port of router one i.e. north _out1. Then packet communication through the routers east _out2, south_out5, east_out8 and finally to router 9 of east_out9 port.

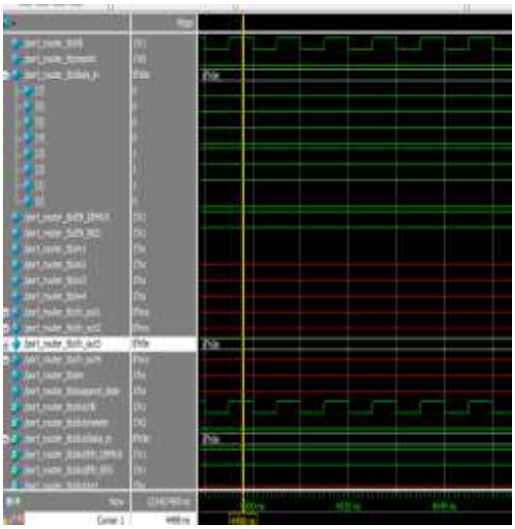


Figure 6: simulation of router block

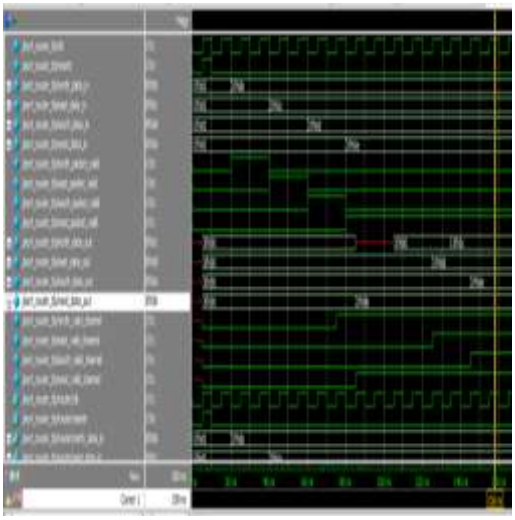


Figure 7: simulation of five port router

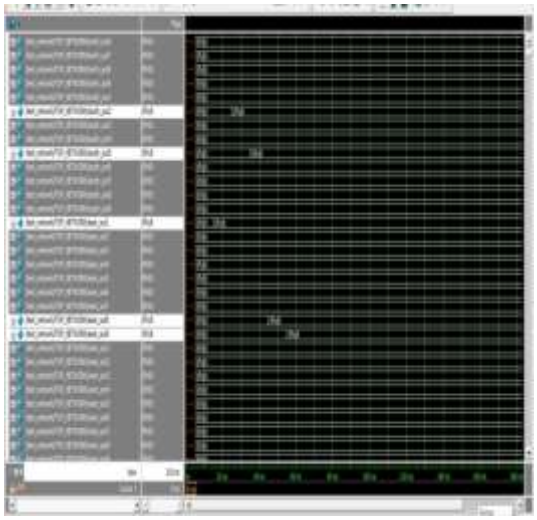


Figure 8: simulation of 2×2 mesh network

VI. SYNTHESIS RESULTS

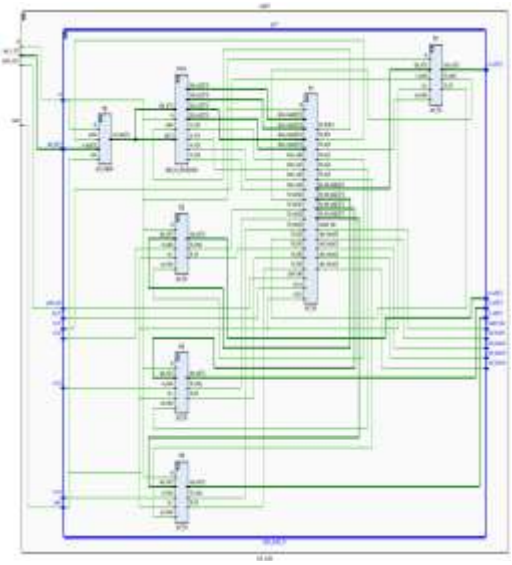


Figure 9: RTL schematic of router block

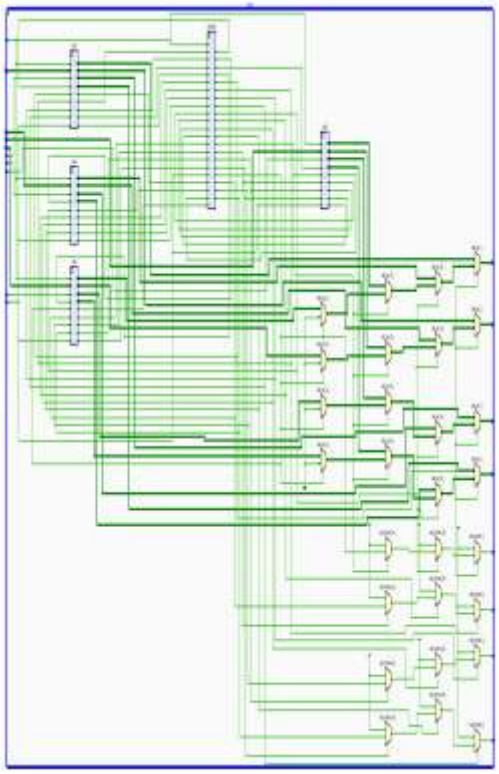


Figure 10:: RTL schematic of five port router

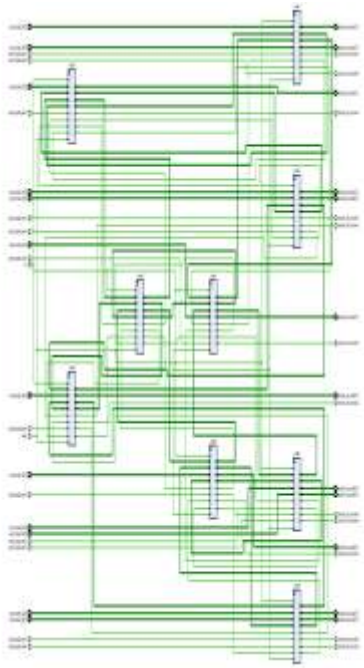


Figure 11: RTL schematic of 3×3 mesh network

The RTL view of the proposed structure has been synthesised by utilizing Vivado software. figure.9 shown is the schematic of a router block with the essential modules for example Register, Demultiplexer, FIFO and Controller having one inputand four output port and Figure 10 is the RTL schematic of five port router. The design has a four input ports and four output ports which include four router block and one scheduler block. Figure 11 is the RTL schematic of 3×3 mesh network where five port routers were interconnected each other with corresponding five port routers in 3×3 order to create mesh topology.Figure 12.a shows the resource utilization report of the proposed five port router and 12.b shows the power consumption of the design in power estimationreport.

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	682	0	8000	8.53
LUT as Logic	490	0	8000	6.13
LUT as Memory	192	0	5000	3.84
LUT as Distributed RAM	192	0		
LUT as Shift Register	0	0		
Slice Registers	532	0	16000	3.33
Register as Flip Flop	532	0	16000	3.33
Register as Latch	0	0	16000	0.00
F7 Muxes	0	0	7300	0.00
F8 Muxes	0	0	3650	0.00

Figure 12a: Resource utilization table

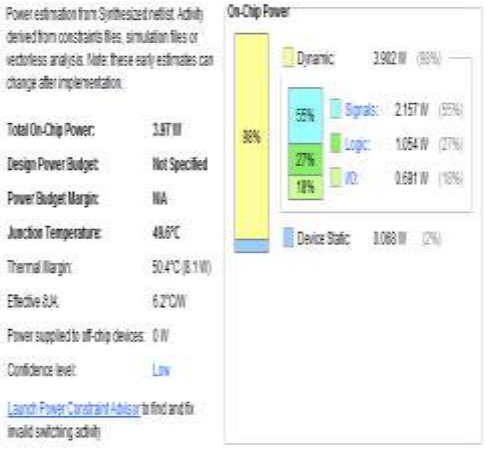


Figure 12b: power estimation report

VII. CONCLUSION

Here we have proposed the router which supports five connections at the same time without any communication congestion. We have used simplest store and forward flow mechanism, packet switching, XY deterministic routing, input and output buffering which increases the performance of router. In this paper we proposed a 5 Port router design and implement on 3×3 mesh network for effective data transfer.simulation was done using the systemverilog coding in modelSim 10.4a software and synthesized in vivado software with FPGA Spartan-6 implementation.

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