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A Comparative Study of Ring VCO & LC-VCO based PLL

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ABSTRACT: In the present life, Phase locked loop (PLL) have turned out to be universal in modern communication systems. Voltage controlled oscillator (VCO) is the most essential part in radio frequency systems. This paper presents a comparative review of Ring VCO and LC-VCO in PLL on the premise of their performances with respect to different criteria. The ultra-fast wire line application use LC-VCO because of their more extensive tuning range since the DC-levels of the two yields in LC-VCO are roughly 50% of the supply voltage. Based on the study it was discovered that LC-VCOs are the most important part utilized in superior RF frameworks because of their ultra-low phase noise and power dissipation than Ring VCO. Further different trade – offs of the two VCOs are likewise looked at.
Keywords: Ring oscillator, LC-VCO, Phase locked loop (PLL), phase noise

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I. INTRODUCTION:

These days, the Phase locked loop (PLL) is utilized in different applications, for example, radio, media communications, PCs and so forth. Regardless of whether to demodulate a signal or recover a signal from a noisy communication channel, PLL has an imperative use. Indeed, a chip installed with its very own clock generator to give the rapid clock flag, clock recovery and synchronization of chips or phase noise decrease, each circumstance needs PLL. In electronic frameworks, oscillator is the key component in designing of PLL, Digital PLL (DPLL), recurrence synthesizer and media transmission systems. VCO is a piece of electronic circuit which changes over the input voltage into its corresponding frequency at the yield/output. Oscillator has most extreme tuning range, recurrence and phase noise. The overall execution of PLL is improved by the oscillator utilized. For CMOS based VCO configuration in present innovation, LC and Ring based VCOs are two choices utilized in PLL structuring. LC-VCO based PLLs are utilized for high recurrence activities as they have superior phase noise performance.

II. PLL ARCHITECTURE:

PLLs are generally utilized in present day integrated circuit based high-speed advanced systems to play out an assortment of clock handling undertakings, for example, clock recurrence duplication and clock de-skewing. PLL is a controlled framework that produces an output signal whose phase is in relation to the phase of the input signal.

The architecture of PLL is made out of five noteworthy obstructs: phase-frequency detector (PFD), a charge pump, a second order loop filter, a VCO and a divider. In Figure 1, the diverse squares of PLL are shown. The oscillator creates an occasional flag.

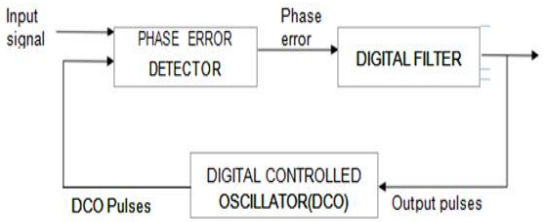

Fig 1: Block Diagram of PLL

The job of oscillator is to generate a periodic signal. The phase detector compares the phase of the signal with the phase of the input periodic signal, adjusting it to keep the phases matches. By changing the divide ratio of the frequency divider, PLL can orchestrate another frequency which is dependent upon the reference input while holding the steadiness and spectral purity of the original reference.

III. RING VCO VS LC-VCO:

For CMOS based VCO design in present technology, LC and Ring based VCOs are two typical choices used in PLL designing.

a) Ring Oscillator:

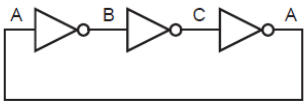

Fig 2: Ring VCO

Ring oscillator is utilized in media transmission systems, estimating the impacts of temperature and voltage on chip. It is used in PLL designing. Numerous wafers have a ring oscillator which acts as scribed line test structures. They are used for estimating the impacts of assembling process variation amid wafer testing. Jitter of ring oscillator is utilized in equipment random number generator. Because of their poor phase noise performance, ring oscillators are very rarely utilized in RF systems. These oscillators are easy to incorporate however they have very high phase noise. In spite of all these facts, Ring VCOs are quite often used in high speed data links.

b) LC Oscillator:

LC oscillators have low phase noise which makes them appropriate for use in radio frequency frameworks. They have a larger area when contrasted with ring oscillators.

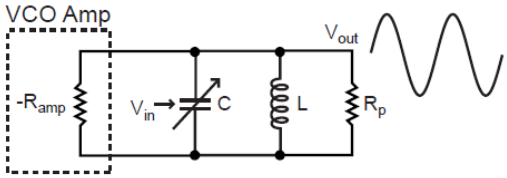

Fig 3: LC Oscillator

LC-VCOs are utilized to give input for mixers to up-convert and down-convert signals and have primary significance in fully-integrated transceivers. The best combination of very low-phase noise specifications with very low power utilization (battery operation) urges the VLSI planners to use LC-VCOs more in different areas.

In paper [1], the essential parts of the PLL circuit for RF application – a PFD and a VCO were planned and executed in a standard CMOS process AMS 0.35 micrometer. The proposed LC oscillator was structured and acknowledged utilizing double cross topology with A-MOS capacitance tuning component with the supply voltage of 2.7V. The tuning scope of the proposed VCO was more than 500MHz, along these lines the accomplished outcome demonstrated that for a superior RF building squares, LC-VCO is viewed as best.

The chip area, power utilization and frequency range were considered as essential parameters for structuring of Ring oscillator in [2]. Low frequency/recurrence range, conventional ring oscillator contained more power and huge chip zone. Different topologies were utilized to structure a ring oscillator to enhance the recurrence run, reduce power consumption and small chip area was investigated.

Further the power utilization of four unique topologies of LC tank VCO were thought about and compared in [3]. It was discovered that as supply voltage diminishes, power consumption likewise decreases and therefore there was low phase noise. This phase noise accordingly offered to lessen the start up vitality preserved by the RF transmitter.

In [4], the execution of two clock generation PLLs was analyzed, a ring based PLL and an LC based PLL with the design experiment. It was obvious from the subjective assessment that in chip territory, control utilization and tunable frequency range, a ring PLL is better than LC-PLL, however with respect to phase noise and jitter, a LC-PLL is far phenomenal. It was additionally anticipated that the relative execution distinction between both the VCOs will end up steady sooner rather than later.

Table 1: Performance comparison between two PLLs [4]

	Ring PLL	**LC PLL**
Technology	**0.18µm digital CMOS,5LMM, 1.8V**	
Frequency Range Power consumption Phase Noise @ 1MHz Core Chip area	400MHz-1.8GHz 10.4mW -65dBc/Hz 0.07mm^2	1.49GHz-1.64GHz 22.1mW 29ps/3.6ps 0.26mm^2

Again in [5], the examination of jitter, power and area between LC and Ring VCO based PLL was done in a standard 90nm CMOS process technology. It was seen that for a PLL plan which required a wide recurrence run, an LC-VCO based PLL would require numerous VCOs to switch between recurrence ranges.

In this manner, from the above review and study, Table 2 unmistakably demonstrates the outline of the trade-offs among Ring and LC-VCO based PLL plans. Each of the VCO has its own particular advantages and disadvantages.

Table 2: Tradeoffs of LC and Ring based PLL [5]

VCO Type	**ADVANTAGES**	**DISADVANTAGES**
Ring VCO based	• Common approach for digital chips	• High phase noise->Widen loop BW to reduce

PLL	• Many ways to control frequency • Multi-phase clock generation • Wide frequency tuning range	• High VCO gain->sensitive to disturbance • Not suitable for SONET transmit clocks • Poor stability at high frequency
LC VCO based PLL	• Common approach for RF design • Good stability • Long term and period jitter filtering • Low long-term and period jitter • Low phase noise	• Larger layout area->larger area for inductor • Narrow tuning frequency range • Requires a lot of characterization • More complex design

IV. CONCLUSIONS:

Based on the above study, it has been discovered that a Ring VCO based PLL has more extensive loop bandwidth with higher phase noise response and it is most appropriate for clock and information recuperation circuits, while an LC-VCO based PLL has smaller loop bandwidth with predominant phase noise response which is very much coordinated for RF-applications.

Likewise, the outcomes demonstrate that a Ring VCO based PLL can meet the execution prerequisites of a specific rapid clock synthesizer application if the PLL circle transfer speed is appropriately improved. However, for RF applications, LC-VCO based PLL is the best.

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