RESEARCH ARTICLE OPEN ACCESS

Design Of Pipelined RISC MIPS Processor Using VLSI Technology

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ABSTRACT: The main aim of this project is to design and implement RISC MIPS processor using VLSI technology. The project involves simulation and synthesis. The processor is designed with Verilog HDL, synthesized using XILINX-13.1. A Reduced Instruction Set compiler (RISC) is a microprocessor that had been designed to perform a small set of instructions, with the aim of increasing the overall speed of the processor. The idea of this project was to create a RISC MIPS processor as a building block in Verilog HDL. Each block is separated by pipeline to speed up the processor. High level of complexity is easier to implement the function in software. The objective of project is to increase the speed and reduce the power consumption. Single cycle execution method applied to complete one instruction through all stages.

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I. INTRODUCTION

Reduced Instruction Set Computers (RISCs) are now used for all types of computational tasks such as DSP, DIP etc. A RISC is a microprocessor that is designed to perform a smaller number of types of computer instruction so that it can operate at a higher speed. John von Neumann designed a Reduced Instruction Set Computer (RISC) includes separate data memory and program memory to execute a set of instructions. The aim of project is to implement the five pipelined stage processor using RISC and MIPS architecture. Using single cycle, processor executes instructions and increases the overall speed and reduces the power consumption. In this work, analyze MIPS instruction format, instruction execution path through all stages, control unit performance for each instruction. Project designed with RISC philosophy, for load and store separate instructions used. To avoid access of memory repeatedly, separate register bank is designed. The project is build using Verilog HDL. The code is synthesized and simulated using XILINX-13.1.

II. OBJECTIVES

- To increase instruction execution speed and to reduce the power consumption of RISC processor.
- To apply single cycle execution method to complete one instruction through all stages.

III. MOTIVATION

Reduced Instruction Set Computer is a type of microprocessor. RISC processors are also used in supercomputers such as ‘k’ computer and especially representing a major force in the UNIX workstation market as well as embedded processors. It reduces the transistor count of a MIPS processing unit by scaling down the bus and register width.

IV. LITERATURE SURVEY

Table.No:1-Comparison of different technologies used forRISC implementation.

Sl.no	Author	Title	Technology	Limitations
1.	N.Alekya, P.Ganesh Kumar	Design of 32-Bit RISC CPU Based on MIPS	MIPS	VHDL language is used to implement the 32bit processor
2.	Galani Tina G. Riya Saini and R.D.Daruwala	Design and Implementation of 32 – bit RISC Processor using Xilinx	Spartan 2E	A 32 bit RISC processor build using xilinx virtex4 Tool for embedded and portable applications required minimum area and minimum delay
3.	Navneetkaur, Adesh Kumar, Lipika Gupta	VHDL Design and Synthesisof 64 bit RISC Processor System on Chip (SOC)	Spartan 2	Four stage pipelines used. 8bit and 16 bit instruction set is used to access logical, arithmetic and memory, jump instructions
4.	R.Uma	Design and Performance analysis of 8-bit RISC Processor	XlinixTool	For sign multiplication Booth Multiplier is used

V. SYSTEM MODELING

Figure 1 illustrates the procedure to design a system. With the help of XILINX 13.1, all stages of processor are developed as a separate module using Verilog language. Bit file generation is important criteria to dump into any FPGA.

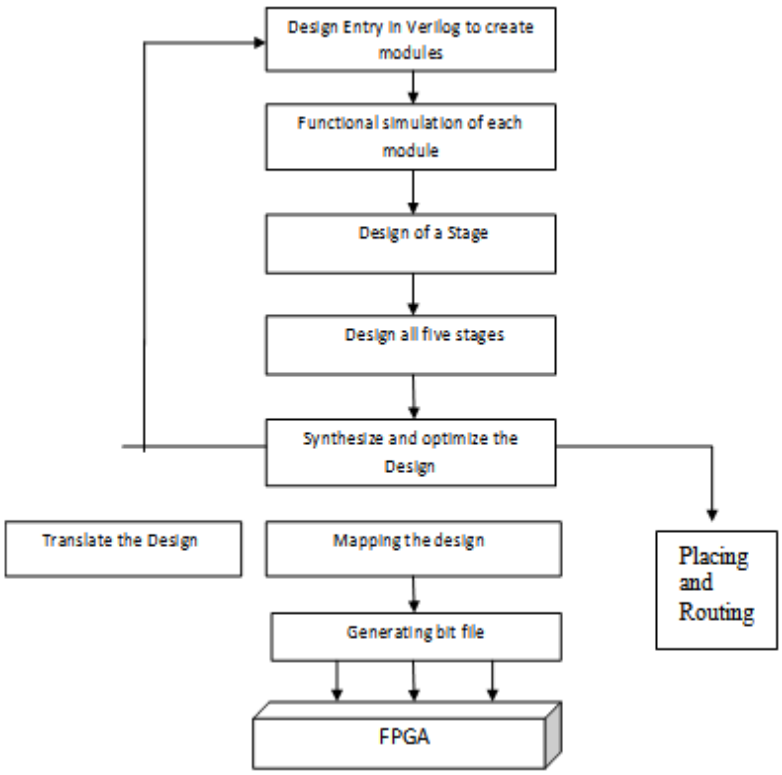

Figure 1: Generation of bit stream for FPGA

Construct five pipeline stages

The project includes instruction fetch stage (IF), decode stage (ID), execution stage (EX), data memory (MEM), write back (WB) stages. For jump instruction separate block is designed. Pipeline consists of the overlapping of set of instructions. Pipeline reduces the execution time of instructions.

The processor executes an instruction in single cycle. Each instruction passes through all stages or passes according to instruction. Program counter loaded with the address it acts as a pointer to the program memory.

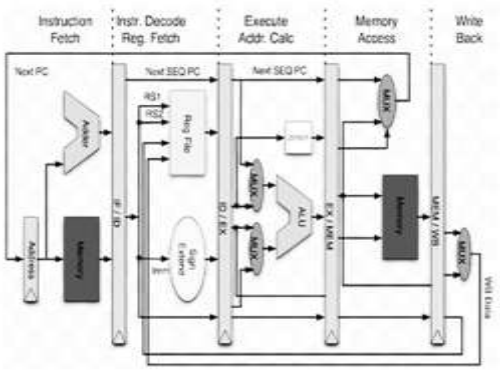

Figure 2: Five Stage Pipeline

Instruction Fetch

The program memory loaded with Instructions. The instruction fetched from memory. Each time program counter has the address of memory location. All fetched instructions passed to decoder stage through latch.

Instruction Decode

The Instruction Decode stage decodes the instruction. The six bit Opcode is passed to the control unit to generate the signals according to instruction code. The data passed through decoder latch for execution as per signals generated by control unit. Sign extension unit used to extend the value according to control signals. If instruction is load or store type, immediate [15-0] bits extend to 32 bit for ALU. In decode stage Register Bank performs as cache memory to store the data for fast calculation.

Execute Stage

In Execute stage, the instructions are executed. All arithmetic and logical operations perform by ALU. Type of operations are addition, subtraction, AND, OR etc.

Memory Access

Data memory is storage device accessed as per the load and store instruction. For load instruction, Data is loaded to register bank from memory. For store instruction, current data stores in the data memory.

Write back stage

The result writes back to the register file. All instructions passed via Write back stage. Except nops and store type of instruction.

Advantages:

- Easier to implement.
- Faster clock speed.
- Power consumed per instruction execution is less.
- Simpler hardware.
- Shorter design cycle.
- Few

er transistors count for RISC cores.

Applications:

- Used in video processing, telecommunication and image.
- Used in digital signal processing.
- Used in high performance applications like servers (mobile).
- Used in embedded applications where ultra low power consumption is needed.
- Used in virtualization and memory management.

VI. SIMULATION RESULTS:

Figure 3: All gates

Figure 4: Adder

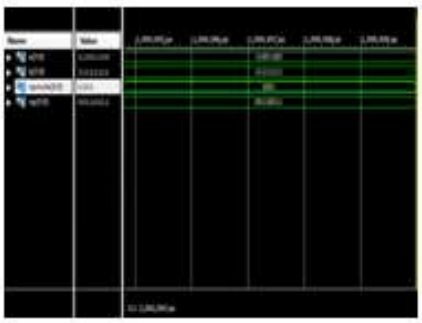

Figure 5: Arithematic & Logical Unit

Figure 6: Multiplexer

Figure 7: Encoder

Figure 8: Decoder

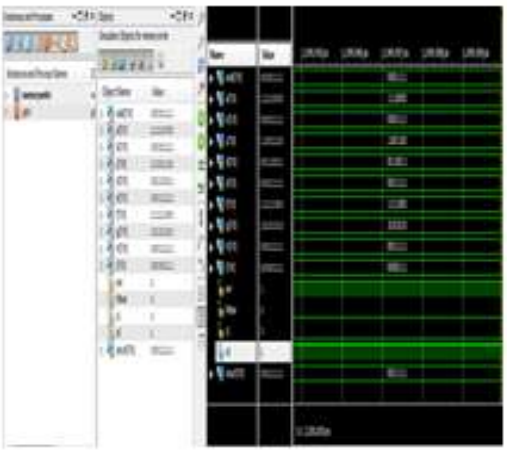

Figure 9: Memory Read

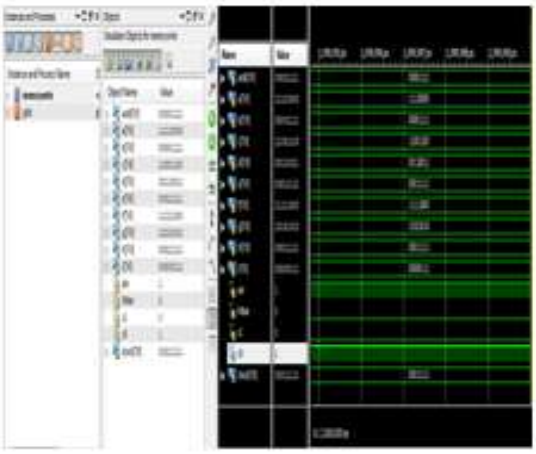

Figure 10: Memory Write

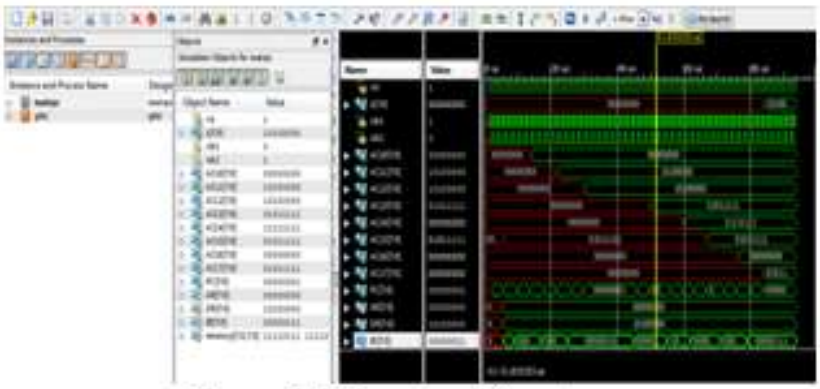

Figure 11: Program Counter

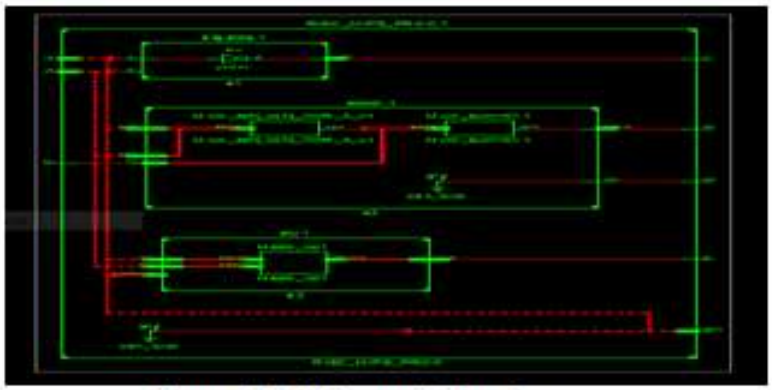

Figure 12: Schematic Results

VII. FUTURE SCOPE AND CONCLUSION

The RISC MIPS architecture of pipelined 8 bit is executed successfully and got the correct results. The project has reduced the power consumption considerably, and increased the speed of execution. The program has given correct results for number of times. The project code is much efficient in terms of number of bits and in reducing the amount complexity accomplished. This project can be further modified to obtain the results for the numbers with the numbers of bits greater than 16 bit and 32 bit and memory management.

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