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Operation and Design Considerations for a High-Power Density Ultra High Step-Up DC-DC Converter

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ABSTRACT
This paper proposes a new dual-coupled inductor (CI) single-switch high step-up DC-DC architecture with high power density. To serve as a more effective power interface between the input and the load, a variety of capacitive and inductive power transfer techniques are applied. To disperse the total output voltage, reduce voltage ripple in high-voltage gain ratios, and lessen voltage stress on the port component, the output terminal has three ports. The proposed converter has the following features: (i) a high voltage gain at lower switching duty cycles; (ii) recycling the stored energy of magnetizing and leakage inductances in both Cls; (iii) reducing switch voltage spikes; (iv) operating without circulating current; (v) presenting low-size passive components; (vi) obtaining high-power density and widened voltage range; and (vii) providing a simple PWM using a wide control range. This research analyzes the steady-state operation in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM), and it compares the converter's performance to similar works to assess its performance. Furthermore, experimental outcomes have been shown to support the design's viability.

Keywords: DC-DC Power Conversion, High Step-up Converter, High Power Density, Coupled Inductor

I. INTRODUCTION

DC-DC converter design is usually difficult [3] and reaching a higher output voltage and voltage gain are generally important considerations [6]. Voltage multiplier cells (VMCs), linked inductors (CIs), and switched capacitor (SC) modules are a few common methods that may be used to increase the voltage gain. Switched capacitor converters disperse the voltage stress of the primary switch in the absence of inductors in the converter structure, and the resultant converter's voltage-boosting capability may be increased. However, the disadvantages of these low-efficiency converters include high current stress over the main switch, significant switching losses, inrush currents of the capacitors during switching transitions, and trouble adjusting the voltage of the capacitors [7]. Furthermore, the components have a very high di/dt when they flip between states. Thus, using an auxiliary current sniffer should address this problem [8]. Consequently, CIs continue to be desirable options for DC-DC converters looking to achieve the high voltage gain characteristic.

Even by putting the CI's turns ratio or duty cycle range in the middle, embedding CIs in the converters can help boost the voltage gain. By doing this, the rectifier diode's reverse-recovery problems will be resolved. Two comparable converters with a single switch and a large step-up voltage gain have been shown in [10]. To increase voltage gain while recycling the energy in the leakage inductance, these converters combined CI and VMC. The primary disadvantages of these converter topologies are increased output voltage ripples and a notably high VMC inrush current (during the switching transition period). The researchers in [11] used a similar method to accomplish a soft-switching performance for the converter by using two switches. Although the goal of [11] is to reduce switching loss, the use of two switches in the structure increases conduction loss, increases the difficulty of controlling the switches, and narrows the duty cycle range of the primary switch. In [12], the interleaving technique was used to a coupled-inductor converter. The voltage stress on the switch has been reduced by the structure that is being provided, and the input current is drawn with little ripple. However, there are a significant number of semiconductor components, and their parasitic capacitances are crucial in ensuring flawless performance. To increase the voltage gain at the converter's output terminal, the researchers in [13] combined VMC and CI and used them in an interleaved boost converter. However, the

utilization of two big CIs results in an increase in the converter's size.

Two comparable-structured DC-DC converters that use VMC and CI to lower voltage stress and increase voltage gain have been proposed in [6]. On the other hand, the magnetizing and leakage inductances are not used appropriately. To have a large voltage gain, a three-phase interleaved converter has been suggested. Because the construction uses two switches and a linked inductor in each phase, the converter is difficult to install and costly. The DC-DC converter was first presented in [7] with the goal of obtaining a high voltage gain and soft-switching capability. This converter's excessive input current ripple is its primary flaw. Furthermore, a high duty cycle is required to achieve the desired voltage gain, which results in increased conduction loss. Two step-up converters have been shown in [1] using the interleaved approach. The input current auto-balancing was the main objective of these converter architectures. These methods have several drawbacks, such as an issue with electromagnetic interference (EMI), high resonant currents, and excessive operational modes that complicate control. In [20], CI and VMC are combined to provide an interleaved DC-DC converter with minimal input current ripple and high voltage gain. However, the primary shortcomings of this arrangement are its excessive number of circuit parts and restricted duty cycle range. The authors of the recommended methods in [2] focused on lowering the input current ripples. Less efficient VMC limits this interleaved-CI DC-DC converter's actual implementation viability.

The following are the primary issues with the most recent CI-embedded converter topologies: circulating current losses, a limited duty cycle region, an inefficient use of leakage and magnetizing inductances, an excessive number of CI turns ratios or high duty cycles to achieve high output voltage gains, an issue with the amount of output voltage ripples, an excessive use of components yielding lower power density, and an issue with the inrush current of voltage multiplier cell capacitors during switching transitions are all listed. We suggest a high step-up DC-DC converter as a solution to the issues. This converter reduces or eliminates the constraints and has a broad range of applications in electroplating, DC power supply, motor driving systems, and renewable energy systems like solar. The work is divided into several areas, including operation analytics, power loss estimates, design process, comparative analysis, and experimental findings from a 600W prototype.

II. PROPOSED CONVERTOR

Fig. 1 shows the suggested DC-DC converter with high step-up voltage gain and dual-CI technology. Six diodes (D1–D6), two connected inductors with two and three windings, four capacitors (C, Co1, Co2, and Co3), and one power switch (S) make up this converter. An ideal transformer is used to mimic the three-winding coupled inductor. It has turn ratios of n1: n2: n3, magnetizing inductance (Lm), and leakage inductances (Lr1 and Lr2). Additionally, an ideal transformer model with n4: n5 turn ratios and Ln, Lk1, and Lk2 inductances is used to represent the input coupled inductor. Flyback and forward procedures are used in the converter structure to convert the input voltage (Vi) to high output voltages (Vo1, Vo2, and Vo3). The output voltage (Vo) in the output terminal is provided by the arrangement of the corresponding capacitors (Co1, Co2, and Co3).

2.1 – CCM Operational Interval

The suggested converter operates in continuous conduction mode (CCM), with two distinct intervals marked by the ON and OFF states of the S switch Figure. 2. Investigating the converter's performance is done under the following assumptions:

- The parts are thought to be perfect.
- The converter is in a steady state when it comes to the waveforms and operational analytics.
- It is assumed that the capacitor voltages (VC, Vo1, Vo2, and Vo3) are ripple-free.
- The corresponding voltage and current of the leakage inductances (vLr1 and iLr2) are omitted if the values of voltage and current are low on the main (low voltage) and secondary (high voltage) sides of the coupled inductor, respectively.

The following provides an explanation and formulation of each operational interval, and Fig. 3 shows the waveforms of the primary components in the steady state of the components under the previously indicated assumptions. Pulse width modulation (PWM) control (GS) drives the single switch of the proposed converter (S), as seen in Fig. 3. This causes the switch to be in the ON and OFF states in 0<t<t according to figure 2, switch S is ON and Vi charges $\boldsymbol{L=L_n+L_k}$ via D_2 which yields:

$$i_l(t) = \frac{V_i}{L}t + I_l(0)$$

Where, I_l (0) is the initial current of L at t=0

The input power cannot be transferred to Vo1 while D3 is in the OFF state. Lm is charged by the energy stored in C, which is then sent to n2 and Vo2 via n1, activating the diode D4. The voltages (vLm and vLr2) across Lm and Lr2 are computed as

$$v_{Lm} = \frac{V_i}{(1\ -\ D}, v_{Lr^2} = V_i \frac{n_2 - D(n_2 + n_3)}{n_1(1-D)}$$

where S's duty cycle is represented by D in the equation above. Based on the values of D, n2, and n3, which determine the charging or discharging states of Lr2, i.e., diLr2/dt > 0 or diLr2/dt < 0, it can be deduced that the sign of vLr2 might be either + or -. The energy flow may also be found in intervals 1 and 2, as Fig. 3 illustrates.

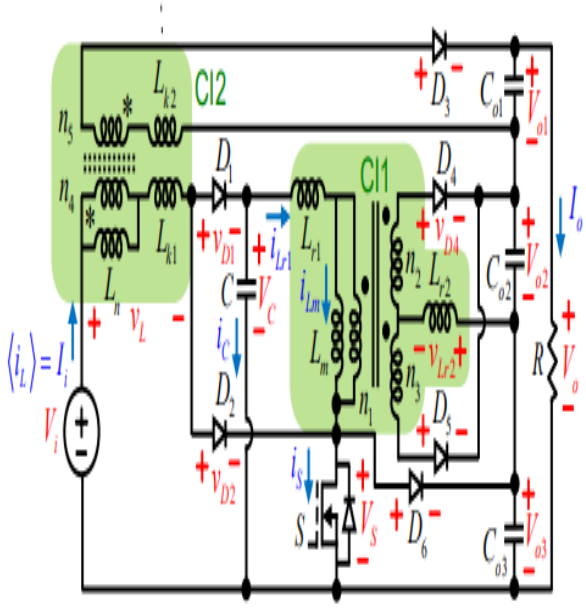


Figure No. 1 - High step-up DC-DC converter structure proposed.

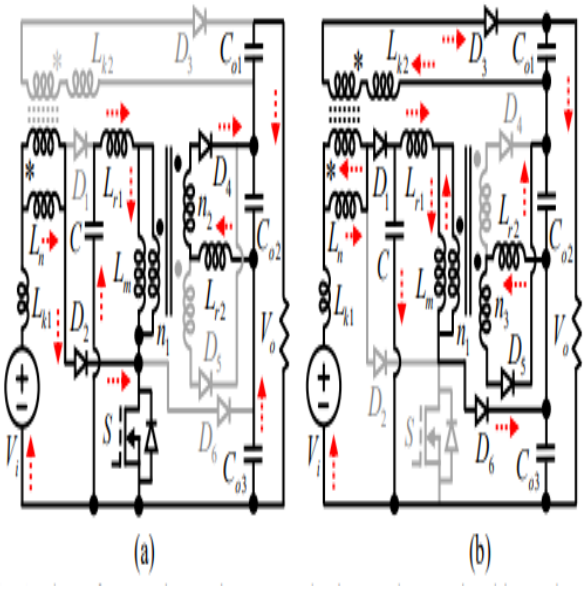


Figure No. 2 - The following describes the current flow during Continuous Conduction Mode operational intervals

S is switched off at t = DTS, which changes the switching states of diodes D1, D2, D3, D4, D5, and D6 into ON, OFF, ON, OFF, and ON states, respectively, after the switch duty cycle. The energy that was stored in the inductance (Lk) is released to the capacitor (C) in the following phase. Consequently, that energy is moved to Co3, where the following equation states that iL(t) is decreased.

III. VOLTAGE STRESS ANALYSIS

Applying (10), one can compute the voltage stress of the power switch (S) during (1-D) TS using the resulting capacitor voltage equations in (7) and (8). The normalized form of the voltage stress (VS / Vo), as shown in Fig. 6, is regarding D, a, (n2+n3)/n1, and n5/n4.

$$V_s = \frac{V_i}{(1\ -\ D)^2}$$

states that the turns ratio of the CIs has no bearing on the voltage stress experienced by the power switch. Therefore, it is possible to achieve both high voltage gain with high (n2+n3)/n1 and n5/n4 values and conduction loss reduction by using low voltage-rated power switches with low drain to source resistance as the power switch (S). Figure depicts the intended operation zone for design consideration from the perspective of switch voltage stress. where: (i) the normalized switch voltage stress decreases with increasing "a" value; (ii) low switch voltage stress occurs in the most frequent duty cycle range of high step-up converters (0.5 < D < 0.85); and (iii) the suggested converter topology offers a sufficiently wide switch design area. The voltage stresses on the diodes may be computed using the following formulas.

$$|V_{D1}| = \frac{V_i}{(1-D)}, |V_{D2}| = \frac{V_i D}{(1-D)^2}$$

Provides a three-dimensional representation of the normalized per-unit accumulative voltage stress on diodes in Figs. 10 and 11 to attain the intended design region for the voltage of the diodes. These numbers show that the suggested converter offers a reasonable design area when seen from both the "a" and "D" perspectives. A larger fraction of the solution area is devoted to 0.5 < D, which is more likely to occur in high step-up converter applications. Furthermore, by considering the voltage stresses on the diodes, raising (n2+n3)/n1 is a better option than n5/n4 to attain high voltage gain.

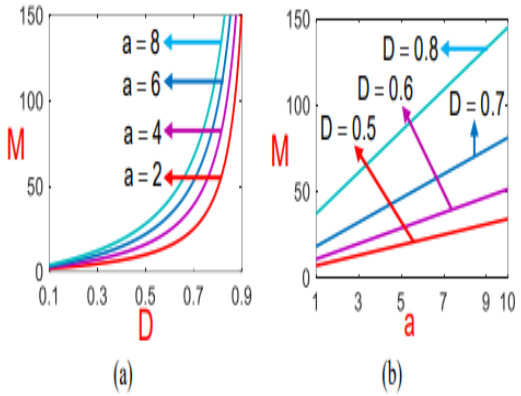


Figure No. 3 - Voltage gain in terms of; (a) Duty cycle. (b) CI turns ratio.

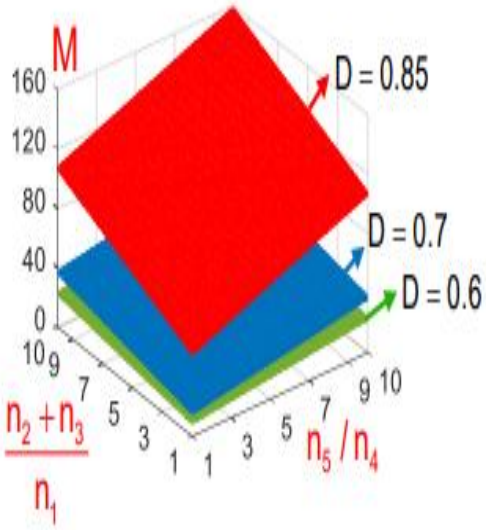


Figure No. 4 - Voltage gain with respect to (n2+n3)/n1 and n5/n4.

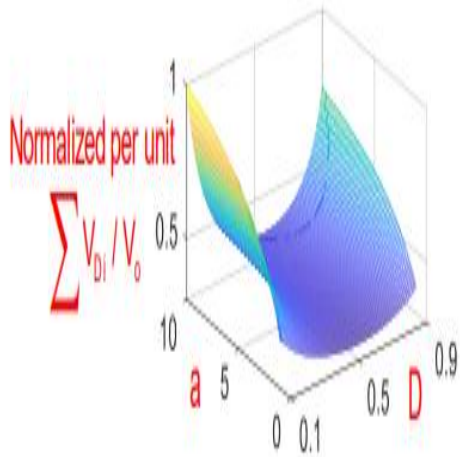


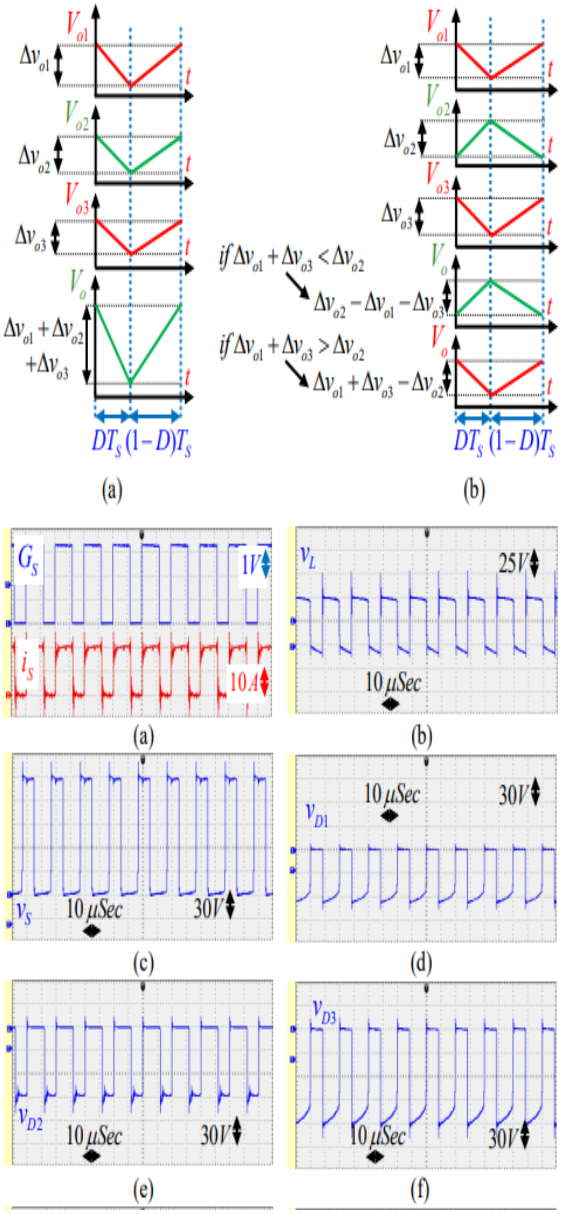
Figure No. 5 - Normalized per unit accumulative diodes voltage stress.

The converter design cannot fulfill all goals and may have some weak points, as well as realizing the power points. In this section, a comparison is made in the design and performance metrics corresponding to the proposed approach against other step-up DC-DC structures, which are based on the coupled inductor and have recently been introduced. A numerical comparison is made available in Table II with respect to the number of components (#S, #D, #L/CI and #C) and VMC utilization. According to Table II, topologies in [1] and the proposed structure possess the least achievable number of switches.

IV. EXPERIMENTAL VALIDATION

A 600 W prototype with a 1.028 W/cm3 power density has been made available to verify the theoretical analytics of the suggested methodology. The switch and diodes for the circuit elements are chosen to be IRFP4868pbf, HER3003PT, and HER3006PT, respectively. To reduce the voltage ripple by 2% in VC, VCo1, VCo2, and VCo3, respectively, one 33µF, one 22µF, and two 6.8µF electrolyte capacitors are selected for C, Co1, Co2, and Co3, based on (3) and (2). In addition, n1=8, n2=16, n3=16, n4=15, and n5=30 is intended for the CIs that have EE55 cores, in that order. The LPC1768 ARM microcontroller is used to control the suggested converter.

The suggested converter's input voltage (Vi) is set to 24 volts, and its output power (Pin) is set to 416 watts in the experiment. Moreover, fs = 50 kHz is the switching frequency. In Fig. 25, the test results are presented. The applied gate pulse of the power switch S is D = 0.6, as shown in Fig. 25(a), leading to a switch current curve with IS = 20A. In Fig. 25(b), vL is shown for this duty cycle. The predicted charge (vL = 24V) and discharge (vL ≈ -36V) values in DTS and (1-D) TS, respectively, are validated by vL in the experimental data.



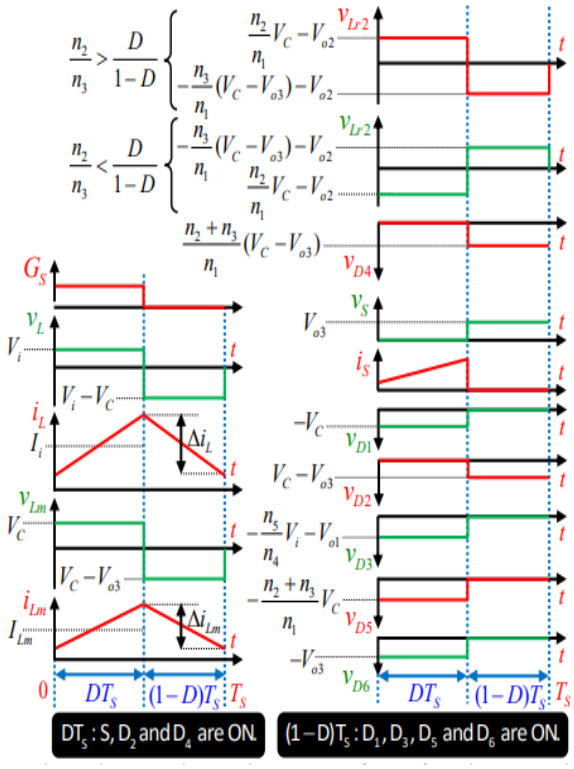


Figure No. 6 – Experimental Results

The approximate voltage stresses of VS ≈ 150V, VD1 ≈ 60V, VD2 = 90V, VD3 ≈ 120V, VD4 ≈ 360V, VD5 ≈ 240V, and VD6 ≈ 150V are detected, supporting (10)-(13), respectively, as seen in the voltage waveforms of the semiconductors. Low-voltage spikes are expressed during the switching transitions by the suggested converter.

Figure No. 7 – Prototype

Thus, in situations where high voltage and high frequency are needed, the suggested form makes sense. The voltages across C, Co1, Co2, and Co3 are shown in Figs. 25(j)–(l), where the actual findings of VC=58V, VCo1=70V, VCo2=140V, and VCo3=147V approximately achieve the theoretical values of VC=60V, VCo1=72V, VCo2=144V, and VCo3=150V. The converter's operation point, as shown in Fig. 15, is situated in the intended ∆vo reduction zone that complies with Figure

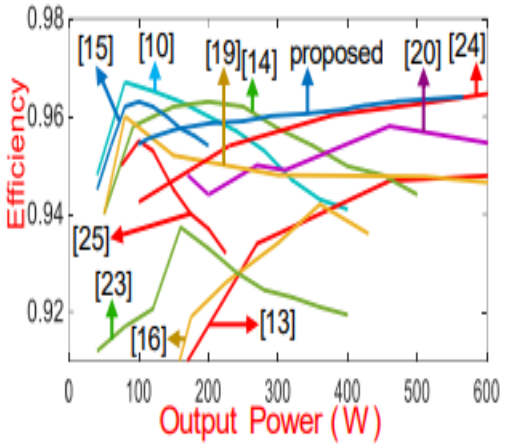


Figure No. 8 – Convertor Efficiency with respect to the Output Power

The prototype is also treated in the discontinuous conduction mode; vL is shown in Fig. 25(m), which supports the theoretical analytics in Figure. Where the load value is raised, the impact of the load step change on the output voltage is finally assessed. Finally, Figure presents a comparison of the efficiency plots and the converter prototype, confirming the reasonable efficiency of the suggested topology.

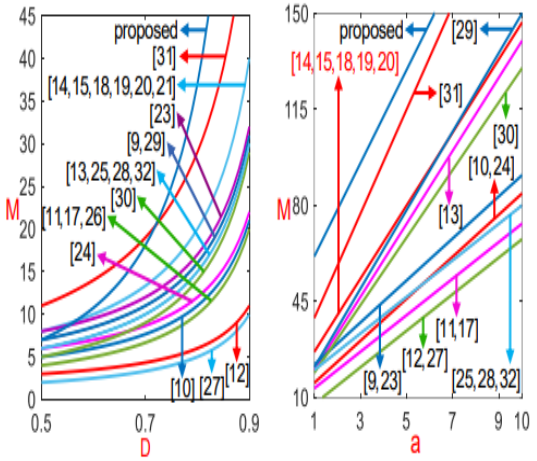


Figure No. 9 – Comparison of the CI-based DC-DC Converters performance in CI turn ratio of 1 and D=0.85

The architectures shown in [9] contain the most passive components, which increases the converter's weight and dimensions, From the inductive point of view, the value of normalized delta Wl in the proposed structure is the highest normalized form has been chosen from comparison. In the meanwhile, the suggested converter's used passive component count is reasonable given the output voltage level it generates. Furthermore, the suggested construction doesn't use any voltage multiplier cells, hence there are no capacitive inrush currents during the voltage multiplier cell switching transitions. Regarding the duty cycle and turn ratio of the linked inductor as the primary duty, the suggested solution provides the maximum voltage gain when compared to comparable works in terms of voltage and energy performance.

V. CONCLUSION

This study has proposed a high step-up DC-DC converter of the latest generation. A 600 W experimental prototype has been used to evaluate and validate the suggested construction. Its main features are as follows: (i) it transfers input power and harvested magnetic energy to the output load using various inductive and capacitive methods; (ii) it achieves a high voltage gain with a lower turns ratio in the coupled inductor; and (iii) it makes use of a straightforward PWM control with a wide duty cycle range. The main characteristics of the suggested method were carefully examined, and their numerical comparison with state-of-the-art structures was done. A thorough design discussion is given to reach the intended operating zone with respect to the semiconductors' power density enhancement, input current and output voltage ripple reduction, and voltage stress reduction. Furthermore, a 600W prototype has been made available to verify the theoretical studies. The suitable efficiency range of 94.7% - 95.8% and the voltage gain of 14.8 are confirmed by the testing findings.

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