*Ms. Sethulakshmi S, et. al. International Journal of Engineering Research and Applications*
*www.ijera.com*
*ISSN: 2248-9622, Vol. 11, Issue 4, (Series-I) April 2021, pp. 48-54*

RESEARCH ARTICLE OPEN ACCESS

# A Novel Reconfigurable Topology for Hybrid Multi Level Inverters

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**ABSTRACT**
Multilevel inverters (MLI) since its initiation have gained the attention of researchers for medium and high power application. However, a topology with a lower number of device count for higher efficiency and reliability has always been necessory. A reconfigurable structure for hybrid MLI is introduced by combining switched-capacitor technique along with conventional hybrid topology in asymmetric mode. The floating capacitors in HBs can be charged by the input voltage source directly or indirectly. Thus, simplified voltage balance controls are achieved which result in simplified modulation. In addition to the merits of conventional topology, reconfigurable hybrid multilevel inverter (RHMLI) is more flexible and can provide wide range of output. All these merits make this topology appropriate for developing a staircase AC output of single phase 7 level, 15 level, 31 level and three phase seven level using minimum switch count, with higher efficiency and lower costs. The simulations of reconfigurable hybrid multilevel inverter integrating switched capacitor techniques are carried out in MATLAB/SIMULINK environment.

**Keywords:** reconfigurable multi-level inverter, switched capacitor, staircase output, asymmetric mode

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Date of Submission: 26-03-2021 Date of Acceptance: 09-04-2021

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## I. INTRODUCTION

In power electronics, multilevel inverters(MLI) always has it's own position as a device which is able to provide desired alternating voltage level at the output using DC source. The introduction of multi level inverters were as a replacement to the convensional two-level inverter used in order to generate the AC voltage from DC voltage. The concept of multilevel inverter (MLI) was mainly focused on overcoming the disadvantages of two- level inverter. It deals with creating a smoother stepped output waveform, more voltage levels are combined together and the output waveform with lower dv/dt and also lower harmonic distortions instead of the two level voltage with large harmonic distortion. The introduction of a series-connected H-bridge, which is also known as cascaded H-bridge (CHB) leads to the multilevel stepped waveform concept resulted in multilevel inverter technology.

Till now so many different multilevel inverter topologies are introduced and many of the researchers are continue to study and research furthermore in this area. Majority of them are mainly focuses on overcoming the limitations that they face today, includes voltage balancing of floating capacitor in MLIs, large device count, increased switching freequency, multiple voltage source requirement etc. On the aim of realizing a higher-quality output with lower total harmonic distortion (THD), while outputing more voltage levels with reduced components and low-voltage devices have been already introduced[1]. It focused on comparing symmetric and asymmetric topologies of hybrid MLI. [2] introduced a DC to AC converter with the ability of voltage increasing. It is designed in a way that just one DC source is used. Also, by using power storage technique and with combining charged capacitors and DC source in series form, output voltage levels can be increased. This inverter is in a modular structure and has the ability of capacitor's voltage self-balancing. But this topology requires large number of capacitors which leads to large power loss. A hybrid seven-level converter based on T-type converter (T2C) and H-bridge (HB) cascaded suitable for low-voltage and high power density application is also there[3]. Two modulation methods, SPWM and SVM, are applied for this topology, aiming at floating capacitor voltage balance. Fundamental switching frequency

modulation is found more convenient to get proper control of multilevel inverter switches to achieve the required output. This can make the system under perfect control and ensures low switching frequency which thereby results in reduced switching loss. [4]suggested that high-frequency inverter serves as source side in high-frequency AC(HFAC) power distribution system(PDS). However, it is complicated to obtain a high-frequency inverter with simple circuit topology and straightforward modulation. A new variety of asymmetric multilevel inverter configuration for generations of seven levels of output voltage is studied[5]. This multilevel inverter topology is implemented with different pulse width modulation (PWM) techniques, which requires less count of power switches and voltage sources to reduce the complexity of a circuit as compare to other multilevel inverter configurations. After detailed study of all the advancements in multilevel inverter this paper is introduced which deals with a novel reconfigurable topology for multilevel inverters which can overcome many of the drawbacks of convensional multilevel inverters.

Here presents a RHMLI topology which is simply a multi-mode topology. That is, a single inverter structure stands for 4 different inverter topologies giving AC staircase outputs of different step number. This work aims to have nearly sinusoidal output voltage waveforms, output current with reduced harmonics, less stressing of electronic devices leads to decreased voltages, switching losses that are lower than that in conventional inverters, smaller size and lower EMI, all of which make them cheaper, lighter, and compact.

## II. CIRCUIT CONFIGURATION AND SWITCHING STATES

Multilevel inverter provides significant advantages over the typical two-level converters such as improved output waveforms with lower harmonic distortion, lower electromagnetic interference (EMI) and reduced stress across the semiconductor switching devices. A novel reconfigurable hybrid MLI topology integrating switched capacitor technique is discussed below.

### *A. Reconfigurable Hybrid Multi Level Inverter*

A novel reconfigurable hybrid multilevel inverter(RHMLI) is introduced here, which can provide a wide range of outputs by the reconfiguration of a single structure. That is, it can operate in both three phase and single phase mode. In single phase mode of operation itself, the RHMLI can achieve three different kinds of output voltage only by varying it's control strategy. Fig. 1 shows the reconfiqurable structure of switched capacitor multi level inverter (SCMLI) where 4 switches $S_A$, $S_B$, $S_C$ and $S_D$ are added into the conventional structure to achieve different topologies of operation. It is formed by adding the four switch combination into the asymmetric hybrid multi level inverter topology. They are explained below in detail.

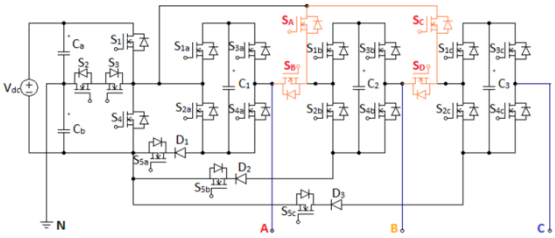

Fig. 1. Reconfigurable Hybrid SCMLI

Basic building block of this RHMLI topology is a single phase hybrid seven level inverter(H7LI) integrating switched capacitor technique shown by Fig. 2. Single phase hybrid seven level inverter is a combination of the T-type converter and an H-bridge. It consist of nine switches $S_1$ to $S_9$, two DC link capacitors $C_a$ and $C_b$, one floating capacitor $C_1$, and a diode $D_1$. $V_{dc}$ is the input DC voltage source and $V_o$ is the AC output voltage. Switching states are explained based on this topology. The basic principle of control strategy of this inverter is fundamental frequency modulation (FFM) which ensures reduced switching frequency and loss.

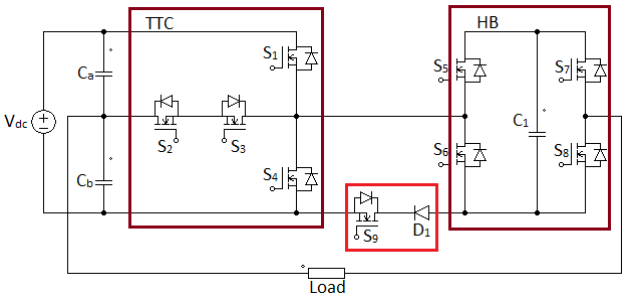


Fig. 2. Single Phase Seven Level Inverter

### *B. Switching States*

For better understanding of the principle of operation of RHMLI, switching state corresponding to each voltage level is analysed for a single phase hybrid seven level inverter integrating switched capacitor technique. The working of the circuit can be explained by 7 states of operation, which are corresponds to the seven voltage levels in one cycle of output. Since for both half cycles the system operates symmetrically, only working corresponds to the positive half cycle voltage levels are explained below. The theoretical waveform of each switching state is shown in following figures.

***Switching State 1 (+3$V_{DC}$/2 )***

In this mode, switch $S_3$, $S_4$, $S_5$ and $S_8$ are turned on while others are in off state. Here capacitors $C_b$ and $C_1$ discharges through the load. At this time, output voltage level of $V_0$ will be +3$V_{DC}$/2. Fig. 3 shows the equivalent circuit diagram with the current path and inverter output voltage level. $S_2$ and $S_3$ are bidirectional switches on the same path, hence the branch will be open until both the switches turned on.

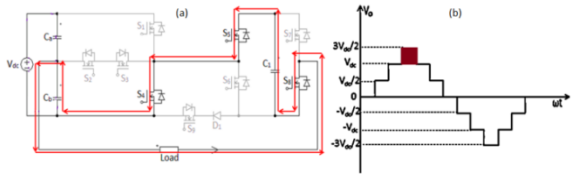

Fig. 3. (a) Operating Circuit of State 1 (b) Inverter Output Voltage Level

***Switching State 2 (+$V_{DC}$ )***

In this mode, switches $S_2$, $S_3$, $S_5$ and $S_8$ are turned on, while $S_4$ turned off. $C_1$ discharges to load to get +$V_{DC}$ output. Fig. 4 shows the equivalent circuit diagram showing current path for this state and corresponding output voltage level is also shown.

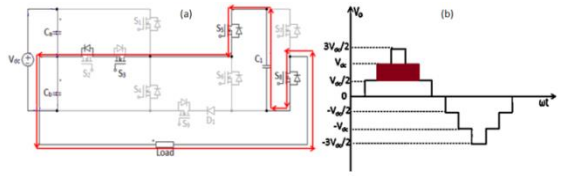

Fig. 4. (a) Operating Circuit of State 2 (b) Inverter Output Voltage Level

***Switching State 3 (+$V_{DC}$/2 )***

In this mode, switches $S_1$, $S_2$, $S_5$, $S_8$ and $S_9$ are turned on, while $S_3$ turned off. $C_b$ discharges to load to get +$V_{DC}$/2 output, while $C_1$ charges from the supply. Fig. 5 shows the voltage level and equivalent circuit diagram and current paths for this switching state is also shown.

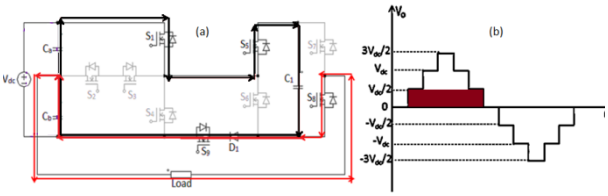

Fig. 5. (a) Operating Circuit of State 3 (b) Inverter Output Voltage Level

***Switching State 4 (0$V_{DC}$)***

In this mode, switches $S_1$, $S_8$ and $S_9$ turned off while $S_3$ and $S_7$ are turned on. This mode short circuites the load to get 0 $V_{DC}$ at the output. Fig. 6 shows the voltage level and equivalent circuit diagram showing current path during this state.

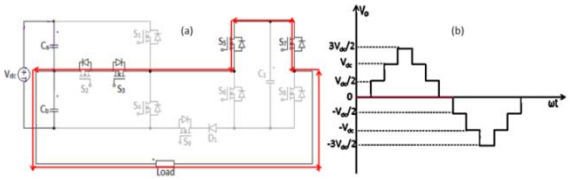

Fig. 6. (a) Operating Circuit of State 4 (b) Inverter Output Voltage Level

Above circuits describe the switching states corresponding to the positive steps of AC output voltage. Switching states corresponding to the negative voltage levels are symmetric to that of positive states.

Table I: Switching States of H7LI

| Levels | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ |
|---|---|---|---|---|---|---|---|---|---|
| +3$V_{DC}$/2 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| +$V_{DC}$ | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| +$V_{DC}$/2 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| -$V_{DC}$/2 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| -$V_{DC}$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| -3$V_{DC}$/2 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

The Table I given above lists the switching states of each of the nine switches of hybrid seven level inverter to achieve 7 voltage steps at the output, where 1s ans 0s represents the switch is turned on and off respectively.

***C. Control Strategy***

The working of the circuit can be controlled by proper control of switching pulses. Here fundamental frequency modulation (FFM) is the control strategy used, which is the simplest modulation technique th

at ensures reduced switching frequency and loss. To easily control a multilevel inverter is to use fundamental frequency switching control where the switching devices generate staircase waveform that tracks a sinusoidal waveform. That is, a modulating sinusoidal signal of 50 Hz(fundamental frequency) is compared with different constant carriers. Control strategy for each of the modes of RHMLI is shown in the following figures. In Fig. 7(a) it shows the FFM for 3 phase H7LI where, amplitude of modulation signal Vpeak is 3 V and constant carriers ± e1 to ± e3 have magnitudes 0.5:1:2.5. Similarly Fig. 7(b), (c) and (d) are FFM corresponds to single phase 7 level, 15 level and 31 level inverter respectively. It is clear from the figure that as the number of output voltage level increases so is the number of carrier. In general, for an N level inverter number of carriers will be N-1.

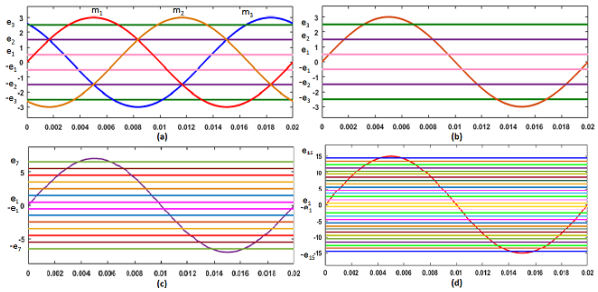

Fig. 7. FFM of SC H7LI

## III. SIMULINK MODEL AND RESULTS

Simulation of RHMLI is carried out using certain parameters and results are varified as follows. With the same structure different topology of operation can be achieved by this RHMLI. They are simulated using MATLAB and results are given as follows. Since each of the topology has different gain, inorder to obtain a fixed output from all the 4 topologies each require different value of input, which requires multiple DC source. Otherwise with a fixed source, voltage can be supplied for all topologies, which results in output with different magnitude and quality. The simulation parameters for different modes of topologies of RHMLI is given in Table II.

Table II: Simulation Parameters

| Parameters | | Specification |
|---|---|---|
| Input Voltage | Topology1 | 210V |
| | Topology2 | 210V |
| | Topology3 | 90V |
| | Topology4 | 46V |
| Auxiliary Capacitor: $C_1$ | | 4400μF |
| Auxiliary Capacitor: $C_2$ | | 8800μF |
| Auxiliary Capacitor: $C_3$ | | 17600μF |
| Input DC Capacitors: $C_a$, $C_b$ | | 2200μF |
| Load Resistance(R) | | 50Ω |

Inorder to obtain an output AC voltage Vo of 220 V rms for a resistive load of 50, the parameters from the table has to be used for the system. The DC link capacitors $C_a$ and $C_b$ have the same rating and floating capacitor will have different ratings according to the step number in the output voltage. The reconfigurable hybrid multi level boost inverter is simulated in MATLAB/SIMULINK by choosing the parameters listed in Table II and the simulink model is shown in Fig. 8.

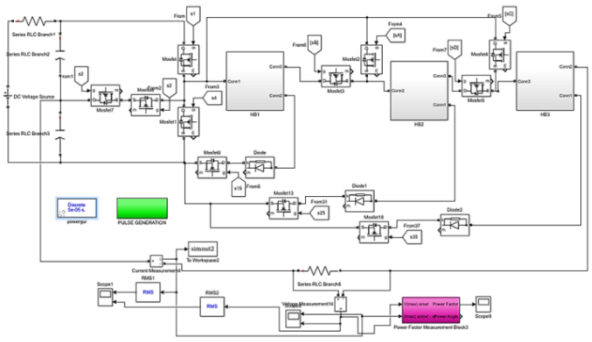

Fig. 8. Simulink Model of Reconfigurable Hybrid MLI

The simulation results of the reconfigurable hybrid multi level inverter are shown in the following figures.

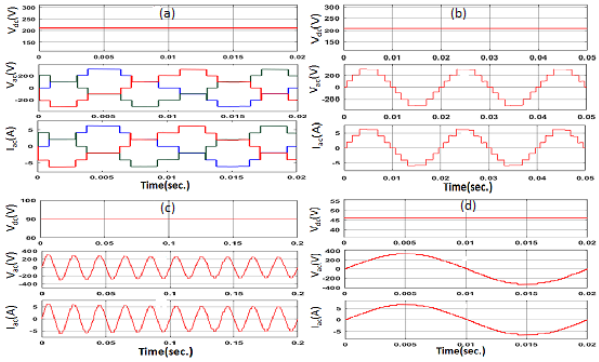

Fig. 9. Simulink Result: (a) 3 Phase 7 Level Input and Output (b) Single Phase 7 Level Input and Output (c) Single Phase 15 Level Input and Output (d) Single Phase 31 Level Input and Output

Fig. 9 shows the DC supply voltage and it's corresponding AC voltage and current output of each of the four topologies of RHMLI. Output voltage and current waveforms are obtained as stepped output. So it doesn't require any additional filter circuits. For an inductive load the output will become smoother and closer to sinusoidal. From the above figure showing the result it is clear that as the step number increases the waveform become more sinusoidal as well as the gain will increased. i.e., for 7 level, 15 level and 31 level the system gain varies as 1.5, 3.5 and 7.5.

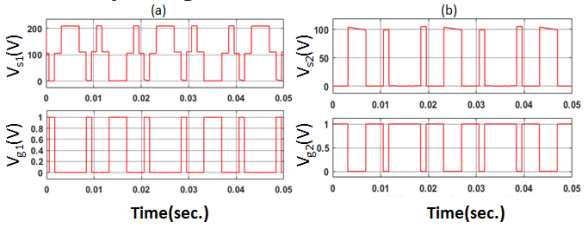

Fig. 10. Simulink Result: (a) Voltage Stress and Gate Pulse to $S_1$ (b) Voltage Stress and Gate Pulse to $S_2$

The basic idea of switching pulses and stress of the RHMLI can be described by considering the single phase hybrid 7 level inverter. Fig. 10 shows the voltage stress across and gate pulse to $S_1$ and $S_2$. $V_{S1}$, i.e., stress across switch $S_1$ will be $V_{DC}$ and $V_{S2}$, stress across switch $S_2$ will be $V_{DC}/2$. From the results shown above it is clear that the average voltage stress across the switches is low.

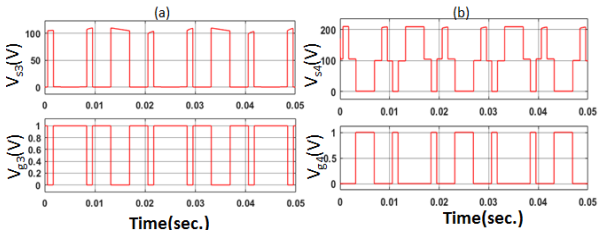


Fig. 11. Simulink Result: (a) Voltage Stress and Gate Pulse to S3 (b) Voltage Stress and Gate Pulse to S4

Fig. 11 shows the voltage stress across and gate pulse to $S_3$ and $S_4$. $V_{S3}$ will be $V_{DC}/2$ and $V_{S4}$ will be $V_{DC}$. Low switching frequency modulation technique is used here which reduces the switching loss. $S_2$ and $S_3$ are bidirectional switches on the same leg whose pulses are complimentary to each other.

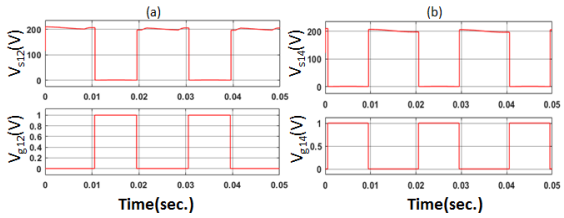


Fig. 12. Simulink Result: (a) Voltage Stress and Gate Pulse to S12 (b) Voltage Stress and Gate Pulse to S14

Figure 12 shows the voltage stress across and gate pulse to switches $S_{12}$ and $S_{14}$. $V_{S12}$ and $V_{S14}$ will be equal to $V_{DC}$. Switches in the same leg will have complimentary pulses. Hence, gate pulse to $S_{11}$ and $S_{13}$, i.e., $V_{g11}$ and $V_{g13}$ will be complimentary to $V_{g12}$ and $V_{g14}$ respectively. Fig. 13 shows the voltage stress across and gate pulse to $S_{15}$. $S_{15}$ is the feedback switch which is a part of switched capacitor, that enables the direct charging of switched capacitor $C_1$ from the DC source in H7LI. After examine the switching stresses across each switches, it can conclude that all the switches of a hybrid MLI, except the bi-directional switches will have a voltage stress eqaul to $V_{DC}$, while bi-directional switches with stress $V_{DC}/2$. This is considered as one of the main advantage of this MLI over other inverters.

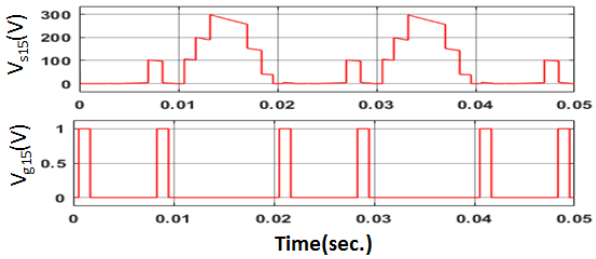


Fig. 13. Simulink Result: Voltage Stress and Gate Pulse to $S_{15}$

## IV. ANALYSIS

The analysis of reconfigurable hybrid multilevel inverter is carrried out by considering parameters like total harmonic distortion (THD), voltage stress and power factor.

### *A. Power Factor Curve*

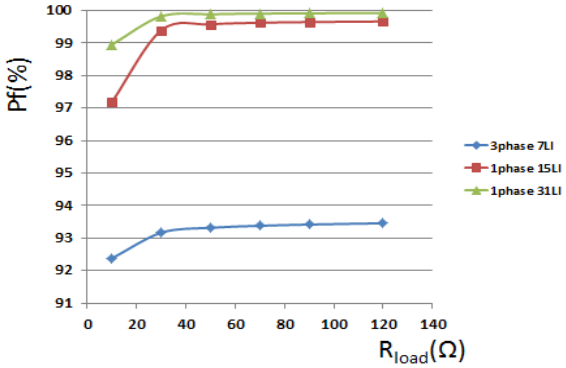


Fig. 14. Power Factor Vs R Load

The term power factor can be defined as the cosine of phase angle between voltage and current. A typical curve for the variation of power factor as a function of load for three phase 7 level, single phase 15 level and 31 level is shown in Fig. 14. Maximum power factor is obtained as 93.46%, 99.67% and 99.92% respectively. From the graph it is clear that, as the output step number increases the waveform becomes more smoother and distortion free which results in improved power factor.

### *B. Voltage Stress Analysis*

The voltage stress experienced by the semiconductor switching devices in the RHMLI corresponds to each of the operating topology is analysed as shown in Fig. 15. The bar graph simply indicates that this system operates with a fixed average switching stress across all the switches except for two bidirecctional switches, i.e., equal to the source voltage, where the bi-directional switches

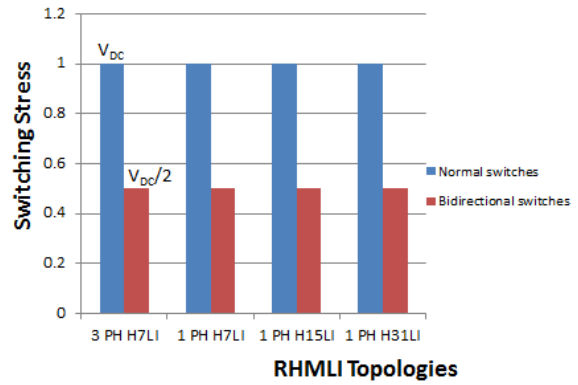


Fig. 15. Power Factor Vs R Load

will experience a stress of half of the source voltage. This can be achieved by the fundamental frequency modulation technique used for developing control pulses.

### *C. FFT Analysis*

The FFT analysis of a RHMLI is shown in Fig. 16. Here shows the FFT analysis of the 31level inverter output alternating current flowing through the load considering 20 cycles of it.

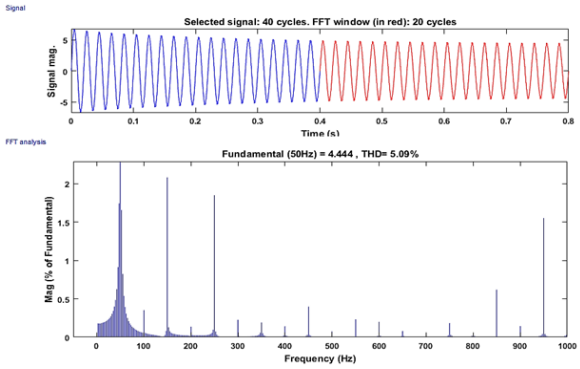


Fig. 16. FFT Analysis

It indicates that by achieving the large step number at the invereter output the total harmonic distortion(THD) can be reduced to a great extend, i.e., 5.09%. Hence this mode of operation of RHMLI can be applicable to high quality AC requirements such as induction motors, heaters, etc.

### *D. Comparison*

Comparison is done between the symmetric, asymmetric hybrid MLIs with typical SCMLIs proposed in [2], [6], [7] [8] and [1] considering all outputing 2m+1 voltage levels, where m is the step number of the staircase output. A comparison about hardware components and the voltage gain is done here. This comparison helps to conclude that the asymmetric MLI topology is the best choice to synthesise a staircase AC output with minimum switch count and lower cost. Reduction in device number also means savings in driving circuits, installation space, and costs.

Table III: Comparison Between Each RHMLI Topologies

| Parameters | Ref[2] | Ref[6] | Ref[7] | Ref[8] | Asymmetric Ref [1] |
|---|---|---|---|---|---|
| Boost gain | m | m | m | m | m/2 |
| Capacitor number | m-1 | m-1 | m-1 | $\log_2^m$ | $\log_2^{(m+1)}+1$ |
| Switch number | 5m-1 | 3m+1 | 2m+3 | $3\log_2^m+3$ | $5\log_2^{(m+1)}-1$ |
| Diode number | m-1 | 0 | m-1 | $\log_2^m$ | $\log_2^{(m+1)}-1$ |
| MPIV(* $V_{step}$) | 1 | m | m | m | (m+1)/2 |

Where m is the step number. For 15 level, m = 7

Table IV shows the comparison of different hybrid multilevel inverter topologies of RHMLI. The comparison is done for a system that outputs an AC rms voltage of 230 V. The relationship between each topology based on hardware setup, gain, distortion, capacitor voltage and switching frequency can be obtained from this.

Table IV: Comparison with Different MLI Topologies

| Parameters | 1ph 7L | 1ph 15L | 1ph 31L | 3ph 7L |
|---|---|---|---|---|
| Input voltage | 210V | 90V | 46V | 210V |
| Boost gain | 1.5 | 3.5 | 7.5 | 1.5 |
| Capacitor number | 3 | 4 | 5 | 5 |
| Switch number | 9 | 16 | 21 | 21 |
| Diode number | 1 | 2 | 3 | 3 |
| Capacitor Voltages | $C_a,C_b=V_{dc}/2$, $C_1=V_{dc}$ | $C_a,C_b=V_{dc}/2$, $C_1=V_{dc}$, $C_2=2V_{dc}$ | $C_a,C_b=V_{dc}/2$ $C_1=V_{dc}$, $C_2=2V_{dc}$, $C_3=4V_{dc}$ | $C_a,C_b=V_{dc}/2$ $C_1,C_2,C_3=V_{dc}$ |
| THD | 12.5% | 6.96% | 5.09% | 12.5% |
| Average switching frequency | 72Hz | 271Hz | 584Hz | 72Hz |

## V. CONCLUSIONS

A novel reconfigurable hybrid multilevel inverter with boosting ability is proposed in this project. The main concept of this topology is the reconfiguraton from one topology to another in simplest manner according to it's application, which helps to improve the efficiency, reduces volume and enhances reliability of the system. Also it can have grid connected as well as islanded mode of operation. This RHMLI mainly aims to provide a high quality AC with reduced harmonics and loss. By analysing the system for a fixed load, maximum power factor of 3 phase 7 level, single phase 7, 15 and 31 levels are 93.46%, 98.5%, 99.67% and 99.92% respectively and corresponding THDs are 12.50%, 12.50%, 8.60%, and 5.09% respectively. The proposed novel reconfigurable hybrid MLI can be used for applications with medium voltage and high power, such as PV system, HVDC ststem, electric power conversion system (EPCS), fault tolerence of EPCS, grid tied networks etc.

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