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Continuous-Time Analog Filter based on a Programmable CMOS Current Cell

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ABSTRACT
This work presents an active filter design using a programmable basic cell. In contrast to traditional design techniques, the cell allows to the designer to configure it to build gain stages and circuits emulating resistors. The proposed cell is a PPN current branch, where the sizing of transistors is done by using the Ohm's law and needed node voltages given by the designer. The cell's sizing warranty why, when designing a circuit based on the cell, the connection of them do not alter the operation point of the circuit. SPICE simulations show the usefulness of the cell to design analog integrated circuits. As an example, a single-ended Sallen-&-Key 2nd order band-pass filter is designed and analyzed. The active filter is designed in a standard 0.5μm, ±2.5V CMOS technology. The expected performance of the filter shows the relevance of the circuit analysis based on a design method, and supported on physical principles.

Keywords **–** Active filters, analog integrated circuits, circuit analysis, MOSFET circuits, Ohm's law

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I. INTRODUCTION

A programmable/tuned resistor is not a new idea. It has been proposed as a bank of passive/active resistors, where its programming allows obtaining a series, parallel, or series-parallel array according to the required resistive value [1]-[6]. Although the concept is useful for making analog design, those proposals have several disadvantages where some of them are just model a resistor, or alternatively the proposal based on floating gates are viable in not standard manufacturing processes. The passive resistor, on the one hand, in addition to being integrated in silicon and requiring a large area, is a network element that is also a source of thermal noise. Not to mention that when the resistor is made of polysilicon, its performance is equivalent to a transmission line and it is a source of thermal noise as well. The active resistor, on the other hand, is also a source of noise, but does not require a large integration area. Although the MOS transistor is an option for developing a resistor, it is also true that its useful frequency range is only limited by parasitic capacitances. Therefore, if the transistor is of minimum size the frequency range increases. Now, in MOS technology it is recommended to use a PMOS transistor because its noise spectral power is less than the power generated by an NMOS transistor. In this way, the basic cell proposed is made up of three transistors, two PMOS and one NMOS, generically called the PPN current branch. In addition, from the point of view of circuit design, the basic cell has the characteristics to configure it by itself as an active resistor, or as a single-ended amplifier, i.e. an inverting amplifier or an inverting amplifier with source degeneration. These properties of the cell are used as an example to show the design of a filter network, completely integrated in silicon, where its design consists of using replicas of the basic cell. This fact does not alter the operating point when connecting cells, and each cell is just configured to perform a single function. The reader may conclude that the cell facilitates the design of other circuits such as a voltage follower, a cascode amplifier, and the design of differential circuits is immediate. However, it should be noted that a deficiency of this proposal is the reduced number of circuits that can be designed, that is, the development of circuits is limited by the number of transistors in the basic cell.

This paper is organized as follows. Section II presents the basic characteristics of the programmable CMOS basic cell, which uses MOS transistors in strong inversion and operating in saturation region. The small-signal parameters are obtained from LEVEL=49 SPICE simulations. The data set, obtained from a design of experiments, has a twofold purpose: 1) to show the sizing tiny effect on the operation point variability, 2) how the designer must take advantage of the V_{SB} voltage in order to simplify his/her design method. The same section shows how to get grounded resistors and what conditions must met the cell to obtain a

floating resistor. As an extension of the cell's characteristics, it is shown how to configure it to obtain inverting amplifiers. Some Continuous Time (CT) analog circuits are presented and analyzed in section III, where a 2nd order active filter is designed by integrating those CT circuits. The filter design is used to show its programmability, and to highline the usefulness of the proposed design cell as well. For illustrative purposes, the MOS transistor model of a 0.5μm standard process, N-well, ±2.5V, was used, while Tanner Tools was our choice for doing the SPICE simulation at room temperature. At the end of the paper, both discussion of results and conclusions of this work are given.

II. PROBLEM DEFINITION

The design of analog circuits, in addition to satisfying the requirements of the various applications, must meet the regulations of the consumer market. At present, minimum weight, small size and optimization of power consumption are some design constrains that define the designer's design space, where he/she actually has few degrees of freedom. The designer, in that scenario, can meet some of those specifications but not all in reality. However, and although manufacturing technologies have been developed to integrate more and more digital solutions, there are mixed-mode circuits that cannot be omitted because they are the link between analog and digital processing. Therefore, the first design consideration is to satisfy the bandwidth that the application requires, and those are understood as time constants defining poles/zeros (in the frequency domain) and that involve two basic design components, capacitors and resistors. Some of those are intrinsic to the circuit under design, but may still be under the designer's control. In addition, the most complicated to develop, due to its various non-idealities, is the resistor. Since several decades ago, polysilicon resistor have been used as load resistors in static RAM cells, as a resistor with irreversible resistance transition as memory element, and as the gate electrodes in CMOS integrated circuits [1]. These examples show different levels of doping depending on the resistor application. However, although doping can be controlled, polysilicon films are the top plate of a parasitic capacitor, which conditions its use in a limited range of frequencies. Another disadvantage of the passive resistor is the integration area, which grows for large resistance values. On the other hand, the MOS transistor operating in strong inversion in the triode region has been used as a resistor, and it has been incorporated into circuits requiring programmability. In practice, a drawback of this proposal is that the resistor has a moderate linearity. Some proposals to improve linearity is using quasi-floating gate transistors [7], where some very high resistance components are implemented with transistors biased in sub-threshold. Another design option to improve resistor linearity is to use transistors in strong inversion in saturation. Moreover, although some harmonic components affect linearity, the design of differential circuits has been proposed to cancel even harmonics [6]. Unfortunately, this solution, in addition to the integration area, consume more power. One more differential proposal uses a voltage-controlled resistor, which is a voltage-to-current converter, and where linearity depends on a transistor operating in the triode region and on the exact value of the threshold voltage, V_{TH} [4]. In other proposals, the resistance value is tuned with a Phase Locked Loop [8] or using both Fowler-Nordheim tunneling and hot electron injection techniques [9]. For all the above, in this work, alternatively, it is proposed to use a basic design cell, with polarized transistors in strong inversion in saturation, which in addition to offer resistance properties it can also be programmed to offer other properties such as signal amplification (single-ended and differential amplifiers), or impedance coupling (source follower circuits), etc. In this way, the use of the basic cell allows the designer to build continuous time systems of greater complexity.

2.1 Basic design Cell characteristics

The proposed basic cell is a PPN current branch, where the sizing of each transistor is done by using the Ohm's law and knowing the reference voltages ($V_{REF,1}$ and $V_{REF,2}$) given by the designer (see Figure 1a). The sizing of the basic cell is obtained from the relation $W_{p2}=\alpha W_{n3}$, $W_{p2}=W_{p1}$, where α (= 36.0844) depends on both the bias conditions and few parameters of the CMOS technology [10]; the W_{n3} channel width is a design variable under the designer's control. Table I shows the sizing of the channel width $W_{p2}=W_{p1}$ for different values of W_{n3}; for all transistors the channel length is L=1.5μm. The expected value for $V_{REF,1}$ and $V_{REF,2}$ is 1.25V and 0.0V, respectively, while results from SPICE simulation, LEVEL=49, were 1.1959V and -108.71mV, respectively. In practice, because the design method is based on equations LEVEL=1, the sizing has an implicit error at the point of operation, but transistors still operate in saturation. It must be noted that sizing of transistors grows (see Table I) as the operation point moves away from the desired value; this variation does not modify the expected operation of all transistors. So, in the space of the design variables, all about the Design of Experiments (DE) is in a plane (x_i-W_{n3}) located at g_m/I_D (=0.9471), where x_i means each characteristics of the PPN circuit under analysis, i.e. gain,

bandwidth, power consumption, harmonic distortion, active resistance and so on (see Figure 1b).

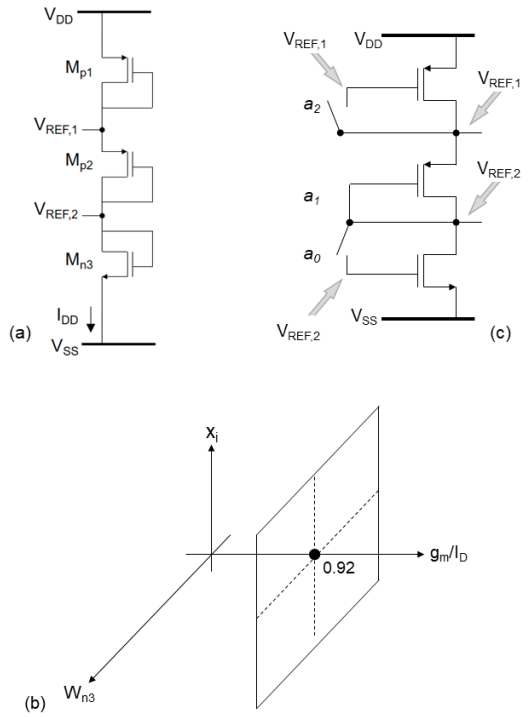

Figure 1. Basic cell (a), performance plane in the design variables space (b), programmable cell (c).

The last nine lines in Table I correspond to the small signal parameters for each transistor obtained from SPICE simulations, and the first three lines are analytical results obtained from design equations. The PPN basic cell includes for illustrative purposes three digital inputs (a2, a1 and a0) to control the connection of the transistor gate to its drain terminal (*VGD*=0) or at the corresponding reference voltage where also *VGD*=0 (see Figure 1c). Depending on each digital input, is the particular resistance value, where the small-signal resistance is actually the output impedance *Zin* seen from the *VREF,2* node to ground. Once the small-signal equivalent circuit is analyzed, eight different resistance values are obtained. In all small-signal analysis, transistors satisfy the condition V_{SB}=0 because each PMOS is manufactured in its own well. This fact favors that the transistor is on with the minimum threshold voltage.

TABLE I: Simulation values, where L=1.5µm

	1	**2**	**3**	**4**
W_{n3}	3,00µm	6,00µm	7,50µm	9,00µm
W_{p2}	104µm	209µm	259µm	311,4µm
W_{p1}	104µm	209µm	259µm	311,4µm
$V_{REF,1}$	1,22V	1,20V	1,19V	1,185V
$V_{REF,2}$	-60,6mV	-106mV	-118mV	-130mV
I_{DD}	182µA	410µA	525µA	621,6µS
g_{mn3}	180µS	370µS	475µS	10,19µS
$g_{ds,n3}$	2,81µS	6,43µS	8,29µS	2,86mS
g_{mp2}	843µS	2,00mS	2,49mS	308,88µS
$g_{ds,p2}$	9,16µS	20,6µS	26,4µS	2,86mS
g_{mp1}	843µS	2,00mS	2,49mS	30,89µS
$g_{ds,p1}$	9,16µS	20,6µS	26,4µS	9,00µm

2.2 Grounded resistor

Figure 2 shows the eight different arrangements to obtain the same number of grounded resistors, where v_t is a test voltage source and *it* is the small-signal current. Note that the $V_{REF,2}$=0 requirement was not a random value, but rather considering that this would be the output node in small signal analysis. Note also that the transistors are either biased in diode configuration or biased from the voltage divider, in both cases the condition V_{GD}=0 is satisfied. To analyze the performance of the basic cell, the transistor´s equivalent electrical model (LEVEL=1) based on the square law was considered [11]-[15]. For low frequency analysis, parasitic capacitances are assumed open circuits. Note that each transistor satisfies the condition $g_m >> g_{ds}$ (see Table 1) and consequently, the function of each transistor is different depending on the network under analysis. This characteristic is highlighted with symbol **1** and **0**, where **1** represents a transistor in diode configuration, and **0** is an open-loop transistor. It is easy to conclude that solving the network 111 we have a general transfer function, which can be simplified for each of the remaining configurations as eq. (1) shows, here superscript *x* means that this transconductance contributes to the transfer function if and only if it is a diode-connected transistor. For example, when configuration is 000, those parameters (with superscript x) do not contribute and the result simplifies to (5), and it can be verified that *Zout,000*≈1/*gds,n3*. This result allows us to observe that depending on the dimensioning of the basic cell (see Table I) will be the resistance value. Then, with the help of (1), and substituting the small signal values, the resistance can be calculated for each cell configuration.

$$Z_{out} = \frac{\frac{d_x}{c_x g_{ds,p2}}}{\left(d_x - 1 - \frac{g_{mp2}}{g_{ds,p2}}\right) + \frac{b_x g_{ds,n3}}{c_x g_{ds,p2}} d_x} \quad (1)$$

$$d_x = 2 + \frac{g^x_{mp1} + g_{mp2}}{g_{ds,p1}} \quad (2)$$

$$c_x = \frac{g^x_{mp2}}{g_{ds,p1}} + 1 \quad (3)$$

$$b_x = \frac{g^x_{mn3}}{g_{ds,n3}} + 1 \quad (4)$$

$$Z_{out,000} = \frac{2 + \frac{g_{mp2}}{g_{ds,p1}}}{g_{ds,p2} + g_{ds,n3}\left(2 + \frac{g_{mp2}}{g_{ds,p1}}\right)} \quad (5)$$

Figure 3 shows –for each of the possible configurations– the resistive value obtained for two different channel length L values (1.5µm→dark color, 2.1µm→light color); the sizing of the transistors corresponds to experiment 1 (see Table I). As expected, the higher the value of L the higher the value of resistance. The bias current for both designs was 184µA and 132µA, respectively. Furthermore, to perform the analysis at moderate frequencies, we must include the effect of the transistor capacitances. With the sizing of transistors (see Table I) and using parameters of the technology, the values of C_{gd} and C_{gs} are calculated [13], [16], [17]:

$$C_{gs,j} = \frac{2}{3} W_j L C_{ox} + W_j C_{gs,ov} \quad (6)$$

where j=1,2, 3

$$C_{gd,j} = W_j C_{gd,ov} \quad (7)$$

and C_{ox} is the oxide capacitance, and the overlap capacitances are $C_{gs,ov}$ and $C_{gd,ov}$ in the source and drain regions, respectively. The values of those parameters are in the spice simulation model. Note that by substituting the known values, in (3) and (4), the value of each parasitic capacitance for each terminal, of each transistor, is obtained (see Table 2).

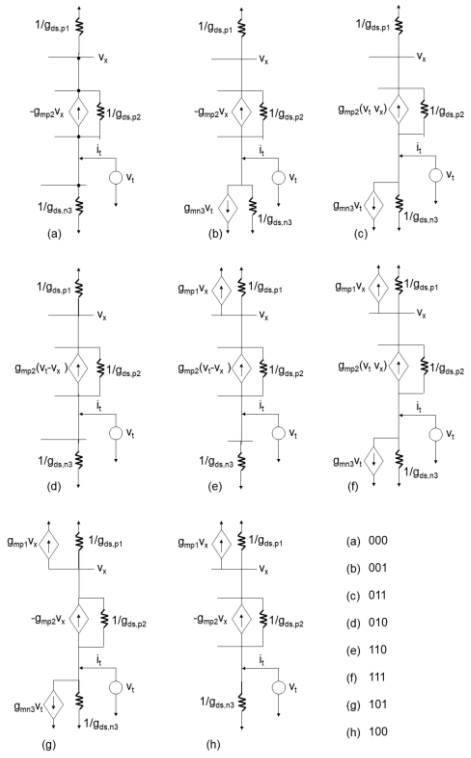

Figure 2. Low-frequency equivalent circuits for obtaining the output impedance.

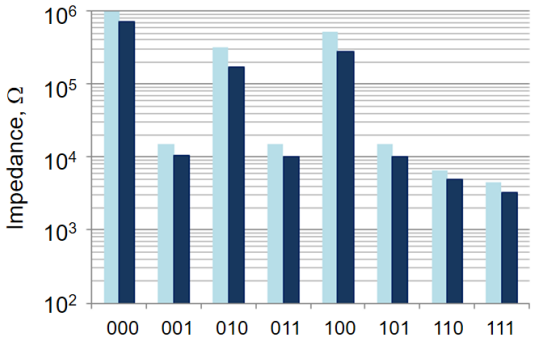

Figure 3. Low-frequency output impedance according to the cell programming.

Capacitances can be included in the equivalent circuits as Figure 2 shows, and the bandwidth can be determined. As an example, Figure 4 shows the equivalent circuit for the impedance $Z_{out,000}$, and its Bode plot as well. This result corresponds to the cell design with the lowest sizing (see Table I), where L=1.5µm and C_L=1.0pF.

TABLE II: Parasitic capacitances, $C_{gd,p2}$=$C_{gd,p1}$ and $C_{gs,p2}$=$C_{gs,p1}$.

	1	2	3	4
$C_{qd,p2}$	20,80fF	43,200fF	51,900fF	62,100fF
$C_{qs,p2}$	218,4fF	453,60fF	544,95fF	652,05fF
$C_{qd,n3}$	0,6000fF	1,2000fF	1,5000fF	1,8000fF
$C_{qs,n3}$	6,300fF	12,600fF	15,750fF	18,900fF

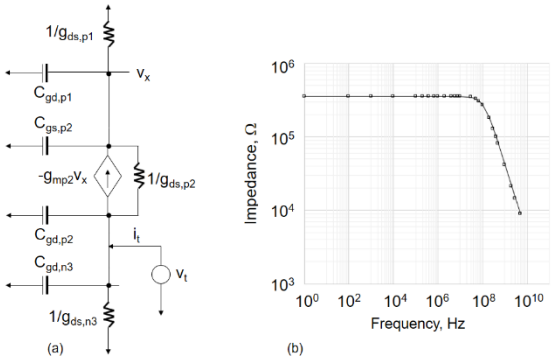

Figure 4. LEVEL=1 equivalent circuits for the 000 configuration (a), and frequency response (b).

2.3 Floating resistor

A floating resistor takes advantage of the MOS transistor's properties in saturation, where $g_m >> g_{ds}$. Figure 5a shows the equivalent circuit for the configuration 010, where $r_p \approx 1/g_{dsp}$, $R_p = 1/g_{mp}$ and $r_n = 1/g_{dsn}$. In this configuration, an input current i_{in} is expected to flow through R_p, so that the contribution by the equivalent resistors r_p and r_n is ideally zero (see Figure 5b). Furthermore, if a capacitor C_L were connected in series with the resistor R_p, the impedance seen from the input node would be expected to be $Z_{in} = R_p + (sC_L)^{-1}$. However, analyzing the equivalent circuit (see Figure 5b), it is easy to verify that the impedance is given by

$$Z_{in}(s) \approx \frac{\frac{1}{g_{mp}}}{1 - \frac{\left(1 + \frac{g_{dsp}}{g_{mp}}\right)^2}{1 + 2\frac{g_{dsp}}{g_{mp}} + s\frac{C_L}{g_{mp}}}} \qquad (8)$$

and analyzing this result, it can be concluded that indeed the resistance is dominated by $1/g_{mp}$. Note that the output voltage is a low-pass response, where the bandwidth is limited by the time constant $\tau_0 = C_L/g_{mp}$. From the point of view of the basic cell bias, note the values of the reference voltages. In other words, in analog signal processing it is very important that both input and output signals are on equivalent DC potentials. To achieve this purpose, two basic cells are used, connecting both nodes $V_{REF,2}$, so that the equivalent resistor is $R_{eq} = 2R_p$ (see Figure 6a) and the newest time constant is $\tau_0 = 2C_L/g_{mp}$. Because the cells are replicas, one of the other, the operation point is preserved. This solution increases in fact the power consumption, but the excursion of the response is now symmetrical. In practice, this implementation requires three basic cells, where $P_{DC} = 6I_{DD}V_{DD}$. The same figure shows the Tspice simulation result, and the $V_{REF,1}$ and $V_{REF,2}$ values obtained from the simulator have been included as well. This result, at room temperature, corresponds to the basic-cell sizing with $W_{n3} = 6.0\mu m$ (see Table I). Note that if another basic cell sizing is used, the variant will be the equivalent resistance value, and the parasitic capacitances will increase.

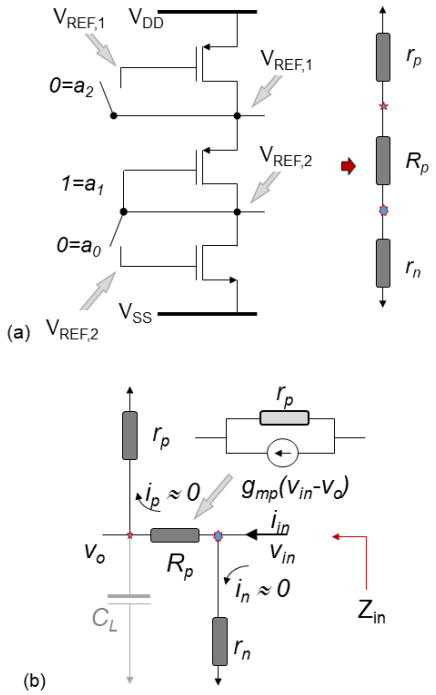

Figure 5. Floating resistor (a) and small-signal equivalent circuit (b).

III. RESULTS

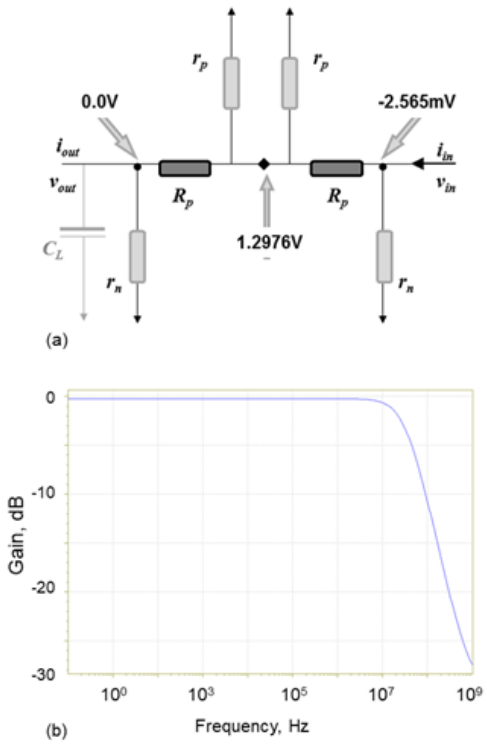

Figure 6. Enhanced floating resistor (a) and Tspice simulation result (b).

With the previous results, a second order filtering system is designed. Figure 7a shows the active circuit, where two floating resistors and two capacitors define a low-pass characteristic. It can be shown that if g_{ds}/g_m <<1, the transfer function is given by (9), where where $R=R_1=R_3$ and $C=C_2=C_4$ [18]. To synthesize a Butterworth approximation, the gain must be k=1.586; by using that gain value the response of the network was obtained as shown in Figure 7b; the dimensioning of the PPN network is that of W_n=3.0μm. In this example f_{-3dB}=45.38MHz and C=5.0pF.

$$\frac{V_o(s)}{V_{in}(s)} = \frac{\frac{k}{R^2C^2}}{s^2 + s\frac{3-k}{RC} + \frac{1}{R^2C^2}} \tag{9}$$

Note that the value of $R=1/g_{mp2}$ controls the cutoff frequency. For example, if a lower cut-off frequency is desired, the value of L can be increased, which also reduces current consumption. For a higher cutoff frequency, the suggestion is to change the value of C. On the other hand, it is important to comment on the design of the non-inverting amplifier.

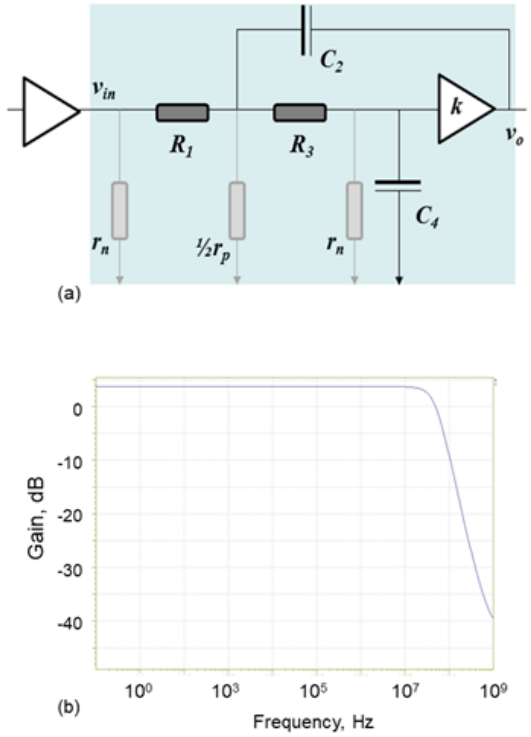

Figure 7. Sallen-and-Key 2nd order low-pass filter (a) and Tspice simulation result (b).

Figure 9a shows the amplification options offered by the basic cell. Each configuration is an amplifier with source degeneration, and they can all be grouped into a single circuit (see Figure 9b). By substituting the Mp2 transistor with its small-signal circuit, it is easy to demonstrate that the transfer function is given by

$$\frac{v_{out}}{v_{in}} \approx \frac{-\frac{g_{mp2}}{R_{p1}}}{\left(\frac{1}{R_{p1}} + g_{mp2}\right)\left(\frac{1}{R_{n3}} + g_{ds,p2}\right)} \tag{10}$$

where the highest and lowest amplification is provided by configurations 1$\underline{0}$0 and 0$\underline{0}$1, respectively, and $\underline{0}$ means that the Mp2 transistor is the one that receives the input signal. By connecting both amplification cells, a non-inverting amplifier with gain k=2.77 is obtained. Although it is not the desired value, it does allow a quasi-Butterworth design. This gain corresponds to the basic-cell sizing with W_{n3}=7.5um. Finally, the simplicity offered by the basic-cell to build circuits should be highlighted. The filtering system consists of five basic-cells, two to implement the floating resistors, two for the non-inverting amplifier, and one more cell to generate the reference voltages. All cells, preserving the initial operating point, provide symmetry in the response because the input and output nodes have equal value in DC. This design option, actually simple, favors that its performance depends only on the characteristics of the basic cell. Moreover, the system under design, make up of basic cells, only other network elements (such as capacitors) are added to define its processing function. Unlike other design options, where the resistance values depend on various design parameters [20], using the basic cell only requires determining its size to know its properties, such as those shown in Table 1 and in Figure 3.

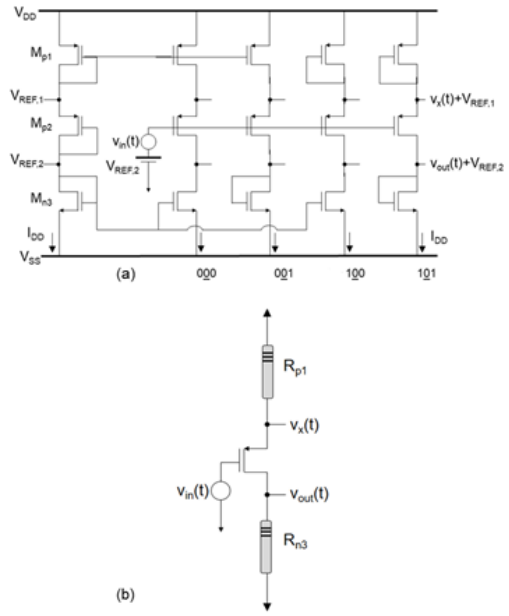

Figure 8. Amplifier with source degeneration (a) and compact model for small-signal analysis (b).

IV. CONCLUSIONS

Analog design, in the strict sense of the word, is putting into practice a method, a design method. In this contribution, the method is based on a basic-cell, which is composed of three transistors and designed according to the Resistive Approach [10], [19]. The advantage of the proposed method is that very analog design uses copies of the basic-cell, so that their connection does not modify the operation point. The proposed method is a particular case of g_m/I_D, not only because the operation of the transistors is in saturation and in strong inversion, but also because the design of experiments is oriented to the analysis of a basic-cell and not to the transistor. From the point of view of its usefulness as a design method, there is no doubt that it works. Although the example is limited to a filtering system, it should be noted that the configuration of the cell allows the development of other applications, with higher performance, and with differential characteristics. For now, these examples serve to use a design technique rather than trial-and-error practices. Therefore, the design method allows implementing resistors of different values, in different configurations, and in circuits where their use does not add complexity to the circuits under design. The control on the resistance value depends not only on the sizing of the cell, but also on the value of the channel length. These characteristics of the proposed design are at all times under the designer's control. Finally, it should be noted, that the capacitors in this contribution are poly-poly. The unitary capacitor C_u, with a value of 0.254pF [21], has a capacitive performance up to 700MHz, a frequency at which parasitic effects appear. The C_u capacitor has an area of 22.2μm×22.2μm and was manufactured in a standard CMOS 0.5μm process, N-well, ±2.5V. Therefore, the designs proposed in this contribution and others that may be of interest, if they require capacitive elements, all development will be for applications no higher than 700MHz.

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