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A Brief Review on Types and Design Methods of ADC

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ABSTRACT: Analog to digital converter ia an essential functional block in many system-on-chips (SOC). Through this paper, a brief report is presented giving an overview of the available ADCs. Input to any processor or a controller has to be in the digital format, hence there is a need for an efficient data converter which can converts analog signal into digital form. The working principle of different ADCs is described here. ADC's can be chosen based on type of applications, required accuracy and number of bits that are required in the system. An overview about performance metrics and its effect is also discussed in this paper
Keywords: ADC, SNR, SNDR, SAR, resolution.

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I. INTRODUCTION

An Analog to Digital Converter (ADC) is a Process which converts analog voltage signal into digital signal form. Practically most of the data is characterized using analog signals but the input to different processors cannot be an analog signal hence it needs to be converted into digital signals, so that processors will be able to read, understand and manipulate the data.

The first process in conversion involves quantization of the input, instead of continuously performing the conversion, an ADC does the conversion periodically, by sampling the input. The main function of this converter is to convert a sequence of digital value i.e converting a continuous time domain analog signal to a discrete amplitude digital signal.

II. DIFFERENT TYPES OF ADC ARCHITECTURES

Based on speed, Performance, dynamic range, different applications along with their interfaces and degrees of accuracy ADC's are classified into various types based on Nyquist rate and oversampling mechanism. The most common types of ADCs are:

1]FlashADC2] Two step Flash ADC
3] Pipeline ADC
4] Successive approximation ADC
5] sigma-delta ADC
6] Oversampling ADC
7] Time- Interleaved ADC
8] Integrating ADC

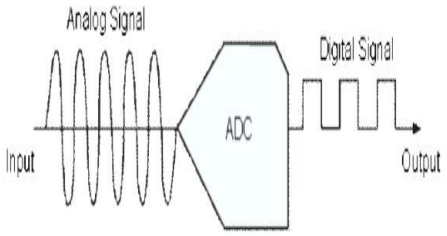

Fig 1: Analog to Digital Converter

An ADC samples an analog signal at uniform time intervals and assigns a digital value to each sample. The digital value appears on the converter's output in a binary coded format. The value is obtained by dividing the sampled analog input voltage by the reference voltage and them multiplying by the number of digital codes. The resolution of converter is set by the number of binary bits in the output code

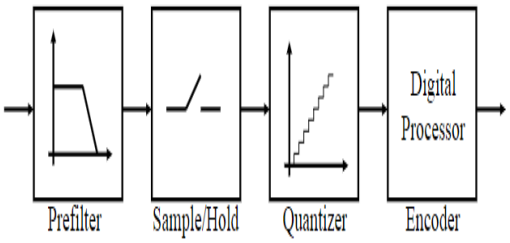

Fig 2: Working principle of an ADC.

The above fig 2 shows the block diagram of Analog to digital converter. The above figure consist of prefilter, Sample/hold circuit, quantizer and encoder block. The prefilter block filters(removes) unwanted input frequencies from the analog signal

using binary search logic, then the filtered signal is sent to the sample/hold logic where the analog signal is sampled. Later the signal is quantized in quantizer block and finally the quantized signal is sent to encoder where the signal is processed in digital form and the digital output is obtained.

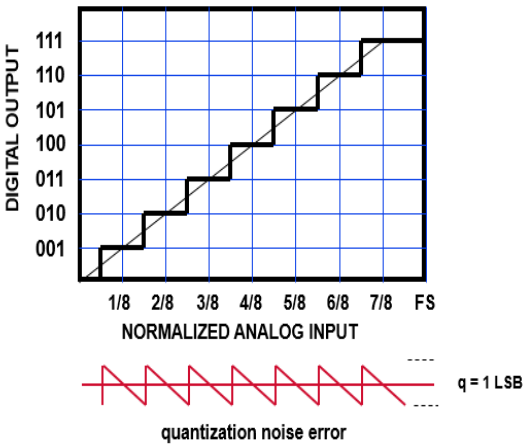

Fig 3: Quantization Process and quantization error.

The representation of an analog signal in an ADC with an infinite resolution is converted and represented in the form of digital code with finite resolution [8]. The ADC produces 2^N digital values where N represents the number of binary output bits. Fig 3 above shows the quantization process of an analog signal. The analog input signal will fall between the quantization levels because the converter has finite resolution resulting in uncertainty or quantization error. That error determines the maximum dynamic range of the converter.

The sampling process represents a continuous time domain signal with values measured at discrete and uniform time intervals [1]. This process determines the maximum bandwidth of the sampled signal in accordance with the Nyquist Theory. Nyquist theory states that the signal frequency must be less than or equal to one half the sampling frequency to prevent aliasing.

Quantization process is representation of an analog signal having infinite resolution with a digital signal having finite resolution. It assigns binary code to sampled and hold value, range and granularity. This process even helps to achieve maximum dynamic range. This process of quantization encounters quantization error or quantization noise.

The two main performance metrics considered in this conversion are static (DC specification) and dynamic (AC specification). These are further classified as static- monotonicity, offset error, gain error, differential non-linearity (DNL), Integral non-linearity (INL) and dynamic- Delay setting time, signal to noise ratio (SNR). Signal to noise + distortion ratio (SNDR), spurious-free dynamic range (SFDR).Each of the above parameters are explained in detail. Monotonicity in an ADC is that if the input in analog form and output in digital form either increase or decrease or stay in the same state. Non-monotonic behavior of ADC results in oscillations [2].Offset error is defined as the deviation from the code transition points which is present across various output codes [2].This function either shifts the entire code towards right or towards left. Gain error is defined as the deviation from the ideal slope of ADC transfer function curve [4]. This is determined by the location of last transition code and then comparing with the ideal case. DNLit is defined as the difference between the actual increment height of transition n and the ideal increment height. INLat any point is defined as the difference between the output values for input code n to the output value of the reference line at that point [7].

Delay setting time is defined as the time taken by an output to reach the final value with desired accuracy in application of a step input. SNR is defined as the ratio of signal power to that of the noise power[7]. Theoretically the maximum SNR of an ADC is given as

SNR = 6.02 N + 1.76 (dB) -- (1)

where N is the resolution of the converter.

SFDR is defined as the ratio of signal power to that of the largest magnitude of any spectral component. A spectral component can be a harmonic of an input signal.

$$SFDR = \frac{P_s}{\max(P_{spectrum}(f))},\ f \in \{1,\ldots, Fs/2\}\backslash\{fin\} \quad -- (2)$$

$P_{spectrum}(f)$ is the spectral component excluding the DC Component.

SNDR is a parameter which completely indicates overall dynamic performance of the converter. This is completely a combination of various performance degradation elements.

$$SNDR = \frac{Ps}{\sum_{i=2}^{h} P_H(i) + P_j + P_{q+DNL} + P_{th}} = 10^{\frac{THD}{10}} + 10^{\frac{-SNR}{10}} \quad -- (3)$$

P_j, P_{q+DNL}, P_H and P_{th} are the jitter, quantization plus DNL, harmonics and thermal noise power respectively.

The two main parameters that affects the behavior of an ADC is its bandwidth and signal-to-noise ratio. The bandwidth of an ADC is characterized primarily by its sampling rate. ADCs are chosen to match the bandwidth and required signal-to-noise ratio of the signal that needs to be quantized [10]. If an ADC operates at a sampling rate greater than twice its bandwidth of the signal, then perfect reconstruction is possible given an ideal ADC and neglecting quantization error. The presence of quantization error limits the dynamic range of even an ideal ADC. However, if the dynamic range of the ADC exceeds that of the input signal, effects may be

neglected resulting in an essentially perfect digital representation of the input signal.

Different types of ADC's mentioned above are described in detail along with its advantages and disadvantages below.

1] Flash ADC:

The flash ADC is the fastest type available. It has the highest speed compared to any other types of ADC. One comparator per quantization level (2^N - 1) and 2^N resistors. Reference voltage is divided into 2^N values. A flash ADC uses comparators, one per voltage step, and a string of resistors. A 4-bit ADC will have 16 comparators, an 8-bit ADC will have 256 comparators. All of the comparator outputs connect to a block of logic that determines the output based on which comparators are low and which are high. The comparator array outputs a thermometer code.

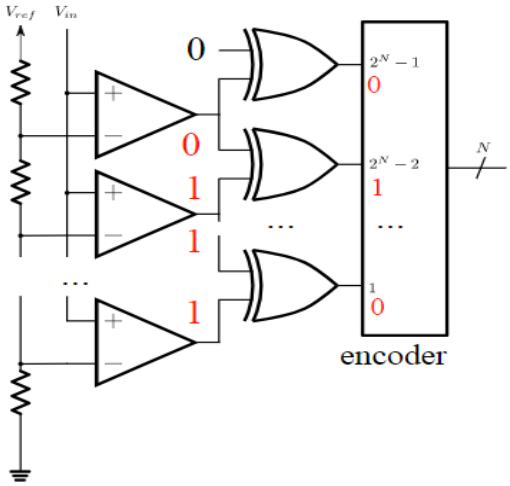

Fig 4: Flash ADC

The conversion speed of the flash ADC is the sum of the comparator delays and the logic delay (the logic delay is usually negligible) [4]. Flash ADCs are very fast, but consume enormous amounts of IC area. Also, because of the number of comparators required, power consumption is more, drawing significant amount of current.

Advantages: It is the fastest ADC, The conversion happens instantly as each clock pulse generates an output digital word.

Disadvantages: The size of the circuit doubles with increase in number of bits, N bit design requires 2^{N-1} comparators. The input capacitance of the comparator is high, Power consumption is high due to circuit complexity.

2] Two-step flash ADC:

Conversion in a two-step flash ADC takes place in two stages. Converters are separated into two flash ADC of single step with feed forward circuitry. Feed forward circuitry senses and measures all the incoming signals and then computes the effect of change in signal and process it. This mainly helps in removing the errors which might have mainly caused due to the changes in incoming signal.

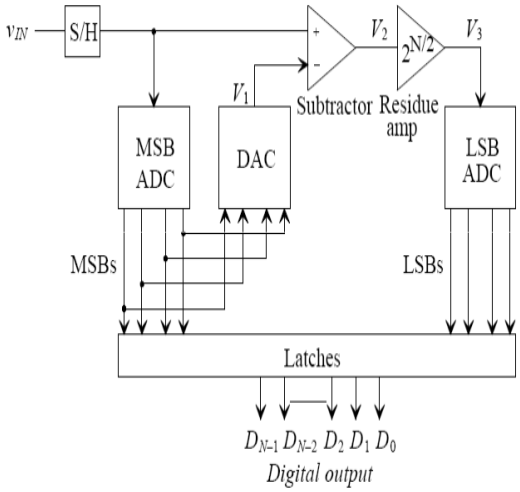

Fig 5: Two-step Flash ADC

The Two-Step Flash architecture evolved from the Full-Flash converter. One of the main drawbacks of the latter is the number of necessary comparators, given by $N_{comp.} = 2^N - 1$, which scales exponentially with the resolution of the converter (N), making it, in some cases, impractical to implement due to the necessary die area. The Two-Step Flash topology alleviates the number of necessary comparators by quantizing the input in two steps, hence its name. The effective reduction factor in the number of comparators when compared to the Full-Flash ADC, is exponentially proportional to the converter's resolution.

Advantages: Number of comparators are greatly reduced compared to that of flash ADC.

Disadvantages: The conversion process takes place in two steps instead of one.

3] Pipeline ADC:

The pipeline ADC is N-step converter, with 1 bit being converted in each stage. To achieve high resolution of 10 to 13 bits at relatively fast speeds, the pipeline ADC consists of N stages connected in series. Each stage of a pipeline architecture consists of sample and hold circuit, a summer and amplifier.

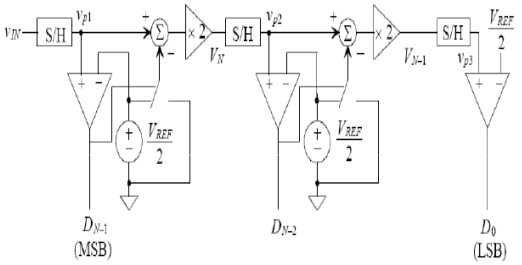

Fig 6: Pipeline ADC

Advantages: These ADC's have high throughput, each conversion takes one clock cycle after a latency of N clock cycles.
Disadvantages: It has initially N clock cycles delay before the appearance of first digital output, the accuracy of the design depends on the most significant stage and if errors are not corrected initially those errors would be propagated throughout the conversion process.

4] Successive approximation ADC:

SAR ADC uses binary search algorithm [number to be stored either in ascending or descending order]. Based on the length it will start searching from its middle term. The different blocks of SAR ADC is shown in Fig 7. SAR unit is heart of the circuit. SAR sets the most significant bit to 1 and rest all other bits are set to 0.
A successive approximation converter uses a comparator and counting logic to perform a conversion. The first step in the conversion is to see if the input is greater than half the reference voltage. If it is, the most significant bit (MSB) of the output is set. This value is then subtracted from the input, and the result is checked for one quarter of the reference voltage. This process continues until all the output bits have been set or reset. A successive approximation ADC takes as many clock cycles as per the number of output bits to perform a conversion.

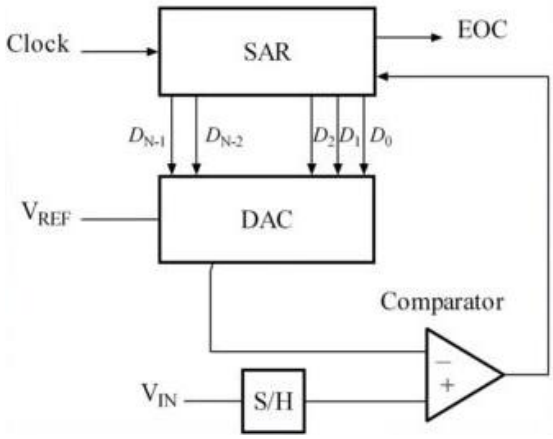

Fig 7: Block diagram of SAR ADC.

Advantages: For an N-bit ADC conversion time is equal to 'N' clock cycle. Hence the time required for conversion is small, Conversion time is constant and independent of the amplitude of input analog signal.
Disadvantages: The conversion time is more compared to flash type ADC.

5] Sigma-delta ADC (ΣΔ):

A sigma-delta ADC uses 1-bit DAC, filtering, and oversampling to achieve very accurate conversions. The conversion accuracy is controlled by the input reference and the input clock rate.

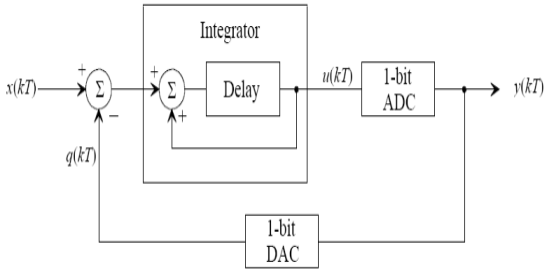

Fig 8: Sigma delta ADC.

The primary advantage of a sigma-delta converter is its high resolution. The flash and successive approximation ADCs use a resistor ladder or resistor string network. The problem with this is that the accuracy of the resistors directly affects the accuracy of the conversion result. Although modern ADCs use very precise, laser-trimmed resistor networks, some inaccuracies still persist in the resistor ladders. The sigma-delta converter does not have a resistor ladder but instead takes a number of samples to obtain result.
Advantages: These ADC's have high resolution,these are used in precision industrial measurement and instrumentation and no precision external components needed.
Disadvantages: Slow due to over sampling and has high cycle-latency.

6] Oversampling ADC:

ADC's are generally classified based on their sampling rate. Sampling rate depends on the Nyquist rate. A signal must be sampled at a rate much higher than twice its bandwidth. Nyquist rate, $f_N = 2F$ where F is the bandwidth of the signaland f_N is the sampling rate.The over sampling ADC is able to achieve much higher resolution than the Nyquist rate converters. The accuracy of the converter does not depend on the component matching, precise sample-and-hold circuitry, or trimming, and only a small amount of analog circuitry is required.

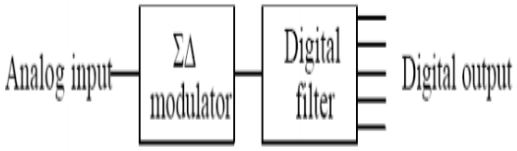

Fig 9: Oversampling ADC.

For over sampled ADCs, aliasing becomes much less of a factor. Since the sampling rate is much greater than the bandwidth of the signal, the frequency domain representation shows that the spectra are widely spaced. The ΣΔ modulator actually provides the quantization in the form of a pulse-density modulated signal. The density of the pulses

represents the average value of the signal over a specific period.

Advantages: It has high dynamic range and wide input signal bandwidth, it has high sampling rate to avoid aliasing effect.

Disadvantage: Due to high sampling rate, time required for conversion is high.

7] Time- Interleaved ADC:

Time Interleaving ADC is a popular technique which is very much essential to increase the throughput and the rate of conversion of the converter. This method can be applied to all ADC topologies. The basic components of the time interleaved ADC are M-parallel converter which are multiplexed at the input to the output. For the ease of implementation the operating range of the converter is F_S/M, where Fs is the total conversion rate and M is the number. These ADCs have high speed and low accuracy hence these are not used much. Fig 11 shows the Time Interleaved ADC which AS V_{in} has the input voltage and Fs is the conversion rate given to the ADC.

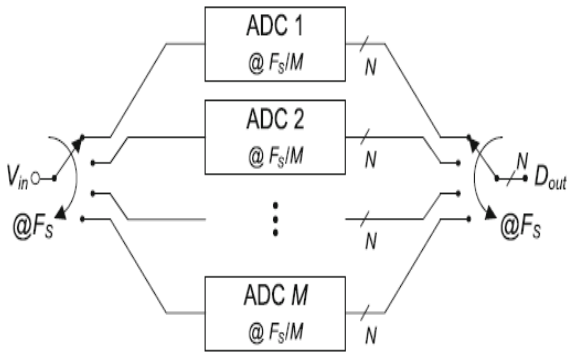

Fig 10: Time-Interleaved ADC.

Advantages: Flash ADC's become inefficient for resolutions higher than 5-6 bits, Time-interleaved ADC's can give nominal resolution up to 14-bits and gives high aggregate throughput.

Disadvantage: The sampling times of n ADC's are staggered in time.To complete one conersion it requires $N.T_s$cycles, where T_s isthe sampling period.

8] Integrating ADC:

The integrating ADC performs conversion of the input code by integrating the input signal and by correlating the integration time with a digital counter. These types of ADC's are required to obtain applications having higher resolution and relatively slow conversions. Integrating ADC's are of two types namely single slope ADC and dual slope ADC.

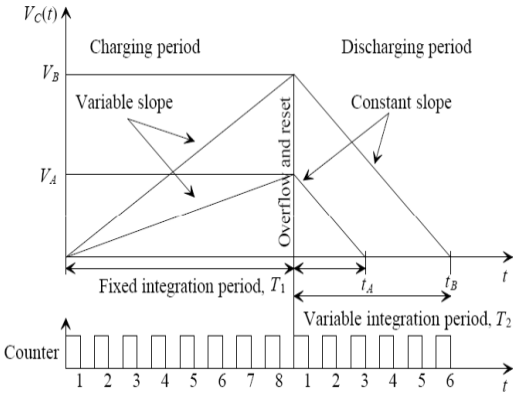

Fig 11: Characteristics of Dual-slope ADC.

Advantages: It has got relatively good linearity, It is less complex and power efficiency is high due to presence of only one comparator.

Disadvantages: It is slow as it takes 2^Nbit clock cycles for coversion of single bit.

III. COMPARISON BETWEEN TYPES OF ADC'S:

Types of ADC	Speed	Accuracy
Flash ADC	High	Low-to-medium
Two-step flash ADC	High	Low-to-medium
pipeline ADC	High	Low-to-medium
SAR ADC	Medium	Medium
Time-Interleaved ADC	High	Low-to-medium
Integrating ADC	Low-to-medium	High
Oversampling ADC	Low-to-medium	High

Table 1: Comparison table based on speed and accuracy.

Based on speed and accuracy ADC's are compared in table 1. ADC's like flash, two-step flash, pipeline and time-interleaved ADC's are having high speed and low-to-medium accuracy. SAR ADC has medium speed and medium accuracy. Integrating and oversampling ADC's have medium speed and high accuracy. Based on applications these ADC's can be used.

Fig 12 shows the comparision based on number of bits of resolution on x-axis and convention time, complexity and component matched respectively in Fig (a), (b) and (c). Based on their architectural trade-offs these graph are plotted,Based on their resolution and sampling rate along with its application. The above graph shows the application of sigma delta ADC, SAR and pipeline ADC. The above

graph depicts various applications in the field of Industrial measurement, Data acquisition.

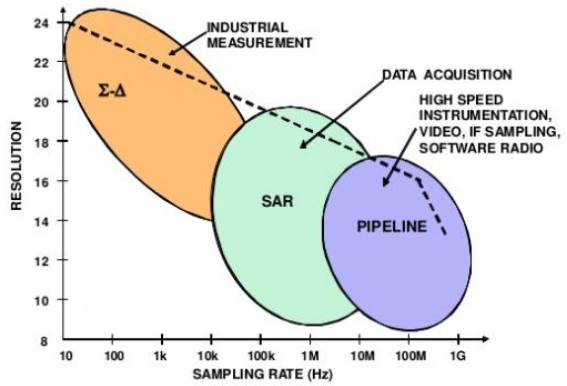

Fig 13: Graphical representation of ADC's.

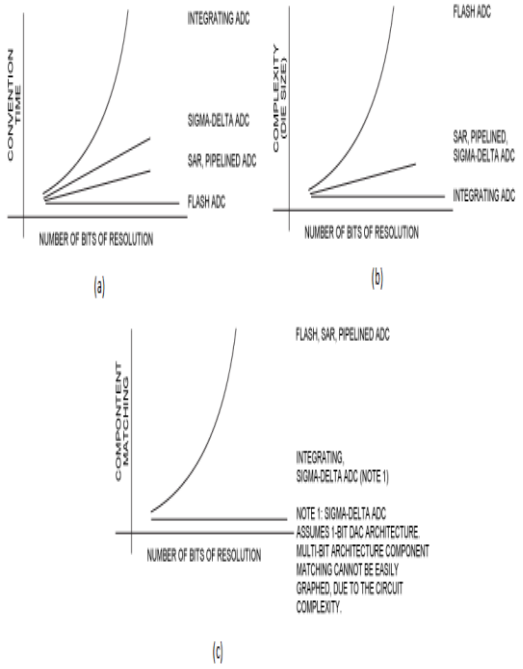

Fig 12: Architectural Trade-off.

IV. CONCLUSION:

This paper has explained about different types of ADCs. It also explains the working principle thus giving a thorough understanding of how an analog signal gets converted in to discreet form. Comparision of performance metrics is also discussed in brief. Lastly comparision between different types of ADCs based on its resolution accuracy speed and sampling rate etc., is given. Based on the application a suitable ADC can be selected.

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REFERENCES

[1] F. Fuiano, L. Cagnazzo, and P. Carbone, "Data Converters: an Empirical Research on the Correlation between Scientific Literature and Patenting Activity," Proc. of 2011 IMEKO IWADC & IEEE ADC Forum, Orvieto, Italy, pp. 1–6, June, 2011

[2] SteveBowling,―UnderstandingA/D Converter Performance Specifications‖, Microchip Technology Inc.

[3] Amir Arian, Mehdi Saberi, and Saied Hosseini-Khayat, ―Successive Approximation ADCwith Redundancy Using Split Capacitive-Array DAC‖, Department of Electrical Engineering, Ferdowsi University of Mashhad Mashhad, I. R. Iran.

[4] F. Kaess, R. Kanan, B. Hochet, and M. Declercq, "New encoding scheme for high-speed flash ADC's," in Proceedings of IEEE International Symposium on Circuits and Systems, vol. 1, June 1997.

[5] K. G. Merkel, and A. L. Wilson, "A survey of high performance analog-to-digital converters for defense space applications," in Proc. IEEE Aerospace Conf., Big Sky, Montana, Mar. 2003, vol. 5, pp. 2415–2427

[6] R.Jacob Baker, ―CMOS Circuit Design, Layout, And Simulation‖, IEEE Press Series on Microelectronic Systems Stuart K. Tewksbury and Joe E. Brewer, Series Editors, pp 523-538.

[7] B. E. Jonsson, "A survey of A/D-converter performance evolution," Proc. of IEEE Int. Conf. Electronics Circ. Syst. (ICECS), Athens, Greece, pp. 768–771, Dec., 2010.

[8] Dr. Paul Hasler and Dr. Philip Allen, ―Data Converter Overview DACs and ADCs‖

[9] B. Le, T. W. Rondeau, J. H. Reed, and C. W. Bostian, "Analog-to-digital converters [A review of the past, present, and future]," IEEE Signal Processing Magazine, pp. 69–77, Nov. 2005.

[10] K.Bult,"Embeddedanalog-todigitalconverters," Proc.ofEur.Solid-StateCirc. Conf. (ESSCIRC), Athens, Greece, pp. 52–60, Sept., 2009.

[11] B. E. Jonsson, "An empirical approach to findingenergyefficientADCarchitectures," Proc of 2011 IMEKO IWADC & IEEE ADC Forum, Orvieto, Italy, pp. 1–6, June 2011.

[12] B.Murmann, "ADC Performance Survey 1997-2012,"[Online].Available: http://www.stanford.edu/~murmann/adcsurvey.html.

[13] B. E. Jonsson, "Using Figures-of-Merit to EvaluateMeasuredA/DConverterPerformance," Proc. of 2011 IMEKO IWADC & IEEE ADC Forum, Orvieto, Italy, pp. 1–6, June 2011

[14] R. A. Nordstrom, "High-speed integrated A/D converter," Proc. of IEEE Solid-State Circ.

Conf. (ISSCC), Philadelphia, USA, pp. 150–151, Feb., 1976.

[15] H. Pan and A. Abidi, "Spectral spurs due to quantization in Nyquist ADCs," IEEE Trans. Circuits and Systems, pt. I, vol. 51, no. 8, pp. 1422–1439, Aug. 2004.

[16] K.Bult,"Embeddedanalog-todigitalconverters," Proc.ofEur.Solid-StateCirc. Conf. (ESSCIRC), Athens, Greece, pp. 52–60, Sept., 2009.

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