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VLSI Modeling of High Performance Aging Aware Multiplier By Using Adaptive Hold Logic Circuit

P.Lokesh[1], U.Somalatha[2], S.Chandana[3]
[1]*P.Lokesh, Assistant Professor, Vemu Institute Of Technology, P.Kothakota*
[2]*U.Somalatha Assistant Professor, Vemu Institute Of Technology, P.Kothakota*
[3]*S.Chandana Assistant Professor, Vemu Institute Of Technology, P.Kothakota*
Corresponding Author: P.Lokesh

ABSTRACT
Digital multipliers are most critical Arithmetic Logic Units. The performance of ALU systems depends on the throughput of the multiplier. In VLSI, the negative bias temperature instability effect occurs when a pmos Transistor is under negative bias. This result in increasing the threshold voltage of pmos transistor. This phenomenon seriously reduces the speed of multiplier. Similarly th positive bias instability occurs when an nmos transistor is under positive bias. These positive and negative biasing effects degrade the speed of multiplier,degrade the speed of transistor and in long term, the system may fail due to timing violations. In this paper we proposed to design a reliable high performance multiplier with a novel Adaptive Hold Logic(AHL) circuit. With AHL the multiplier is able to provide a higher throughput. The design is implemented by using Advanced design tools like Xilinx14.3 ISE Design suite. The experimental results shows that the proposed architecture yields high performance when compare to the Exixting Architecture.
Keywords: *Adaptive hold logic (AHL)), Xilinx14.3, Virtex6 FPFA.*

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I. INTRODUCTION

Virtual multipliers are most of the maximum critical arithmetic functional units in many programs, consisting of the Fourier remodel, discrete cosine transforms, and virtual filtering. The through placed of these applications relies upon on multipliers, and if the multipliers are too gradual, the performance of entire circuits may be reduced. moreover, negative bias temperature instability (NBTI) happens when a pMOS transistor is underneath terrible bias (Vgs = −Vdd). In this case, the interplay among inversion layer holes and hydrogen-passivated Si atoms breaks the Si–H bond generated during the oxidation method, producing H or H2 molecules. while these molecules diffuse away, interface traps are left.

The collected interface traps between silicon and the gate oxide interface bring about multiplied threshold voltage (Vth), decreasing the circuit switching speed. while the biased voltage is eliminated, the opposite response takes place, reducing the NBTI impact. but, the opposite reaction does not take away all the interface traps generated uring the stress segment, and Vth is multiplied inside the long time. subsequently, it's miles crucial to layout a dependable excessive-overall performance multiplier. The corresponding effect on an nMOS transistor is effective bias temperature instability (PBTI),which takes place while an nMOS transistor is below high quality bias. in comparison with the NBTI impact, the PBTI effect is tons smaller on oxide/polygate transistors, and consequently is usually unnoticed. however, for excessive-okay/metal-gate nMOS transistors with big fee trapping, the PBTI effect can now not be disregarded. In reality, it's been shown that the PBTI impact is extra considerable than the NBTI effect on 32-nm high-k/steel-gate methods [2]–[4].

A traditional approach to mitigate the aging impact is overdesign [5], [6], which includes things like shield-banding and gate oversizing; but, this method can be very pessimistic and location and power inefficient. To keep away from this hassle, many NBTI-aware methodologies had been proposed. An NBTI-conscious generation mapping technique became proposed in [7] to assure the performance of the circuit in the course of its lifetime. In [8], an NBTI-aware sleep transistor become designed to lessen the getting old consequences on pMOS sleep-transistors, and the mlifetime balance of the power-gated circuits under attention turned into stepped forward. Wu and Marculescu [9] proposed a oint common sense restructuring and pin reordering method, that is based on detecting useful symmetries and transistor stacking outcomes. additionally they proposed an NBTI optimization technique that taken into consideration direction sensitization [12]. In [10] and [11], dynamic voltage scaling and frame-

basing techniques had been proposed to reduce electricity or extend circuit lifestyles. those strategies, however, require circuit amendment or do now not offer optimization of precise circuits.
traditional circuits use crucial route delay as the general circuit clock cycle if you want to carry out successfully. but, the chance that the essential paths are activated is low. In most instances, the direction delay is shorter than the critical course. For these noncritical paths, the usage of the crucial path delay as the overall cycle length will result in considerable timing waste. for this reason, the variable-latency design was proposed to lessen the timing waste of conventional circuits. The variable-latency layout divides the circuit into two components: 1) shorter paths and a couple of) longer paths. Shorter paths can execute successfully in one cycle, whereas longer paths want cycles to execute. when shorter paths are activated frequently, the common latency of variable-latency designs is better than that of conventional designs. for example, numerous variable-latency adders had been proposed using the hypothesis approach with mistakes detection and restoration [13]–[15]. A short route activation characteristic algorithm became proposed in [16] to enhance the accuracy of the keep common sense and to optimize the overall performance of the variable-latency circuit. An instruction scheduling algorithm turned into proposed in [17] to agenda the operations on nonuniform latency functional devices and improve the overall performance of Very long training phrase processors. In [18], a variable-latency pipelined multiplier architecture witha booth set of rules turned into proposed. In [19], manner-version tolerant structure for mathematics gadgets changed into proposed, where the effect of system-variant is considered to boom the circuit yield. in addition, the essential paths are divided into two shorter paths that could be unequal and the clock cycle is set to the postpone of the longer one. those research designs had been able to lessen the timing waste of conventional circuits to enhance performance, but they did not recollect the getting older impact and could not alter themselves during the runtime. A variable-latency adder design that considers the ageing effect become proposed in [20] and [21]. however, no variable-latency multiplier layout that considers the getting old impact and can modify dynamically has been carried out.

II. PAPER CONTRIBUTION

In this paper, we propose an aging-aware reliable multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. To be specific, the contributions of this paper are summarized as follows: 1) novel variable-latency multiplier architecture with an AHL circuit. The AHL circuit can decide whether the input patterns require one or two cycles and can adjust the judging criteria to ensure that there is minimum performance degradation after considerable aging occurs; 2) comprehensive analysis and comparison of the multiplier's performance under different cycle periods to show the effectiveness of our proposed architecture;3) an aging-aware reliable multiplier design method that is uitable for large multipliers.

III. ADAPTIVE HOLD LOGIC

The adaptive logic programme aims at developing a type of formal logics (and the connected metatheory) that is especially suited to explicate the many interesting dynamic consequence relations that occur in human reasoning but for which there is no positive test (see the next section). Such consequence relations occur, for example, in inductive reasoning, handling inconsistent data, ...

The explication of such consequence relations is realized by the dynamic proof theories of adaptive logics. These proof theories are dynamic in that formulas derived at some stage may not be derived at a later stage, and vice versa.

The programme is application driven. This is one of the reasons why the predicative level is considered extremely important, even if, for many adaptive logics, the basic features of the dynamics are already present at the propositional level. The main applications are taken from the philosophy of science; some also from more pedestrian contexts.

The interest in dynamic consequence relations led rather naturally to an interest in dynamic aspects of reasoning. Some of these already occur in Classical Logic (henceforth CL).
Much interesting actual reasoning displays two forms of non-standard dynamics.

1. An external dynamics: a conclusion may be withdrawn in view of new information. This means that the consequence relation is non-monotonic.[1]
2. An internal dynamics: a conclusion may be withdrawn in view of the better understanding of the premises provided by a continuation of the reasoning.

IV. EXISTING MULTIPLIERS

Multiplication – an important fundamental function in arithmetic operation. Currently implemented in many DSP applications such as FFT, Filtering etc., and usually contribute

significantly to time delay and take up a great deal of silicon area in DSP system. Now – a – days time is still an important issue for the determination of the instruction cycle time of the DSP hip. Both the multiplication and the DSP play a vital role in the implementation of VLSI system. Multiplication – Repeated addition of n – bits will give the solution for the multiplication. The various multipliers are:

A. 4x4Braun multiplier

The Braun multiplier removes the extra correction circuitry needed. Also number of adders is less. But, the limitation of this technique is that it cannot stop the switching activity even if the bit coefficient is zero that ultimately results in unnecessary time delay. Another high speed designs disable the operation in some rows, designed a technique that reduces the switching to fairly good extent.

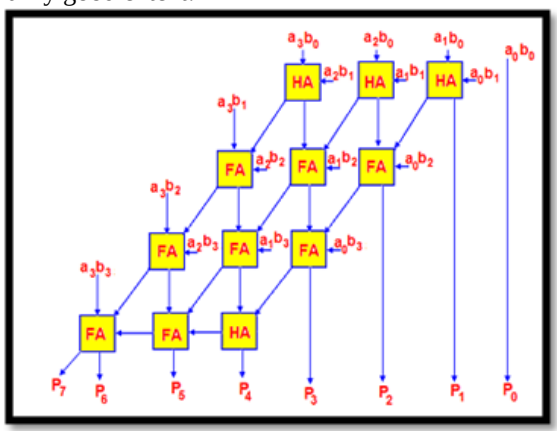

Fig 1. Schematic diagram of Braun multiplier

B. 4x4 Row bypassing multiplier

The Row bypassing multiplier reduces the switching activity by bypassing the row in which the multiplicand bit is zero. That means in the multiplier if a bit is zero then that row of adders will get disabled. For example consider the multiplication of 1011 x 1010. Here the multiplier consists of zero in first and third positions. During multiplication the first and third row of adders get disabled and previous sum is taken as the present sum.

C. 4x4 Column bypassing multiplier

Consider the multiplication of 1010 x 1000. Since the multiplicand contains two zeros, the corresponding columnsi.e. first and third will get disabled. Now, consider another multiplication of 1111 x 1000. Since multiplicand contains no zero, all columns will get switched.

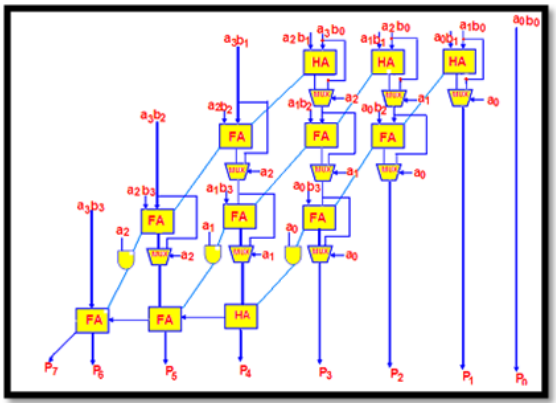

Fig 2. Column bypass multiplier

V. PROPOSED AGING AWARE MULTIPLIER

The proposed aging-aware reliable multiplier design. It introduces the overall architecture and the functions of each component and also describes how to design AHL that adjusts the circuit when significant aging occurs.

Proposed Architecture

proposed aging-aware multiplier architecture, which includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multiplier, 2m 1-bit Razor flip-flops [27], and an AHL circuit.

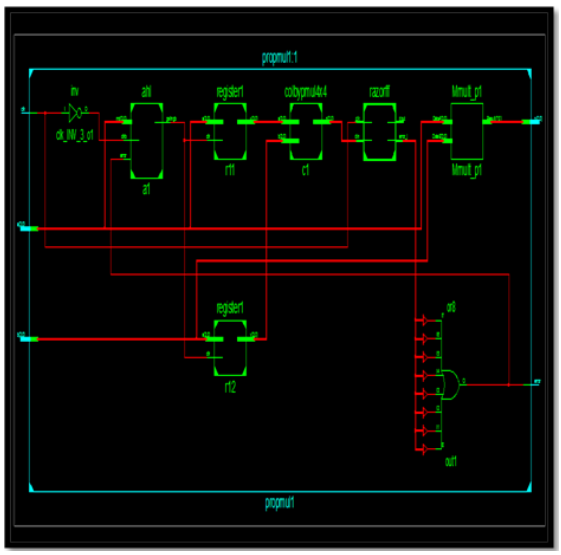

Fig 3. Proposed architecture (md means multiplicand; mr means multiplicator).

Hence, the two aging-aware multipliers can be implemented using similar architecture, and the difference between he two bypassing multipliers lies in the input signals of the AHL. According to the bypassing selection in the columnor row-bypassing multiplier, the input signal of the AHL in the architecture with the column-bypassing

multiplier is the multiplicand, whereas of the row-bypassing multiplier is the multiplicator. Razor flip-flops can be used to detect whether timing violations occur before the next input pattern arrives.

VI. RESULT ANALYSIS

Xilinx ISE

Xilinx ISE 14.3 (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis ofHDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTLdiagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

The **Xilinx ISE** is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors. The Xilinx ISE is primarily used for circuit synthesis and design, while the ModelSim logic simulator is used for system-level testing Other components shipped with the Xilinx ISE include the Embedded Development Kit (EDK), a Software Development Kit (SDK) and ChipScope Pro.

Simulation

System-level testing may be performed with the Xilinx logic simulator, and such test programs must also be written in HDL languages. Test bench programs may include simulated input signal waveforms, or monitors which observe and verify the outputs of the device under test.

Xilinx logic simulator may be used to perform the following types of simulations:

- Logical verification, to ensure the module produces expected results
- Behavioural verification, to verify logical and timing issues
- Post-place & route simulation, to verify behaviour after placement of the module within the reconfigurable logic of the FPGA

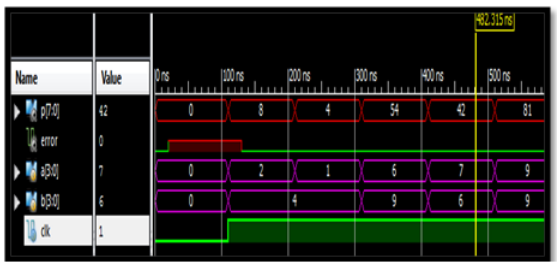

Fig4. Simulation Waveforms

In fig4. For two inputs a and b the result produced is a product between a and b they are multiplicand and multiplier only when the system is free from errors.

Synthesis

Xilinx's patented algorithms for synthesis allow designs to run upto 30% faster than competing programs, and allows greater logic density which reduces project costs. Also, due to the increasing complexity of FPGA fabric, including memory blocks and I/O blocks, more complex synthesis algorithms were developed that separate unrelated modules into slices, reducing post-placement errors. IP Cores are offered by Xilinx and other third-party vendors, to implement system-level functions such as digital signal processing (DSP), bus interfaces, networking protocols, image processing, embedded processors, and peripherals.Xilinx has been instrumental in shifting designs from ASIC-based implementation to FPGA-based implementation

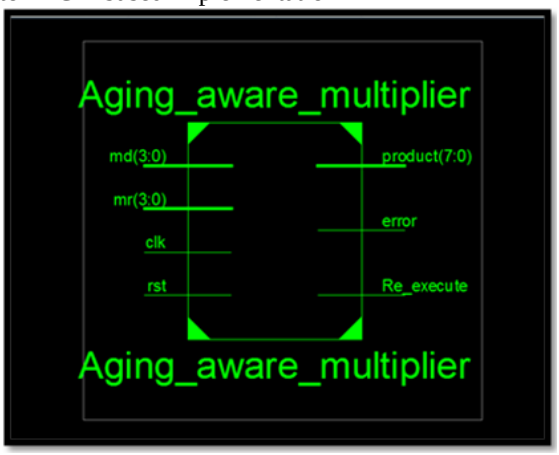

Fig.5 AGING Aware Multiplier Topmodule

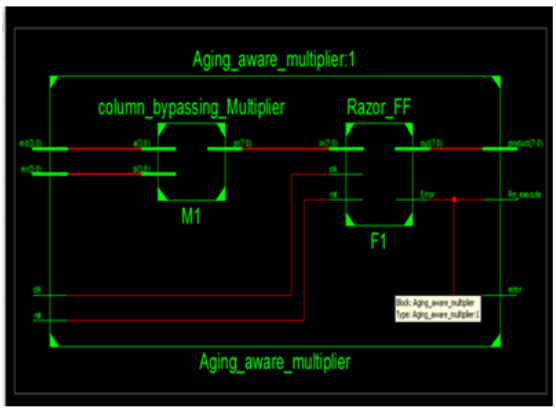

Fig 6. RTL Schematic

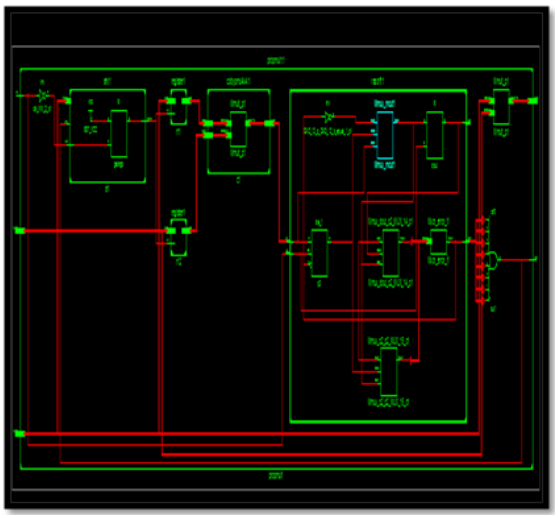

Fig 7. Technology Schematic

ahl Project Status (11/23/2017 - 15:03:09)

Project File:	aging.xise	Parser Errors:	X 2 Errors
Module Name:	propmul1	Implementation State:	Synthesized
Target Device:	xc6vlx75t-2ff484	• Errors:	No Errors
Product Version:	ISE 14.3	• Warnings:	58 Warnings (58 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	25	93120	0%
Number of Slice LUTs	58	46560	0%
Number of fully used LUT-FF pairs	13	70	18%
Number of bonded IOBs	18	240	7%
Number of BUFG/BUFGCTRLs	1	32	3%

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Thu Nov 23 15:03:08 2017	0	58 Warnings (58 new)	19 Infos (19 new)
Translation Report					

Fig 8. Design summary

```
Data Path: a<3> to p<7>
                           Gate     Net
  Cell:in->out      fanout Delay    Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   IBUF:I->O             12  0.003   0.627  a_3_IBUF (a_3_IBUF)
   LUT4:I0->O             1  0.061   0.696  Mmult_p_Madd1_lut<4>1 (Mmult_p_Madd1_lut<4>)
   LUT6:I0->O             1  0.061   0.696  Mmult_p_Madd1_xor<4>11 (Mmult_p_Madd_41)
   LUT6:I0->O             1  0.061   0.000  Mmult_p_Madd2_lut<4> (Mmult_p_Madd2_lut<4>)
   MUXCY:S->O             1  0.248   0.000  Mmult_p_Madd2_cy<4> (Mmult_p_Madd2_cy<4>)
   MUXCY:CI->O            1  0.017   0.000  Mmult_p_Madd2_cy<5> (Mmult_p_Madd2_cy<5>)
   MUXCY:CI->O            0  0.017   0.000  Mmult_p_Madd2_cy<6> (Mmult_p_Madd2_cy<6>)
   XORCY:CI->O            1  0.204   0.339  Mmult_p_Madd2_xor<7> (p_7_OBUF)
   OBUF:I->O                 0.003          p_7_OBUF (p<7>)
  ----------------------------------------
  Total                      3.034ns (0.675ns logic, 2.359ns route)
                                     (22.2% logic, 77.8% route)
```

Fig 9. Synthesis Report

VII. CONCLUSION

This paper proposed an aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The variable-latency bypassing multipliers exhibited the lowest average EDP and achieved up to 10.45% EDP reduction in 32 × 32 VLCB multipliers. Note that in addition to the BTI effect that increases transistor delay, interconnect also has its aging issue, which is called electromigration. Electromigration occurs when the current density is high enough to cause the drift of metal ions along the direction of electron flow.

The metal atoms will be gradually displaced after a period of time, and the geometry of the wires will change. If a wire becomes narrower, the resistance and delay of the wire will be increased, and in the end, electromigration may lead to open circuits. This issue is also more serious in advanced process technology because metal wires are narrower, and changes in the wire width will cause larger resistance differences. If the aging effects caused by the BTI effect and electromigration are considered together, the delay and performance degradation will be more significant. Fortunately, our proposed variable latency multipliers can be used under the influence of both the BTI effect and electromigration. In addition, our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electromigration and use the worst case delay as the cycle period.

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AUTHORS

P.Lokesh received his B.Tech degree in Electronics & Communication Engineering from Yogananda Institute of Technology and Science, Tirupati (A.P), India, in the year 2013. M.Tech degree in VLSI System Design at Chadalawada Ramanamma Engineering College,Tirupati(A.P), India in the year 2015.Currently working as a Assistant Professor in VEMU Institute of Technology, P.Kothakota. His area of research Includes Low power VLSI design, Embedded systems.

U.Somalatha received her B.Tech degree in Electronics & Communication Engineering from yogananda Institute of Technology and Science, India, in the year 2012. M.Tech degree in DECS from Sree Vidyanikethan college of Engineering ,Tirupati(A.P), India..Currently working as a Assistant Professor in VEMU Institute of Technology, P.Kothakota. Her area of research Includes VLSI design,Digital Image Processing.

S.Chandana received her B.Tech degree in Electronics & Communication Engineering from VEMU Institute of Technology, P.KOTHAKOTA India, in the year 2013. M.Tech degree in DECS from Annamacharya Institute of Technology, Tirupati(A.P), India..Currently working as a Assistant Professor in VEMU Institute of Technology, P.Kothakota. Her area of research Includes Low power VLSI design.

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