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Implementation of DSP architecture for LMS

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ABSTRACT
In this paper we have used Urdhva Tiryakbhyam Multipliers method in arithmetic logic unit with carry select adder, high speed Vedic Multiplication techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance of conventional arithmetic logic unit. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on sixteen Sutras. We have done study on efficiency of Urdhva Triyagbhyam – Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It eliminates unwanted multiplication steps with zeros and scaled to higher bit levels using Karatsuba algorithm with the compatibility to different data types. Urdhva tiryakbhyam Sutra is most efficient Sutra method, provide minimum processing delay for multiplication of all types of numbers, either small or large. In this project we will implement DSP architecture method in Xilinx to perform LMS algorithm.
Keywords: Urdhva Tiryakbhyam, carry select adder, LMS, etc.

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I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic logic unit. Some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as filtering, Fast Fourier Transform(FFT), convolution and in microprocessors in its arithmetic logic unit [1]. Since multiplication takes too much of DSP algorithms. Presently, multiplication process time is still the dominant factor in determining the instruction cycle time of a DSP chip. So there is a need of high speed multiplier.

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are too important to achieve the desired performance in many real-time signal and image processing applications [2]. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the power consumption and time delay is very essential requirements for many applications [2, 3]. This work presents different multiplier, square and cube architectures. In multiplier based on Vedic Mathematics is one of the fast and low power multiplier.

For Minimizing power consumption of digital systems involve in design, different optimization technology includes using and implementing the digital circuits, topology and the circuit style, the architecture for implementing the circuits and at the highest leveling the algorithms that are being implemented. Multipliers are the most commonly used elements in all arithmetic logic units (ALU). Vedic multipliers are fast, reliable and efficient part of ALU that are utilized to implement any operation. Depending upon the different method of multiplication, there are different types of multipliers available. Different type of multipliers architecture is chosen based on the application, which provides different delay and different power consumption.

In DSP processes, the multiplier perform very important role. The speed of multiplication operation is of great importance in digital signal processer as well as in general processor. There have been many algorithms proposals in literature to perform multiplication, every offering different advantages and disadvantage, circuit complexity, area and power consumption.

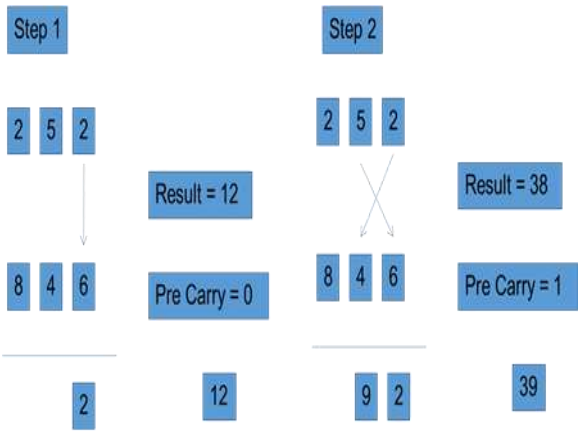
Thus many attempts have been reported in literature about improvement in multipliers speed that has the least number of gate delays and power consume the least amount of chip area. The amount of circuitry involved in design is directly proportional to the square of its resolution; multiplier is not only a high delay block but also a major source of power dissipation. That is why if one also aims to minimize power consumption, it is a great area of interest to reduce the delay by using various delay optimizations.

II. THE VEDIC MULTIPLICATION METHOD

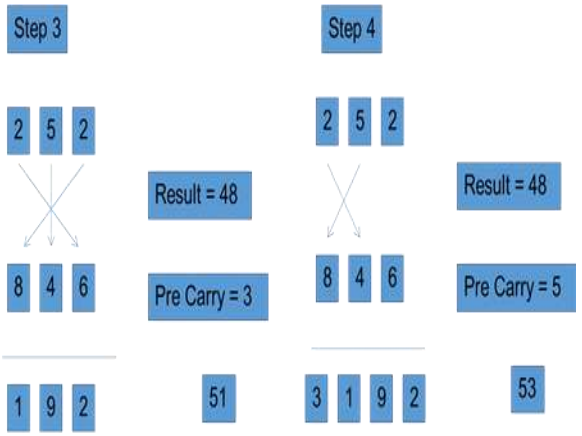
Two numbers decimal system can be multiply speedily using Vedic multiplication method. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on Urdhava Tiryakbhyam sutra is discussed below:

III. URDHAVA TIRYAKBHYAM SUTRA

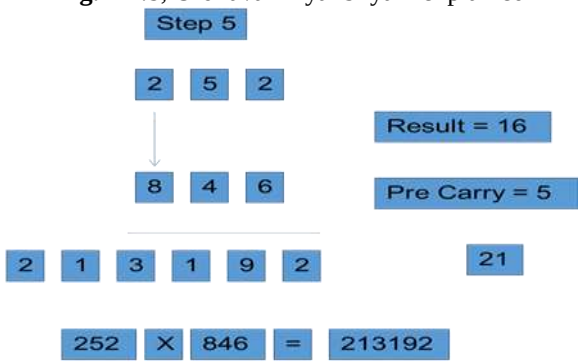
The multiplier is based on an algorithm Urdhava Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhava Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". Urdhava Tiryakbhyam Vedic multiplication method based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhava Tiryakbhyam explained in Figure 1 with example. The algorithm can be generalized for n x n bit number. Hence the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Hence the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net benefit is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its one disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily resolve these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure [7]. Due to its regular structure, it can be easily layout in a silicon chip (IC). The Vedic Multiplier has the advantage over simple multiplier that as the number of bits increases, gate delay and area of fabrication increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. Multiplication of two decimal numbers- 252*846 to illustrate this multiplication scheme let us consider the multiplication of two decimal numbers (252 * 846). Line diagram of Vedic multiplier is shown in below Fig 1. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero. To Make the methodology more clear, an alternate illustration is given with the help of line diagrams in Figure 1 where the dots represent bit 0 or 1. [6]



"**Fig." 1.a**, Urdhava Tiryakbhyam explained



"**Fig." 1**.b, Urdhava Tiryakbhyam explained

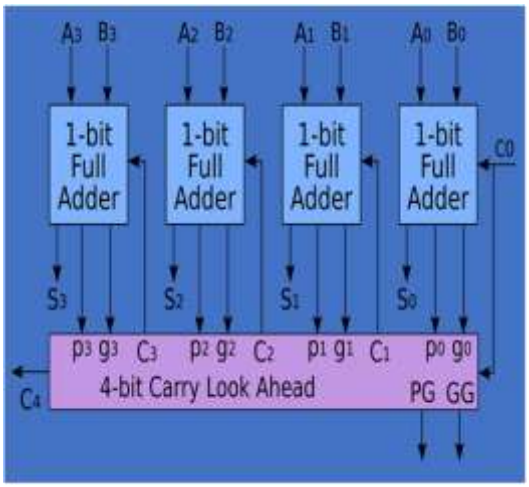


"**Fig." 1**.c, Urdhava Tiryakbhyam explained

IV. CARRY LOOK-AHEAD ADDER

Carry look-ahead adder is designed to overcome the latency introduced by the rippling effect of the carry bits. The propagation delay occurred in the parallel adders can be eliminated by

carry look ahead adder. This adder is based on the principle of looking at the lower order bits of the augends and addend if a higher order carry is generated. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate.



"**Fig." 2** Carry select adder

V. LEAST MEAN SQUARE (LMS) ALGORITHM

The Least Mean Square (LMS) algorithm was first developed by Widrow and Hoff in 1959 through their studies of pattern recognition. From there it has become one of the most widely used algorithms in adaptive filtering. The LMS algorithm is a type of adaptive filter known as stochastic gradient-based algorithms as it utilizes the gradient vector of the filter tap weights to converge on the optimal wiener solution [2-4]. It is well known and widely used due to its computational simplicity. It is this simplicity that has made it the benchmark against which all other adaptive filtering algorithms are judged. With each iteration of the LMS algorithm, the filter tap weights of the adaptive filter are updated according to the following formula.

$$w(n+1)=w(n)+2\mu e(n)x(n)$$

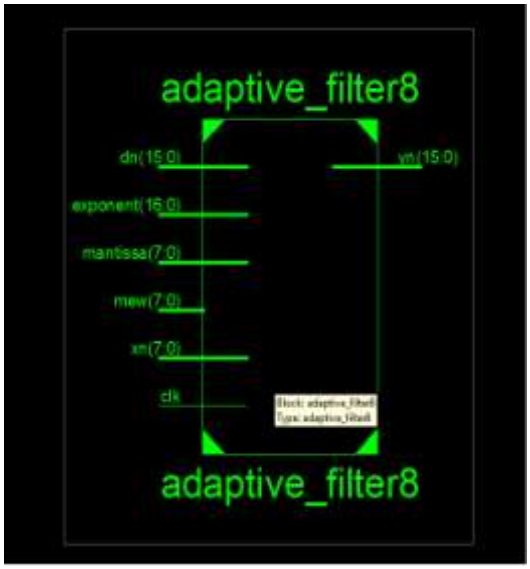
Here x(n) is the input vector of time delayed input values,

$$x(n) = 〚[x(n)\ x(n-1)\ x(n-2)\ ..x(n-N+1)]〛\ ^T$$

The vector

$$w(n)= 〚[w0(n)w1(n)w2(n)..wN-1(n)]〛\ ^T$$

represents the coefficients of the adaptive FIR filter tap weight vector at time n. The parameter μ is known as the step size parameter and is a small positive constant. This step size parameter controls the influence of the updating factor. Selection of a suitable value for μ is imperative to the performance of the LMS algorithm, if the value is too small the time the adaptive filter takes to converge on the optimal solution will be too long; if μ is too large the adaptive filter becomes unstable and its output diverges



"**Fig." 3** RTL view of LMS filter

VI. OBSERVATION AND RESULT

"**Table" 1**: observation

Device name	Spartan 3E – xc3s1400an
ALU	16x16 bits Urdhava Tiryakbhyam and Carry Look-Ahead Adder
Delay	92.445ns
Dynamic power	0.003W
Quiescent power	0.063W
Total power	0.066W

VII. CONCLUSION

In this paper we have successful implement LMS over DSP architecture. DSP architecture is design using Vedic multiplayer Urdhava Tiryakbhyam sutra method for 16x16 bits, with carry select adder to perform LMS algorithm.

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