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# Single Bit Low Power Full Adder Cell using Substrate Bias Effect

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**ABSTRACT**
Ultra low power portable electronic devices are the need of modern world. Portable devices need prolonged battery life, which can be achieved by reducing the power dissipation. Substrate bias effect is a leakage power reduction technique. It describes the changes in the threshold voltage with respect to change in source to bulk voltage. The substrate bias effect is used to control the leakage current. The reverse bias voltage widens the depletion region, due to which the threshold voltage increases. In this paper a single bit low power full adder has been proposed with substrate bias effect. Simulation of low voltage high performance hybrid single bit full adder cell also has been presented. By using the reverse biasing technique we have achieved power reduction in the single bit full adder cell. The power, delay and, power delay product (PDP) results have been obtained for proposed and existing designs with varying supply voltages. The proposed design shows PDP of 253.38fJ as compared to 277.23fJ of low voltage high performance hybrid single bit full adder cell at 1.8 Vdd. Simulation result show that the proposed design also performs better at varying temperature conditions. The power delay product has been also plotted versus the different reverse bias voltages applied in the proposed technique. All the work has been done in 180nm CMOS technology.
**Keywords:** Reverse Biasing, Single Bit Full Adder Cell, Substrate Bias Effect, Threshold Voltage

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## I. INTRODUCTION

The adders are widely used circuit elements in VLSI (Very Large Scale Integration) systems. Adders are used in Digital signal Processing DSP processors, microprocessors, Image processing, video processing. They are the core element for many other operations like addition, multiplication, subtraction, address calculation. They lie in the most critical path which influences the overall performance of the system. The vast use of battery operated applications like mobile, laptop, smart PDAs has put tight requirement on creation of low power consumption electronic circuits. The power consumption can be reduced by scaling the operating frequency and supply voltage. By the above option we can re reduce the power consumption but this in turn increases the propagation delay of the system and also degrades the driving capability of the system. In this paper we have proposed how to achieve power reduction using the Reverse Biasing technique.

### 1.1 POWER CONSUMPTION IN MOS

Due to the recent works in scaling technology there is an increase in the transistor leakage power as power consumption or dissipation increases leads to degradation in performance and reduces the design life time. The sources of power consumption in CMOS are mainly due to dynamic power dissipation and leakage power dissipation. The total power consumption can be summed up as a total of dynamic power and static power**.**

D**y**namic power is consumption due to the switching of the transistors. The dynamic power is due to discharging and charging of load capacitances. This type of power also includes the short circuit power which occurs due to the power from stacked P and N devices in CMOS logic gate that are in ON state simultaneously.[2][3][4]

Static Power is the leakage power dissipation. Nowadays this type of power dissipation has become very significant portion of power consumption. It is the power dissipation due to leakage current which flows through a transistor when no transaction occurs and transistor is in steady state, depending on the gate length and thickness of oxide layer**.** Leakage Power is the power dissipation due to spurious currents in the non-conducting state of the transistor.

$$P_T = P_D + P_{SC} + P_S$$

### 1.2 LEAKAGE POWER

Due to scaling, there has been a decrease in the channel length which leads to decrease in Vdd and Vth of MOSFET. Due to this decrement in Vth there is increase in leakage current. Increase in leakage current leads to more power dissipation. Leakage power dissipation leads to nearly 50% of the total power dissipation.

Four main sources of the Leakage are:

- Junction Leakage(IREV)
- Gate Induced Drain Leakage(GIDL)
- Gate Direct Tunneling Leakage (IG)
- Sub threshold Leakage (ISUB)

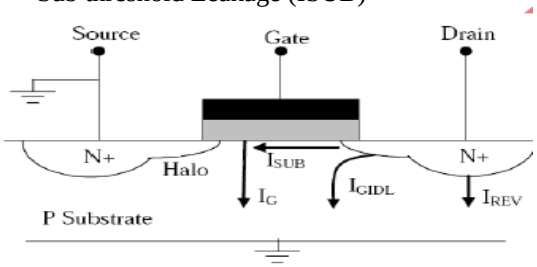


**Fig 1:** Sources of Leakage Current

## II. IMPLEMENTATION OF LOW POWER HIGH PERFORMANCE SINGLE BIT FULL ADDER CELL [1]

In the paper referred the authors have modified the conventional **(Fig 2**) single bit full adder cell. In the modified adder cell **(Fig 3)** the carry and sum outputs selection are made by control of input signal C. The signal C is not generated internally, due to which it provides full output voltage swings with no additional delay. This circuit has good driving capability and is used to drive multiplexers at the output. In the modified single bit full adder cell the NOR and the NAND gates are modified as mentioned in the **Table 1 and Table 2.**The modified single bit full adder cell is made by the above changes and Swing Restored Complimentary Pass Transistor Logic(SR-CPL).

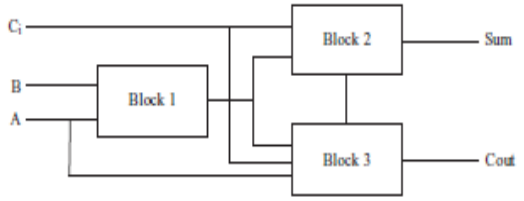


**Fig 2:**Conventional Full Adder Module

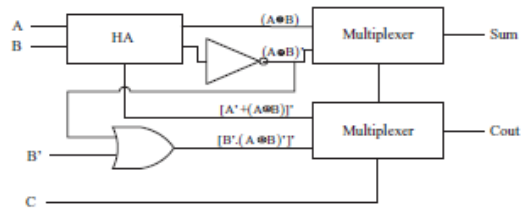


**Fig 3:** The modified Full Adder Module

**Table1:** Truth Table of modified NOR Gate

| A' | $(A \oplus B)$ | $[A'+(A \oplus B)]'$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Table2:** Truth Table of modifed NAND Gate

| B' | $(A \oplus B)'$ | $[B'.(A \oplus B)']'$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

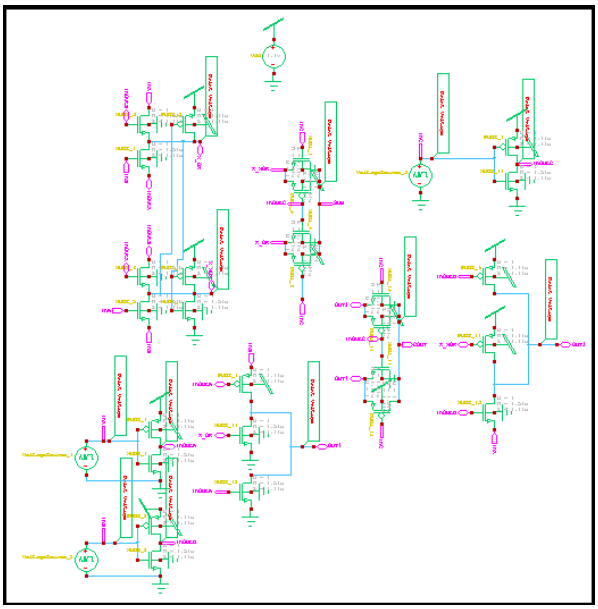

**Fig 4:** Simulated Single Bit Full Adder Cell [1]

## III. PROPOSED WORK

In this paper we have proposed a single bit low power full adder cell using substrate bias effect. The Substrate bias effect explains the change in the threshold voltage Vth by changing the value of Vbs source to bulk voltage. The substrate bias effect is used to reduce the leakage current which in turn reduces the power. The effect of the substrate bias effect can be explained in the threshold voltage equation as mentioned below.

$$V_{TB} = V_{T0} + \gamma( \sqrt{( V_{SB} + 2_{\varphi B})} - \sqrt{(2_{\varphi B})} )$$

Where $V_{TB}$ is the threshold voltage with substrate bias present, and $V_{T0}$ is the zero $V_{SB}$ value of the threshold voltage, γ is the substrate bias effect parameter ,and $2\varphi_B$ is the approximate potential drop between surface and bulk across the depletion layer when $V_{SB}$ = 0and gate bias is sufficient to insure that the channel is present.

The reverse bias voltage widens the depletion region .Due to widening of the depletion region there is an increase in the channel depth. Widening of the depletion region increases the threshold voltage. In PMOS, the body of transistor is biased to a voltage higher than $V_{dd}$. In NMOS, the body of transistor is biased to a voltage lower than $V_{ss}$.

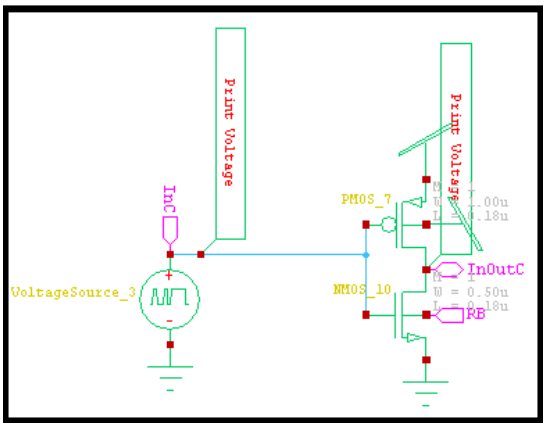


**Fig 5:** Reverse Biasing Technique

## IV. SIMULATION RESULTS

The circuit design is carried out using 180 nm files.

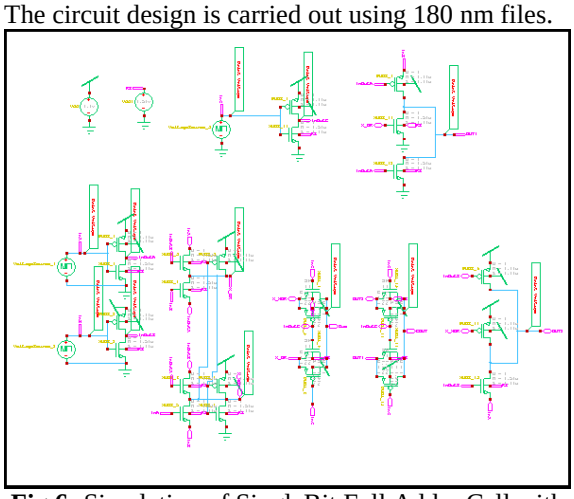

**Fig 6:** Simulation of SingleBit Full Adder Cell with Reverse Biasing

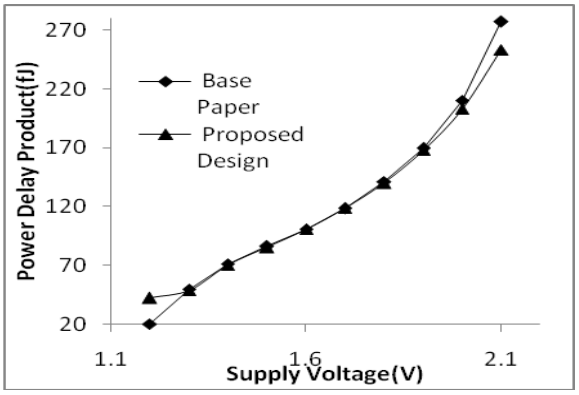


**Fig 7:** PDP vs Supply Voltage

**Table 3:** PDP vs Supply Voltage

| SUPPLY VOLTAGE | BASE PAPER | PROPOSED DESIGN |
|---|---|---|
| 1.2 | 20.32 | 42.1 |
| 1.3 | 49.8 | 48.78 |
| 1.4 | 71.21 | 70.6 |
| 1.5 | 86.04 | 85.41 |
| 1.6 | 100.76 | 101.21 |
| 1.7 | 118.33 | 119.1 |
| 1.8 | 141.21 | 140.07 |
| 1.9 | 169.7 | 168.06 |
| 2 | 210.38 | 203.35 |
| 2.1 | 277.23 | 253.38 |

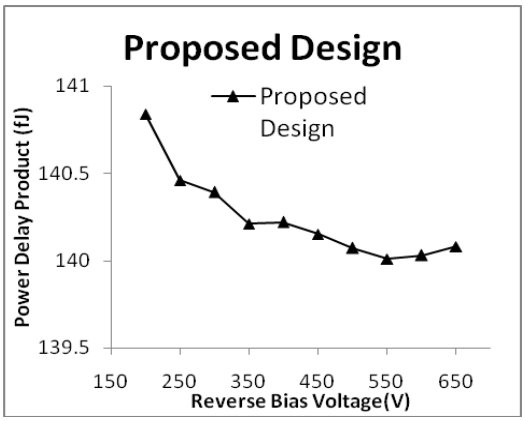


**Fig 8:** PDP vs Reverse Bias Voltage

**Table 4:** PDP vs Reverse Bias Voltage

| REVERSE BIAS VOLTAGE | PROPOSED DESIGN |
|---|---|
| 200 | 140.84 |
| 250 | 140.46 |
| 300 | 140.39 |
| 350 | 140.21 |
| 400 | 140.22 |
| 450 | 140.15 |
| 500 | 140.07 |
| 550 | 140.01 |
| 600 | 140.03 |
| 650 | 140.08 |

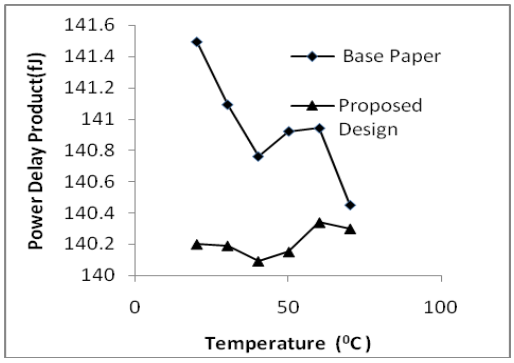


**Fig 9:** PDP vs Temperature

**Table 5:** PDP vs Temperature

| TEMPERATURE (CELSIUS) | BASE PAPER | PROPOSED DESIGN |
|---|---|---|
| 20 | 141.49 | 140.2 |
| 30 | 141.09 | 140.19 |
| 40 | 140.76 | 140.09 |
| 50 | 140.92 | 140.15 |
| 60 | 140.94 | 140.34 |
| 70 | 140.45 | 140.3 |

## V. CONCLUSION

In this paper we have focused mainly to reduce the leakage power using the reverse bias technique on the modified low voltage high performance hybrid single bit full adder cell.

From the results obtained it is clearly visible that the power delay product when plotted against the supply voltage is reduced after applying the reverse biasing technique.

We have also see the effect of temperature on the power delay product for both the base paper referred and our proposed design with the reverse biasing technique. It can be seen that with the increase in the temperature the power delay product increases for our proposed design with the reverse biasing technique.

For various reverse bias voltages applied on the proposed design, the effect on the power delay product can also be noticed.

All the above results are obtained from simulating the above mentioned work using the180 nm technology node

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