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An Improved Low Power Counter Design with Clock Enable

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ABSTRACT
This paper presents an improved low power design of a 4-bit Johnson Counter which is designed using and Clock enable method. The proposed design shows a power reduction of 5mW as compared to the conventional Johnson counter which is 7mW. Pulse triggered flip flop employed in the proposed design can save power up to 28.57% as compared to the conventional design. All the simulations were carried out using Xilinx software in SIM module.
***Keywords*:** Gating Enable, Low Power Design, Counter.

I. INTRODUCTION

Power minimization has become the main design issue in the VLSI circuits with the downscaling of the chip sizes & higher operational frequencies of the devices [1]. In digital circuits, all the operations are executed on the transition edges of the clock (positive or negative clock edge) and at every clock transition, there will always be short circuit current dissipation which contributes almost 15- 45% of the total power dissipation in the system [2]. The existing clock gated Johnson counter design reduces power dissipation to a great extend by eliminating unnecessary clock transitions and generating clock pulse sequences only when an operation needs to be performed. In this paper, the proposed Johnson counter is designed using pulse-triggered flip flops and Gate Diffusion Input based clock gated logic which enables lesser transistor count and hence ensures lower power dissipation as compared to the clock gated counter design. This paper is divided into six sections. Section II describes short circuit power dissipation in sequential circuits. Section III explains clock gated Johnson counter design. Section IV presents the proposed design. Section V shows simulations &VI concludes the paper.

II. Short Circuit Power Dissipation In Sequential

Circuits In sequential circuits, short circuit current dissipation occurs at each clock transition. Fig.1 and Fig.2 shows the schematic of a CMOS inverter and the short circuit current dissipation at every clock transition respectively. Every clock pulse has a certain rise & fall time which is very small as compared to the period of the clock but cannot be neglected when measuring the power dissipation in the system. At certain point of clock transition, both NMOS and PMOS are conducting simultaneously, creating a short circuit path between VDD and ground. Therefore, comparatively large amount of current flows for a very short period of time through that path causing short circuit power dissipation which occurs at every clock transition [3].

Fig. 1: Schematic of a CMOS Inverter

In clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation [3]. Local clocks that are enabled using conditionallyare called gated clocks, because a signal from the environment is used to gate the global clock signal [2]. Average power dissipated in a digital circuit is given as P average is the average power dissipation, P dynamic is the dynamic power dissipation due to switching of transistors, P short-circuit is the short-circuit current power dissipation when there is a direct current path from power supply down to ground , P leakage is the power dissipation due to leakage currents, P static and is the static power dissipation.

Power consumed in digital circuits is given below.
1. Static power
2. Dynamic power.

1. Static Power

Static power is the power dissipated by a gate when it is inactive or idle. Ideally, CMOS (Complementary Metal Oxide Semiconductor) circuits dissipate no power since in the steady state there is no direct path from Vdd to ground.

2. Dynamic Power

Dynamic power is the power dissipated during active state due to switching activity of input signal. In other words, dynamic power dissipation is caused by the charging and discharging. Dynamic power dissipation in a circuit is given as

$$PD = \alpha C_L VDD^2 f$$

Where α is the switching activity, f is the operation frequency, CL is the load capacitance, VDD is the supply voltage.

- **CLOCK GATING TECHNIQUE**

Clock-Gating [8] is the most common register transfer level (RTL) optimization for reducing dynamic power. In clock gating method, clock is applied only to those modules that are working at that instant. Clock-gating support adds additional logic to the existing synchronous circuit [9] to prune the clock tree, thus disabling the portions of the circuitry that are not in use. By adopting the clock-gating approach, power dissipation can be reduced significantly, lowering not only the switching activity at the function unit level, but also the switched capacitive load on the clock distribution network. Here the clock gating [10] is implemented using AND gates. Fig. 1 shows the schematic of a latch element. A significant amount of power is consumed during charge/discharge cycle of the cumulative gate capacitance Cg [11] of the latch when the clock is fed directly (Fig. 1(a)) and there is no change in the clock cycle. Fig. 1(b) shows the latch with gated clock. By gating the clock, charge/discharge of Cg can be affected only when there is change in the clock cycle thus saving power.

PROBLEMS IN PREVIOUS TECHNIQUES

• In AND gate clock gating we have outputcorrectness problem due to glitches and hazards.
• In NOR gate clock gating we have outputcorrectness problem due to glitches and hazards.
• In Latch based AND gate clock gatingdesign hazards problem is removed but glitchesproblem still exists.
• In Latch based NOR gate clock gatinghazards problem is removed but glitchesproblem still exists.
• In MUX based clock gating requires anexpensive MUX per bit and consumes morepower and hardware.

- **Clock Enable Johnson Counter Design**

Design The conventional Johnson counter design contains many unwanted clock transitions which results in larger power dissipation. From the data sequence of Johnson counter as shown in Table I, it can be observed that each flip flop output changes only at 2 clock pulses in one complete cycle (8 clock pulses).So instead of providing 8 clock pulses, only 2 clock pulses for each flip flop are required to be generated which is possible using a proper clock management system where clock pulse sequences are generated only when data switching occurs and ineffective clock transitions are eliminated from the system.

Table 1: Truth Table of 4-Bit Johnson Counter

APPLICATIONS OF GATED ENABLE

1- All sequential circuit.
2- Memory processing
3- Registers & counters.
4- Data processing.
5- Arithmetic and logic units.

- **Result**

The dynamic power reduction by clock Enable technique is verified on 4-bit counter. The results shows that a significant change in dynamic power. Figure 2 shows the input voltage, current drawn; dynamic and static power drawn and total power drawn for 4 bit counter with clock enable applied. Figure 3 shows same result using without clock enable.

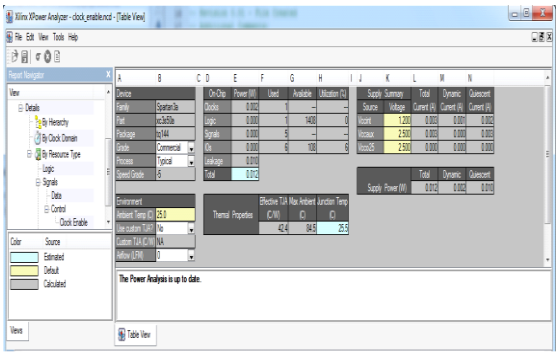

Fig 2 4 bit counter with Enable

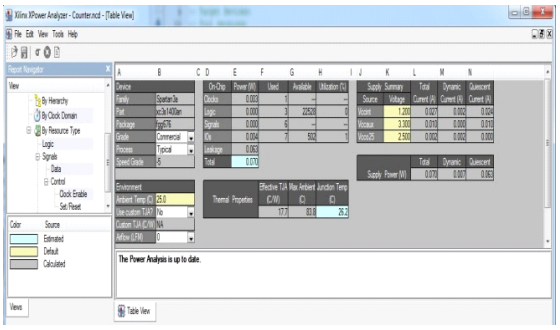

Fig 3 4 bit counter without clock Enable

III. CONCLUSION

A 4-bit Johnson counter implemented using pulse-triggered flip flop & GDI based clock enable system has been presented. The simulation results verify a power reduction upto 28.57% as compared to conventional design. The power dissipation of proposed design 12mW, pulse-triggered flip flop used in the proposed design can save power up to 28.57% as compared to the Conventional counter. The techniques used in the proposed system can be

extended to any sequential circuit design where power minimization is an important constraint.

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