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A Design of Sigma-Delta ADC Using OTA

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ABSTRACT
Sigma-Delta Analog-to-Digital converter (ADC), is widely used in portable electronic products. An operational transconductance amplifier (OTA) is one of the most important components of ADC. This paper presents a new design of two stages OTA. The design incorporates Sleep insertion technique and leakage feedback current approach for improving design parameters such as gain, and power as compared to earlier work. The design is simulated in 0.18µm CMOS technology with supply voltage 1.8V.
Keywords: ADC, OTA, Sleep insertion Technique, Leakage feedback approach.

I. INTRODUCTION

Modern VLSI devices demands for excessive information value with low energy consumption and needless speed. The key additives in the wireless receiver is the ADC, it is far way a margin in the middle of analog and digital design.

Operational Transconductance Amplifier

The OTA is a basic building blocks found in many analog devices such as data converter's (ADC &DAC). The OTA is a Transconductance device in which the input voltage controls the output current, it means that OTA is a voltage controlled current source whereas the op-amps are voltage controlled voltage source. An OTA is basically an opamp without output buffer, so it can only drive loads.

Analog-to-digital converter

ADC is a fundamental block in mixed-signal VLSI circuits. The rapid growth of mobile electronic systems increases the demand for developing low-cost and low-power circuit technique with high performance. Sigma delta (ΣΔ) modulators are one of the preferred architectures for high resolution converters. Power consumption and area are the key parameters for a sigma delta modulator these parameters cannot be changed once an ADC is designed. While it can operate at higher speed and will consume less power when operating at a lower resolution.

II. PROPOSED OTA ARCHITECTURE

OTA is one of the basic building blocks of any analog circuit. OTA is in existence since very long time, this is not a recent technology. An OTA has all the characteristics of an operational voltage amplifier except that the output impedance ideally approaches infinity rather than zero. OTA is used to form the R- C integrator, which is the key block of ΣΔ modulator. An Two-Stage OTA topology with rail to-rail output swing is adopted for low voltage, low power designs. Two stage OTA is a configuration two stages are used. One of them provides high gain followed by second stage which provides high voltage swing. This modification increases the gain compared to single stage OTA. But increases complexity of design, Hence reduce the speed as compared to single stage amplifier[2].

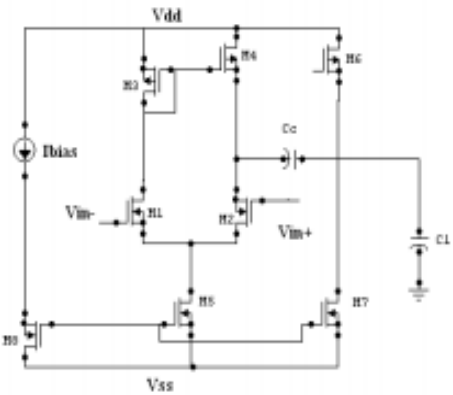

Fig 1: Two stage OTA

III. BLOCK DIAGRAM OF ADC ARCHITECTURE

Fig 2. Shows The block diagram of a first order ΣΔ modulator which consists of a integrator, a comparator, which acts as an ADC and 1-bit DAC, which is placed in the feedback loop. The name first order is derived from the information that there is only one integrator in the circuit, placed in the forward path. When the output of the integrator is positive, the comparator feeds back a positive reference signal that is subtracted from the input

signal of the integrator. Similarly, when the integrator output is negative, the comparator feeds back a negative signal that is added to the incoming signal

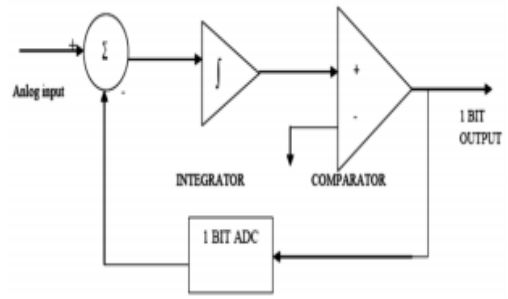

Fig 2. 1 bit Sigma-delta Modulator.

IV. METHODOLOGY

sleep insertion technique and Leakage feedback approach is to reduce tha power consumption, leakage current and to increase the circuit performance.

1) Sleep Insertion Technique

Sleep approach is used to rail off the circuit from Vdd to ground, so insert a PMOS transistor above pull up network and Vdd and NMOS transistor below pull down Network and GND. During standby mode a sleep transistor turns off turn off and rail from Vdd and reduces the leakage current. During active mode ON the sleep transistor and direct connection of circuit with Vdd, so increase the performance of the circuit and Reduces the leakage power.

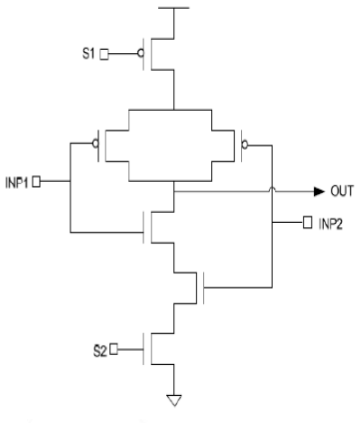

Fig4. sleep insertion technique

2) Leakage Feedback Approach

Leakage reduction technique is leakage feedback approach; In this approach two parallel PMOS transistor above pull up network and Vdd. To provide the inverting output of the circuit connects a inverter at the output, an inverter provides the proper logic feedback to both pull down NMOS(S') and pull up PMOS(S) sleep transistor. This two transistor enhance the circuit performance and maintain the proper logic of the circuit during standby mode.

In standby mode one of the transistor of parallel sleep transistor turn off both NMOS and PMOS, the output of the circuit is pass through inverter which keep ON one of the sleep transistor which is connected parallel by providing the proper feedback approach. Hence circuit is active in standby mode, the various leakage current which flow during standby mode and increase the performance of the circuit

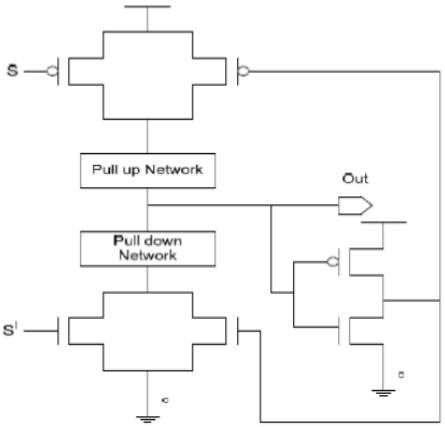

Fig.5: leakage feedback current approach

V.SIMULATION RESULT AND DISSCUSSION

1) DESIGN OF COMPARATOR

Comparator is one of the fundamental building blocks in most analog to digital converters (ADCs). High speed flash ADCs, require high speed, low power and small chip area. Comparators are known as 1-bit analog to digital converter and hence they are mostly used in large abundance in A/D converter [4]. A comparator is same as that like of an operational amplifier in which they have two inputs (inverting and non-inverting) and an output. The function of a CMOS comparator is to compare an input signal with a reference signal which produces a binary output signal [4].

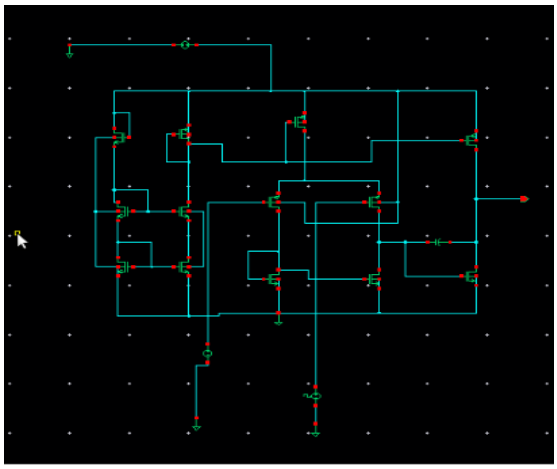

Fig.6: Schematic view of comparator

Simulation Results

From the analysis, the Gain of the design is 3.8 dB and the static and total power consumption of design is 155.5µW and 103.1µW .

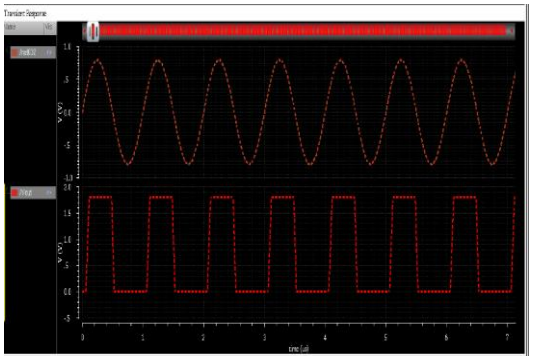

Fig.7: Result of comparator

2) DESIGN OF 1-BIT DAC

This circuit contains two transmission gates and an inverter, two reference voltages. For particular case, +Vref is taken as +1.8 V and -Vref is taken as –1.8V. And the operation of the circuit can be explained by two cases.

If the input is 1, then output of the DAC is +Vref and if the input is 0, then DAC output is -Vref. This logic is implemented using a 2×1 multiplexer circuit. Output of the comparator act as the select lines of the multiplexer to select the 1-bit digital input . Transmission gates are controlled by the output of comparator and its inverted output is obtained from the inverter [1].

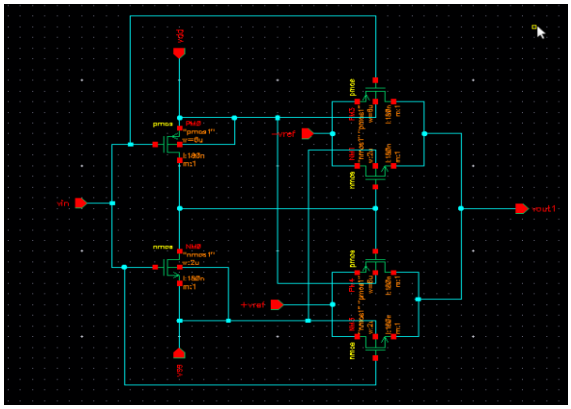

Fig.8: Schematic view of 1-bitDAC

Simulation Results

From the analysis, the Gain of the design is 7.75dB and the static and total power consumption of design is 2.343µW and 2.726µW.

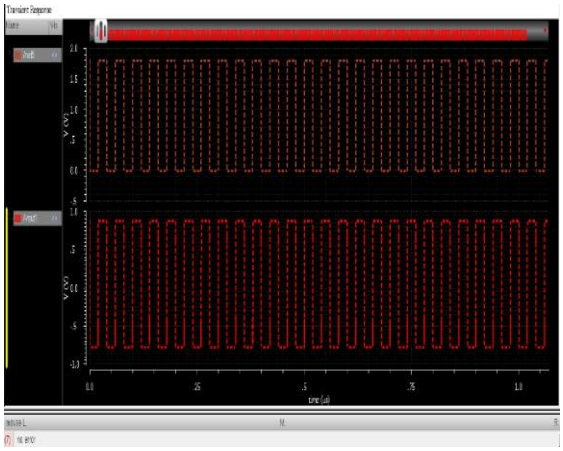

Fig.9: Result of 1-bit DAC

3) DESIGN OF TWO STAGE OTA

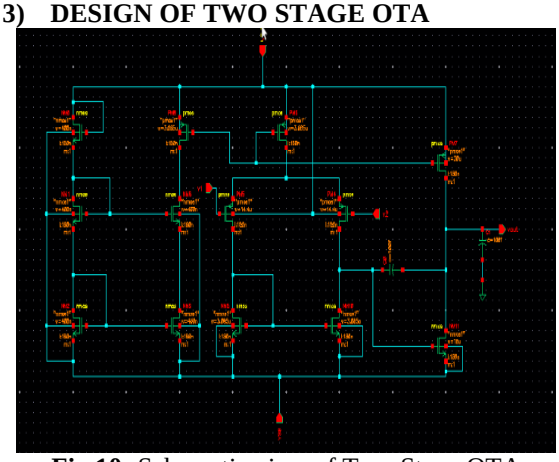

Fig.10: Schematic view of Two-Stage OTA

Simulation Results

From the analysis, the Gain of the design is 9.6dB and the static and total power consumption of design is 15.16mW.

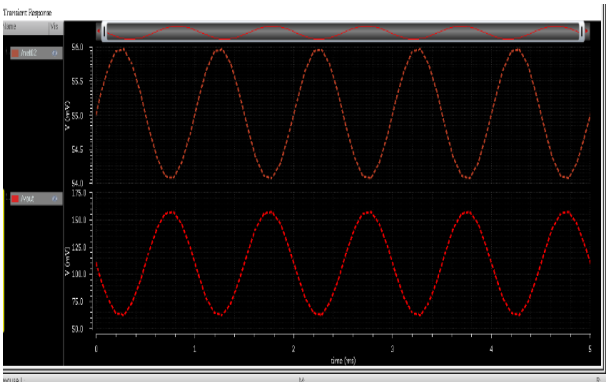

Fig.11: Result of Two-Stage OTA

4) DESIGN OF OP-AMP

An operational amplifier (often op-amp) is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output[11].

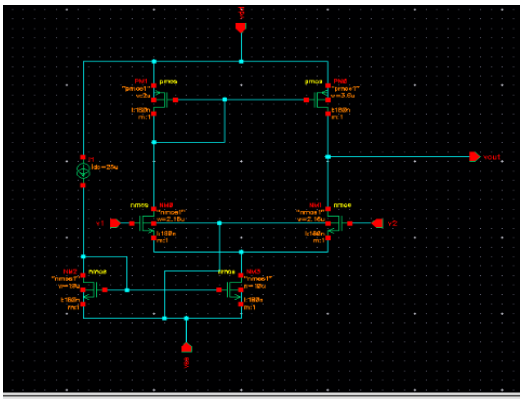

Fig 12 : Schematic view of Op-amp

Simulation Results

From the analysis, the Gain of the design is 2.9dB and the static and total power consumption of design is 118µW and 118.06µW.

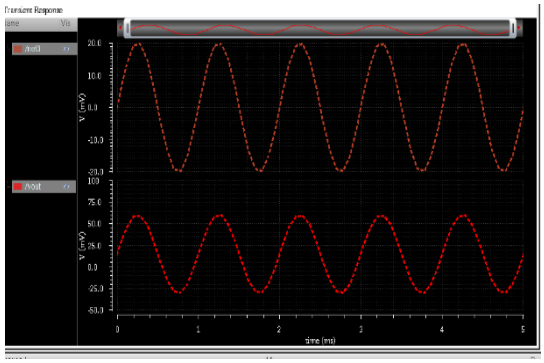

Fig.13: Result of Op-amp

5) OP-AMP INTEGRATOR CIRCUIT

By replacing this feedback resistance with a capacitor we now have an R-C Network connected across the operational amplifiers feedback path producing another type of operational amplifier circuit commonly called an Op-amp integrator circuit as shown in below figure[11].

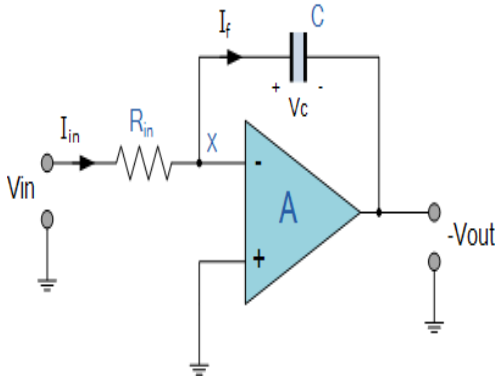

Fig.14: Op-Amp

Op-amp Integrator is an operational amplifier circuit that performs the mathematical operation of Integration**,** that is we can cause the output to respond to changes in the input voltage over time as the op-amp integrator produces an output voltage which is proportional to the integral of the input voltage.

6) DESIGN OF ADC

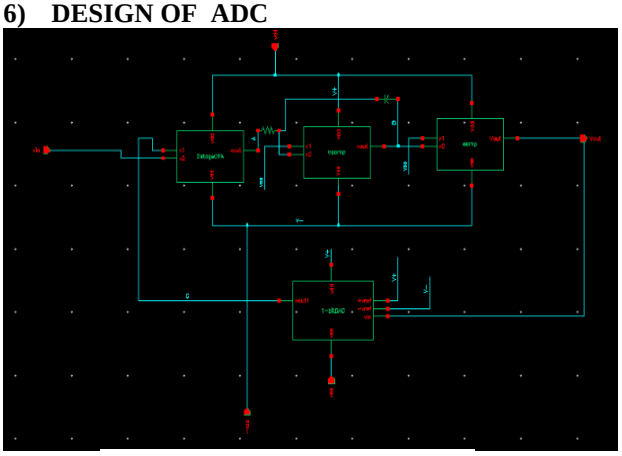

Fig 15 :Schematic of view of ADC

Simulation Results

From the analysis, the Gain of the design is 6.9dB and the static and total power consumption of this ADC design 19.14mW and 19.87mW.

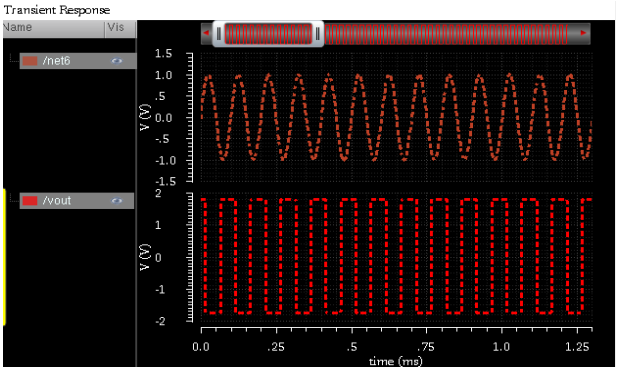

Fig 16: Results of ADC

7) DESIGN OF ADC BY SLEEP INSERTION TECHNIQUE

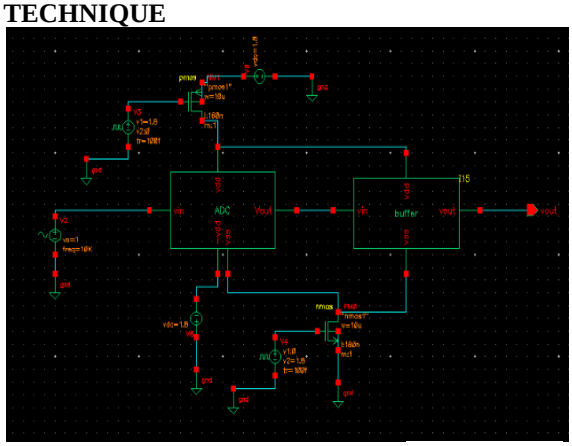

Fig 17: Schematic View of ADC by sleep Insertion Technique

Simulation Results

From the analysis, the Gain of the design is 6.9dB , and static and Total power consumed by OTA is 655.4µW .

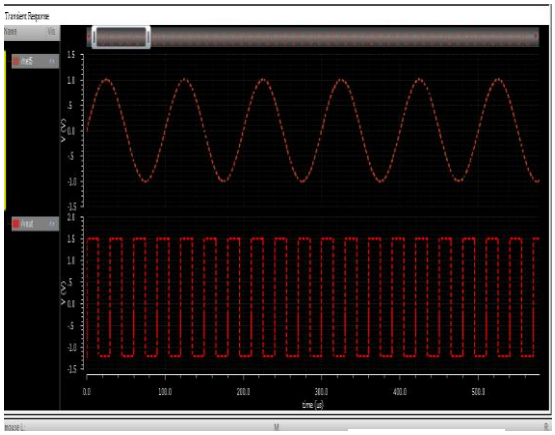

Fig 18: Result of ADC by sleep Insertion Technique

8) DESIGN OF ADC BY LEAKAGE FEEDBACK APPROACH

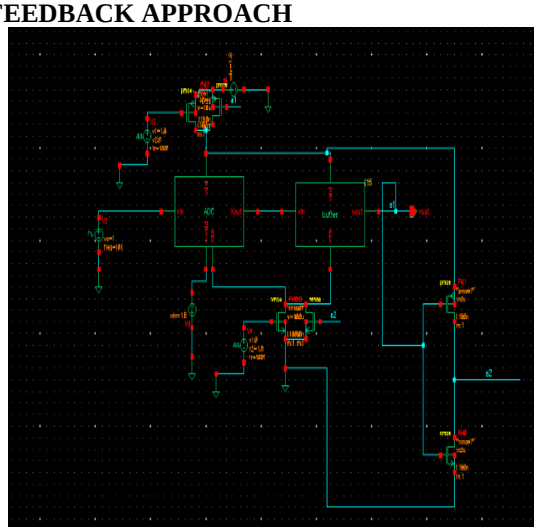

Fig19: Schematic view of ADC by Leakage Feedback Approach

Simulation Results

From the analysis, the Gain of the design is 6.9dB, and static and total power consumed by OTA is 11.38mW.

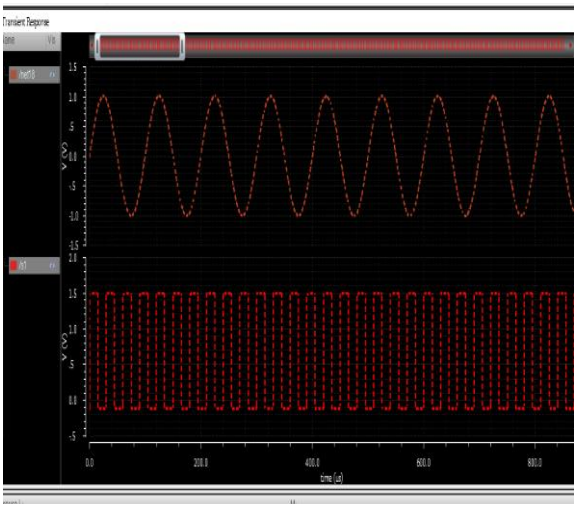

Fig 20: Schematic view of ADC by Leakage Feedback Approach

COMPARITION TABLE

DESIGN	STATIC POWER (W)	TOTAL POWER (W)	GAIN
TWO-STAGE OTA	15.16m	15.16m	9.6dB
OP-AMP	118µ	118.06µ	2.9dB
1-BIT DAC	2.343µ	2.726µ	7.75dB
COMPARATOR	155.5µ	103.1µ	3.8dB
ADC	19.14m	19.87m	6.9dB
ADC BY SLEEP INSERTION TECHNIQUE	655.4µ	655.4µ	6.9dB
ADC BY LEAKAGE FEEBBACCURRENT	11.38m	11.38m	6.9dB

V. CONCLUSION

In this work, two- stage OTA is designed using a sleep insertion technique and leakage feedback approach. The design is carried out in 0.18µm CMOS technology with supply voltage is 1.8V. The obtained Gain of the design with sleep insertion technique is 6.9dB, and total power consumed is 655.4µW. The obtained Gain of the design with leakage feedback current approach is 6.9dB , total power consumed is 11.38mW. The designed OTA is incorporated in Sigma-Delta ADCs for better performance.

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[11] **"**Operational Amplifiers (Op Amps)", Professor Katherine Candler Notes courtesy of Professor Sarah Harris.t, UTU, Dehradun, UK India2