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A Review of Different Methods for Booth Multiplier

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ABSTRACT
In this review paper, different type of implementation of Booth multiplier has been studied. Multipliers has great importance in digital signal processor, so designing a high-speed multiplier is the need of the hour. Advantages of using modified booth multiplier algorithm is that the number of partial product is reduced. Different types of addition algorithms are also discussed which are used for addition operation of multiplier.
Keyword -booth multiplier, modified booth multiplier, radix-8, fixed-width.

I. INTRODUCTION

In many digital signals processing (DSP) applications computer arithmetic is extensively used. As compare to the adders and subtractors multiplier are more complex, so the multiplier speed usually resolves the operating speed of a DSP system. With other considerations such as Hardware complexity, power dissipation of a design and delay the high precision is often looked as a strict requirement. Some applications such as media processing, recognition and data mining are error-tolerant, so an approximate arithmetic unit can be employed. With the accumulation of partial products, the design of an approximate multiplier is usually deals, in its operation which is bottleneck. To reduce the delay and hardware overhead the truncation of the lower part of the partial products is a simple approximation scheme; to as fixed-width multiplier design such a scheme is referred [2]. Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation.

II. LITRATURE SURVEY

Tao Luo et al. [1] In this paper, present an in-memory Booth multiplier based on racetrack memory to alleviate this problem. As the building block of our multiplier, a racetrack memory based adder is proposed, which saves 56.3% power compared with the state-of-the-art magnetic adder. Integrated with the storage element, our proposed multiplier shows great efficiency in area, power and scalability.

Honglan Jiang et al. [2] The Booth multiplier has been widely used for high performance signed multiplication by encoding and thereby reducing the number ofpartial products. A multiplier using the radix-4(or modified Booth) algorithm is very efficient due to the ease of partial product generation, whereas the radix-8 Booth multiplier is slow due to the complexity of generating the odd multiples of the multiplicand. In this paper, this issue is alleviated by the application of approximate designs. An approximate 2-bit adder is deliberately designed for calculating the sum of 1× and 2× of a binary number. This adder requires a small area, a low power and a short critical path delay. Subsequently, the 2-bit adder is employed to implement the less significant section of a recoding adder for generating the triple multiplicand with no carry propagation. In the pursuit of a trade-off between accuracy and power consumption, two signed 16×16-bit approximate radix-8 Booth multipliers are designed using the approximate recoding adder with and without the truncation of many less significant bits in the partial products. The proposed approximate multipliers are faster and more power efficient than the accurate Booth multiplier; moreover, the multiplier with 15-bit truncation achieves the best overall performance in terms of hardware and accuracy when compared to other approximate Booth multiplier designs. Finally, the approximate multipliers are applied to the design of a low-pass FIR filter and they show better performance than other approximate Booth multipliers.

Jiun-Ping Wang et al. [3] This paper presents the design of high-accuracy fixed-width modified Booth multipliers. To reduce the truncation error, firstly slightly modify the partial product matrix of Booth multiplication and then derive an effective error compensation function that makes the error distribution be more symmetric to and centralized in the error equal to zero, leading the fixed-width modified Booth multiplier to very small mean and mean-square errors.In addition, a simple compensation circuit mainly composed of the simplified sorting network is also proposed. Furthermore, experimental results on two real-life applications also demonstrate that the proposed fixed-width multipliers can improve the average peak signal-to-noise ratio of output images by at least 2.0 dB and 1.1 dB, respectively.

Razaidi Hussin et al. [4] in this paper, present the design of an efficient multiplication unit. This multiplier architecture is based on Radix 4 Booth multiplier. The first is to modify the Wen-Chang's Modified Booth Encoder (MBE) since it is the fastest scheme to generate a partial product. However, when implementing this MBE with the Simplified Sign Extension (SSE) method, the multiplication's output is incorrect. The 2nd part is to improve the delay in the 4:2 compressor circuits. The redesigned 4:2 compressor reduced the delay of the Carry signal. This modification has been made by rearranging the Boolean equation of the Carry signal. This architecture has been designed using Quartus II. The Gajski rule has been adopted to estimate the delay and size of the circuit. The total transistor count for this new multiplier is being a slightly bigger. This is due to the new MBE which is uses more transistor.However, in performance speed, this efficiency multiplier is quite good. The propagation delay is reduced by about 2% – 7% from other designers.

Chung-Yi Li et al. [5] In this paper, a probabilistic estimation bias (PEB) circuit for a fixed-width two's-complement Booth multiplier is proposed. The proposed PEB circuit is derived from theoretical computation, instead of exhaustive simulations and heuristic compensation strategies that tend to introduce curve-fitting errors and exponential-grown simulation time. Consequently, the proposed PEB circuit provides a smaller area and a lower truncation error compared with existing works. Implemented in an 8 × 8 2-D discrete cosine transform (DCT) core, the DCT core using the proposed PEB Booth multiplier improves the peak signal-to-noise ratio by 17 dB with only a 2% area penalty compared with the direct-truncated method.

A.S.Prabhu et al. [6] In this paper, booth multipliers are proposed for reducing the power of the multiplier circuit. The multiplier circuit is designed with conventional full adder. The schematics are drawn and simulated. The power results are thus compared for the different inputs. The result shows that average power consumed by the multiplier. When using booth multiplier technique is less compared to column bypass technique and array multiplier. Booth multiplier consumes comparatively less power and hence multiplier with booth recoding unit is designed for low power consumption.

Hsin-Lei Lin et al. [7] This paper presents a novel radix-4 Booth multiplier. A conventional Booth multiplier consists of the Booth encoder, the partial-product summation tree, and the canypropagate adder. Different schemes are addressed to improve the area and circuit speed effectively. A novel modified Booth encodeddecoder is proposed and the summation column is compressed by the proposed MFAr. The proposed design is simulated by Synopsys and Apollo. It results 20% area reduction, 17%&-24% power decrease, and 15% reduction of the delay time of the critical path.

Hwang-Cherng Chow et al. [8] In this paper, a new MBE (modified Booth encoding) recoder, and a new MBE decoder are proposed in CMOS transistor level' to improve the performance of traditional multipliers. The proposed pipelined Booth multiplier can reduce the delay time of critical path by levelizing the complex gate in the MBE decoder. As a result, MBE decoder is never the speed bottleneck of a pipelined booth multiplier, and the speed of the MBE decoder can be improved up to 66.3 percent. Finally, a low voltage, high speed pipelined glitch-free Booth multiplier architecture is presented at lGhz in TSMC 0.35um process with a power consumption of only 100.52mw.

Justin Hensley et al. [9] This paper makes the following contributions. First, a novel counter flow organization is introduced, in which the data bits' flow in one direction, and the Booth commands piggyback on the acknowledgments flowing in the opposite direction. Second, the arithmetic and shifter units are merged together to obtain significant improvement in area, energy as well as speed. Third, design performs overlapped execution of multiple iterations of the Booth algorithm. Finally, the design is quite modular, which allows scaling to arbitrary operand widths, without gate resizing or cycle time overheads.

K. J. Cho et al. [10] In this paper, an efficient fixed-width modified Booth multiplier design method is presented. To efficiently compensate for the quantization error with reduced hardware complexity, Booth encoder outputs (not the

multiplier coefficients) are used for the generation of the compensation bias. Also, the truncated bits are divided into two groups (major group and minor group) depending upon their effects on the quantization error. Then, different error compensation methods are applied to each group. Simulation results show that significant reduction in the truncation error can be achieved by the proposed method compared with the fixed width modified Booth multiplier.

III. BOOTH MULTIPLIER

It is a powerful algorithm for signed-number multiplication, which treats both positive and negative numbers uniformly. For the standard add-shift operation, each multiplier bit generates one multiple of the multiplicand to be added to the partial product. If the multiplier is very large, then many multiplicands must be added. In this case, the delay of multiplier is determined mainly by the number of additions to be performed. If there is a way to reduce the number of the additions, the performance will get better. Booth multiplication is a technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied. It is the standard technique used in chip design, and provides significant improvements over the "long multiplication" technique.

IV. MODIFIED BOOTH MULTIPLIER

There are several Multiplier Architectures which has come into existence over recent years. Multiplier is one of the key hardware blocks in Digital Signal Processors(DSP)and microprocessors. Multiplication operations are so considerable in-order to slow down the system operations. In this present years, multiplier architectures are developed by considering minimal operational speed, area and power. An efficient Multiplier can improve the performance of Digital Signal Processors in case of filtering, spectral analysis. The above multiplier architecture can be divided into two stages. In the first stage the Partial Products are formed by the Booth encoder and Partial Product Generator(PPG). In the second stage the partial products obtained in the above are merged to form the results. Instead of adders we can also use compressors to reduce the carry propagation delay. When the adders alone seen, we can have the adder circuits such as Carry Propagation adder, carry save adders. Prior to Multiplication, we require the two operands, a Multiplier and a Multiplicand which are to be stored in the buffer. In normal Binary Multipliers, the Partial Products are generated by performing AND operation(multiplying) the bits of Multiplier with the Multiplicand bits. Thus, the array of AND gates are used in normal binary multipliers for partial products generation. Here when the multiplier bit is zero then a row of zeros is summed to previous partial product. when the multiplier bit is one then the multiplicand is added once to the previous partial products with a position shift towards left.

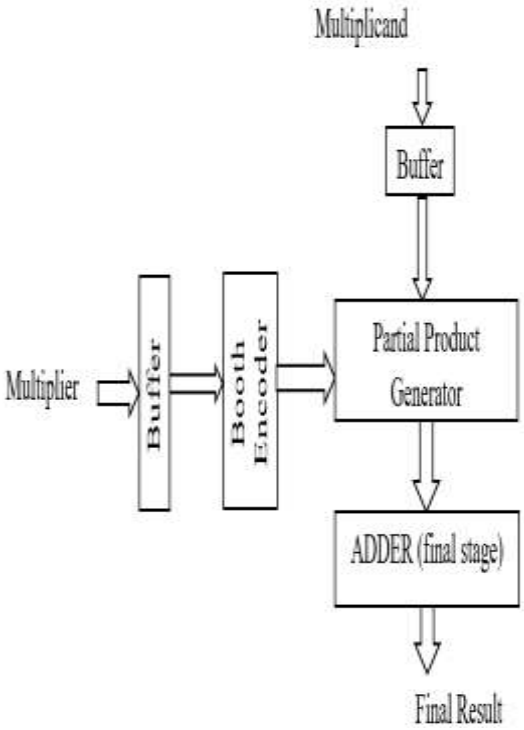

Fig.1: Modified Booth Multiplier Architecture

V. CONCLUSION

This paper presents the design of review of different methods with high-accuracy fixed-width modified Booth multipliers. To reduce the truncation error, firstly slightly modify the partial product matrix of Booth multiplication and then derive an effective error compensation function that makes the error distribution be more symmetric to and centralized in the error equal to zero, leading the fixed-width modified Booth multiplier to very small mean and mean-square errors.

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