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High Performance and Low power VLSI CMOS Circuit Designs using ONOFIC Approach

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ABSTRACT
Leakage power dissipation a major concern for scaling down portable devices. Improving high performance with reduced power consumption and chip area are the main constraint for designing VLSI CMOS circuits. In this paper, high performance and low power ONOFIC approach for VLSI CMOS circuits have been implemented. Mostly the concentrated part in deep sub micron regime is the power dissipation. Many techniques have been proposed for reducing leakage current in deep sub micron but with some limitations they are not suitable for actual requirements. Here we discussed two techniques named LECTOR & ONOFIC. The proposed On/Off Logic (ONOFIC) serves the needs for deep sub micron with its reduced power dissipation and increased performance in VLSI circuits. Thus the proposed ONOFIC approach results have been compared with the LECTOR technique and observed that the proposed technique improves the performance and reduce the power dissipation.

Keywords: ONOFIC, Deep sub micron, LECTOR, Leakage current.

I. INTRODUCTION

The design of low power circuits mainly focus on performance, power dissipation and chip area. The concentrated part in VLSI CMOS circuits is deep sub micron regime. The constraint in deep sub micron is to reduce the device dimensions leads to decrease in chip area. Supply voltage plays an important role in electronic devices to control the power consumption. By reducing supply voltage and threshold voltage we can retains the performance. Introducing new lower level technologies in integrated circuits leads to increase in power dissipation. As the technology scaling down the leakage power dissipation goes up. Several technologies have been implemented to reducing the leakage power dissipation.

Kao and chandrakasan used power gating with Multi-Threshold transistors. This is the most efficient way to lowering the leakage power dissipation of a VLSI circuits in the standby state is to turn off its supply voltage. However this technique cannot be used in sequential circuits and memory cells, as it would result in loss of data stored. Self-bias transistor (SBT) to minimize sub-threshold leakage currents in static and dynamic circuits**.** Which acts as smart switch by virtually power gating either pull-up or pull-down logic, and causes a considerable reduction in leakage currents in both active and standby modes. S.Narendra et al. discovered that by connecting off state transistors in series can reduce the leakage power. In this paper we are discussing Leakage control transistor (LCT) technique to reduce the power consumption and power dissipation. Moreover, for designing high performance and low power CMOS circuits a new method is implemented which is On/Off logic (ONOFIC) approach. Section II briefly describes Power dissipation in CMOS designs. Section III describes LECTOR technique to reduce leakage power. Section IV describes our proposed technique which is ONOFIC to reduce the leakage power. Section V describes results. Section VI is about conclusion.

II. POWER DISSIPATION

Power dissipation is a major problem in microelectronic circuit designing the, exclusively in wireless mobile applications and gadgets computing elements. This paper deals with the reduction and optimization techniques for leakage power dissipation in VLSI CMOS circuits. The causes of power dissipation in CMOS circuits are described by the given below equation (1).

$$P=1/2.C.VDD2.\ f.\ N + I\ leak\ .VDD + QSC\ .VDD.\ f\ .N \quad (1)$$

Where P signifies the total power dissipated, VDD represents the supply voltage, and f represents the operating frequency. The first term denotes the power required for charging and discharging the circuit

nodes. C is the node Capacitance. The factor N is the switching action which gives the number of gate transitions per clock cycle at the output. The second term in Equation 1 signifies the static power dissipation due to the leakage current I leak. The third term in Equation 1 signifies power dissipation. The term QSC shows the amount of charge carried during each transition by the short circuit current in the circuit.

III. LECTOR TECHNIQUE

LECTOR technique was proposed by the authors N. Hachette and N. Ranganathan. In this technique two leakage control transistors are used to control leakage current. These LCT transistors are connected in such a manner so that one of the LCT transistors will be in off state for any input signal. Further, the gate of p – channel and n – channel MOSFET is connected to the drain terminal of n – channel and p – channel MOSFET respectively. The generalized structure for leakage control gates is shown in figure. 1. This technique gives an advantage of reducing the leakage current in a path from VDD to ground. The connection between pull – up and pull – down is connected with leakage control transistors. By breaking the path between pull – up and pull down networks reduces the leakage current. The conventional NAND design and NAND design using LECTOR technique also shown below respectively in figure .2 and figure .3. Simultaneously the conventional NOR design and NOR design using LECTOR technique also shown below respectively in figure .4 and figure .5.

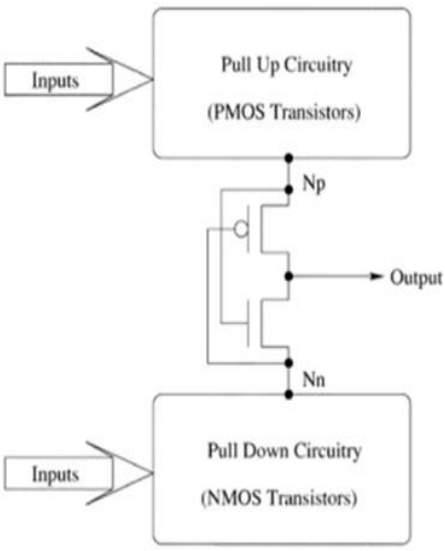

Fig.1. Generalized structure for leakage control gates

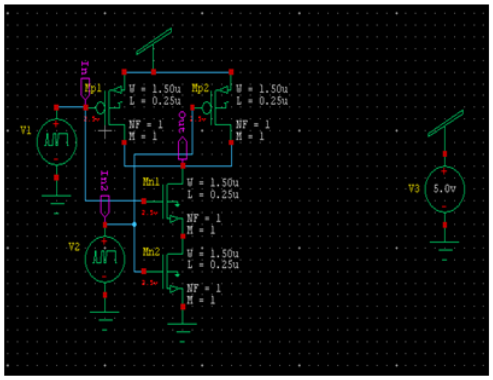

Fig.2. Coventional NAND design

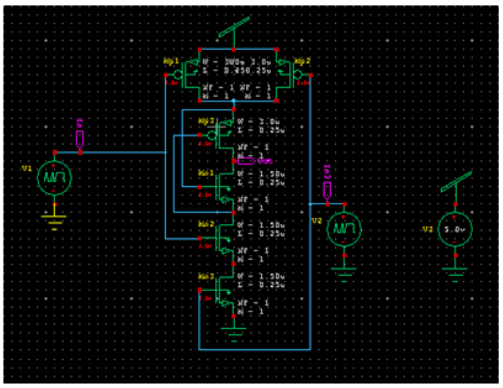

Fig.3.NAND design using LECTOR

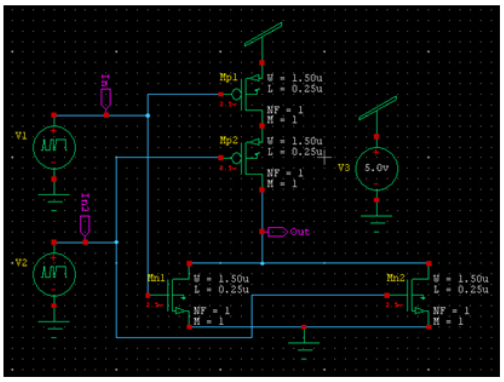

Fig.4. Conventional NOR design

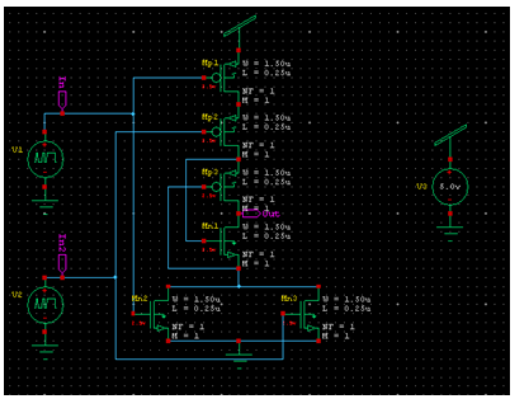

Fig.5. NOR design using LETOR

IV. PROPOSED ONOFIC

The proposed On/Off logic (ONOFIC) approach reduces the leakage current and power with single threshold voltage level approach. This technique efficiently reduces the leakage current in both active and standby mode of logic circuit. Same as LECTOR technique the ONOFIC approach also introduces an extra logic between pull-up and pull-down networks for leakage reduction. This additional introduced circuit is called On/Off logic (ONOFIC) circuit. This proposed approach contains one PMOS and one NMOS transistor. Due to maintaining either on or off condition for any output logic level this technique is known as ONOFIC. The connection of ONOFIC is shown in figure.4. This technique provides the maximum resistance to the ONOFIC block when it is in off state and minimum resistance when it is in on state. This logic directly affects the power dissipation and propagation delay of the logic circuit.

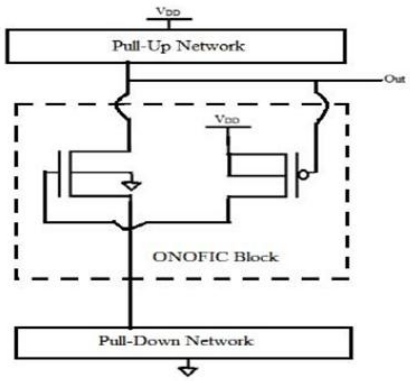

Fig.6. Schematic of ONOFIC logic

In ONOFIC block, the drain of PMOS transistor is connected to the gate of NMOS transistor and the output is connected to the gate of PMOS transistor. The drain of the pull-down network is connected to the source of NMOS transistor and PMOS source terminal is connected to VDD of the circuit. The NMOS transistor drain is connected to the output of the circuit and the substrate of NMOS transistor is connected to the ground while the substrate of PMOS transistor is connected to the VDD. The main concept of this technique is property of On/Off. The both ONOFIC transistors are in linear region when ONOFIC logic is in on condition while ONOFIC logic is in off state both the transistors are in cut-off mode. The good conducting path is obtained by turning on the ONOFIC block and it acts as a good resistance to control the leakage current when it is in off state. The proposed ONOFIC NAND design is shown in below figure .7. The proposed ONOFIC NOR design is shown in below figure .8.

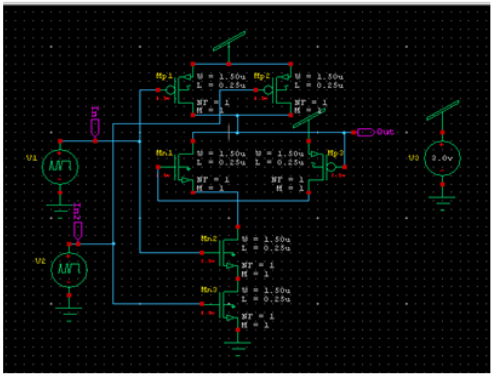

Fig.7.NAND design using ONOFIC

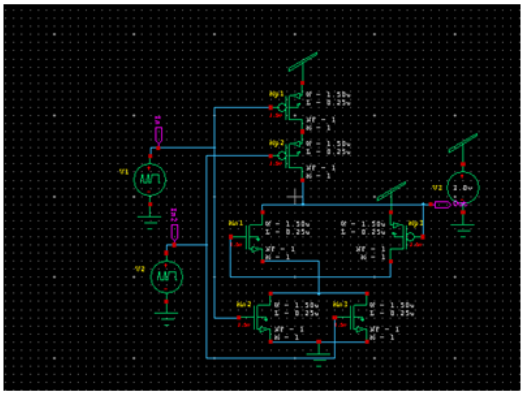

Fig.8. NOR design using ONOFIC

TABLE I The Transistor Operation Of An Onofic Cmos Inverter

Input level	PMOS	ONOFIC PMOS	ONOFIC NMOS	NMOS
Logic 0	On	Off	Off	Off
Logic 1	Off	On	On	On

From Fig.4 when compared to other circuits of the NAND design the ONOFIC technique uses the same threshold voltage throughout the entire block which can improve the performance of the logic circuits. From the Fig.3 shows the NAND design using LECTOR technique also uses the same threshold voltage throughout the circuit block. The slope of the CMOS inverter circuit with any input combinations is given in Equation (1),

$$\text{Slope} = \eth V_{out}/\eth V_{in} = \eth (I_{out}R_{out})/\eth V_{in}; \quad (2)$$

$$I_{out} = k/2\,(VT)^2\, e^{(Vin-Vth)/VT}\,(1- e^{-Vout/VT}); \quad (3)$$

Here k is device process parameter, VT is voltage temperature. Where Vth is device threshold voltage and which depends on doping densities of the material with material's quality factor, the flat voltage and charge storing capacitances. From the Equations (2) and (3) observed that the large slope is occurred due to large I out current which leads to large static power dissipation and hence LECTOR technique has low static power dissipation when compared to conventional and ONOFIC approach. Equation (3) gives the propagation delay,

$$Tp = (Rout\Delta Vout)/Iout; \quad (4)$$

Where, Rout is the sum of loads of resistive and capacitive of the CMOS circuit. ONOFIC and conventional circuits have less propagation delay when compared to LECTOR technique due to large Iout as observed from Equation (4). Due to less propagation delay the output values obtained quicker when input combination applied.

In ONOFIC block, the operation of NMOS transistor is controlled by the PMOS transistor. ONOFIC NMOS transistor mode is depends upon the output logic. The concept of stacking provides the ONOFIC circuit for controlling leakage current with maximum resistance when it is in OFF state and minimum resistance when it is in ON state.

The minimum propagation delay is obtained due to fast performance of turning-off and turning on of a PMOS transistor when compared to other techniques.

V. RESULTS

Power consumption and Propagation delay of basic CMOS designs are tabulated below as shown in TABLE II. Here, the basic CMOS designs are simulated in tanner tools. In the given table we gave the comparison among conventional circuits of different logic gates, logic gates using LECTOR technique and logic gates using our proposed ONOFIC approach. We also showed the graphs of power consumption and delay for NAND designs in the figure.9 and figure.10. Simultaneously NOR designs in the figure.11. and figure.12.

TABLE II: The Power Consumption (W) And Propagation Delay (Ns)

CMOS DESIGN	DELAY	POWER
INVERTER	-102.2930n	6.385162e-005w
LECTOR INVERTER	-101.7726n	5.345801e-005w
ONOFIC INVERTER	-102.3982n	3.982539e-006w
NAND	29.8060n	1.232135e-004w
LECTOR NAND	59.8060n	8.846303e-005w
ONOFIC NAND	-10.4715n	3.424948e-005w
NOR	9.5988n	6.783585e-005w
LECTOR NOR	9.6126n	6.624054e-005w
ONOFIC NOR	9.5340n	1.476662e-005w

TABLE II shows the delay and power consumption of various CMOS circuit designs. Here the comparison is among conventional CMOS circuits, circuits using LECTOR and circuits using ONOFIC. It is found that the delay and power consumption of ONOFIC decreases when compared to conventional circuit results. It is also seen that LECTOR based (LCT) circuits have less power consumption but more delay as compared to conventional design as shown in below graphs. As LECTOR technique consumes less power compared to conventional but has more delay so we went to proposed ONOFIC approach. By observing the above table we get less delay and less power consumption compared to conventional and LECTOR. So, our proposed ONOFIC technique gives high performance compared to other techniques. It is more advantageous by using ONOFIC approach to reduce power and delay. The power and delay graphs are shown below. By comparing ONOFIC circuit designs with other conventional and LECTOR technique circuit designs ONOFIC consume less power and delay.

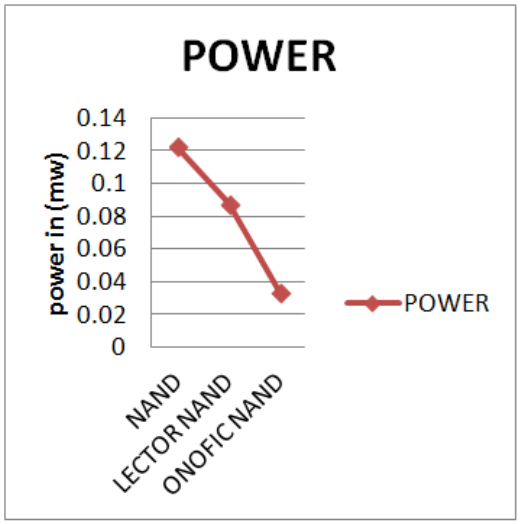

Fig.9. Power Consumption for NAND design

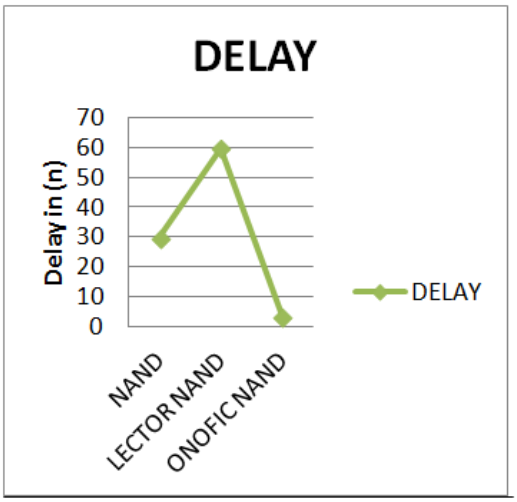

Fig.10. Delay for NAND design

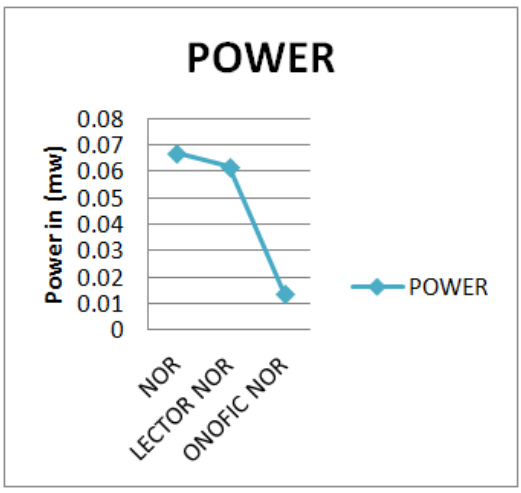

Fig.11. Power consumption for NOR design

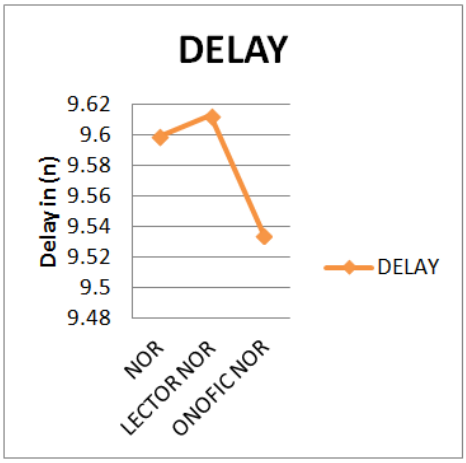

Fig.12. Delay for NOR design

VI. CONCLUSION

The problem of power dissipation is reduced for different VLSI CMOS circuits by using TANNER EDA tool. This work addresses the challenge of obtaining low power losses and efficiently uses IC's and electronic devices. Our proposed ONOFIC approach gives high performance when compared to conventional circuits, LECTOR. So, it is helpful in saving power in CMOS circuits. Hence, our proposed ONOFIC approach gives best results for saving power and gives high performance.

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