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Design of A High Speed And Low Power 4 Bit Carry Skip Adder

Khushbu Nagori[1] , Suman Nehra[1]
**(Department of Electronics and Communication Engineering, Mody University, Lakshmangarh 332311*

ABSTRACT
This paper focuses on carry skip adder (CSKA) structure that has a higher speed yet lower power consumption compared with the conventional one. The speed enhancement is achieved by applying Transmission gate logic (TG) to improve the efficiency of the conventional CSKA structure. The CMOS multiplexer in Conventional CSKA is replaced by multiplexer using transmission gate for the skip logic in proposed CSKA. The structure may be realized with transmission gate multiplexer that improves the speed and delay parameters of the adder. The simulation of this CSKA is done using TANNER EDA. Finally, a low power and high speed proposed structure is implemented, which lowers the power consumption without considerably impacting the speed. The proposed structures are assessed by comparing their speed, power, and delay parameters with those of other existing adders using a 45-nm CMOS technology for a wide range of supply voltages.
Keywords **-** Carry skip adder (CSKA); Multiplexer (2:1); Transmission gate logic;

I. INTRODUCTION

The ever-increasing demand for mobile electronic devices requires the use of power-efficient VLSI circuits. Computations in these devices need to be performed using low-power, area-efficient circuits operating at greater speed. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor. Adders are key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported in [1-5] Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage and addition to the knob of the supply voltage, one may choose between different adder structures/families for optimizing power and speed. There are many adder families with different delays, power consumptions, and area usages. Examples include ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adders (PPAs). The descriptions of each of these adder architectures along with their characteristics may be found in [6]. The RCA has the simplest structure with the smallest area and power consumption but with the worst critical path delay. In the CSLA, the speed, power consumption, and area usages are considerably larger than those of the RCA. The PPAs, which are also called carry look-ahead adders, exploit direct parallel prefix structures to generate the carry as fast as possible. There are different types of the parallel prefix algorithms that lead to different PPA structures with different performances. As an example, the Kogge–Stone adder (KSA) [7] is one of the fastest structures but results in large power consumption and area usage. It should be noted that the structure complexities of PPAs are more than those of other adder schemes.

The CSKA, which is an efficient adder in terms of power consumption and area usage. It is designed to speed up the addition operation by adding a propagation of carry bit around a portion of entire adder [7]. The critical path delay of the CSKA is much smaller than the one in the RCA, whereas its area and power consumption are similar to those of the RCA. Carry-skip adder has the advantage of short delay and high computing efficiency so causes wide attention. In addition, due to the small number of transistors, the CSKA benefits from relatively short wiring lengths as well as a regular and simple layout [8-10]. In this paper, we have implemented a complementary multiplexer as a skip logic using TANNER EDA tool for high speed and low power application of a 4 bit carry skip adder.

The growing market of portable (e.g., cellular phones, gaming consoles, etc.), battery-powered electronic systems demands microelectronic circuits design with ultralow power dissipation . As the integration, size, and complexity of the chips continue to increase, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of the computing systems which make use of those integrated circuits. In this paper circuit logic has

been changed so that power consumption can be reduced.

II. CONVENTIONAL CARRY SKIP ADDER

The conventional structure of the CSKA consists of one stage containing chain of full adders (FAs) (RCA block), AND gate, XOR gate and 2:1 multiplexer (carry skip logic). The RCA blocks are connected to each other through 2:1multiplexers, which can be placed into one or more level structures. The basic circuit layout of conventional carry skip adder (4 bit) is shown in Fig.1 and the schematic diagram of the multiplexer 2:1 is shown in Fig.2

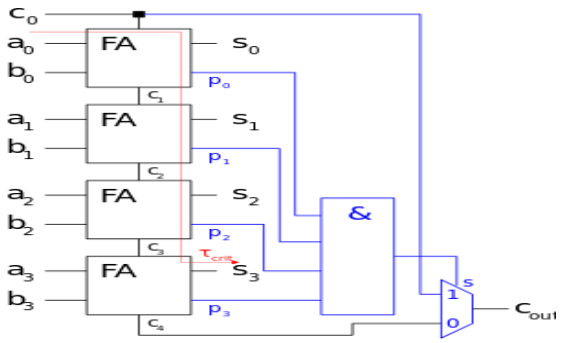

Fig.1 Conventional Carry skip adder

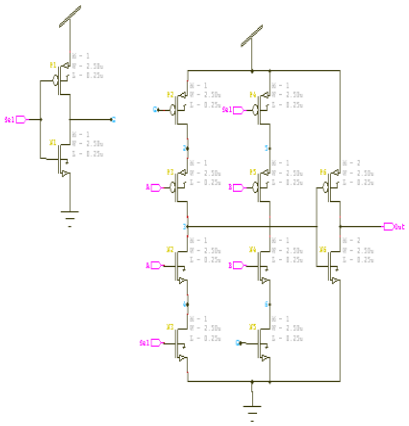

Fig.2 Schematic diagram of multiplexer used in a conventional CSKA

III. PROPOSED CARRY SKIP ADDER

In the proposed CSKA, the multiplexer design has been modified at the output side for better operational characteristics of high speed and low delay (see Fig.3) and the schematic diagram of the multiplexer used in proposed CSKA is shown in Fig.4.Subsequently as the number of transistors are reduced in the multiplexer of the proposed CSKA which is being utilized as a skip logic for the circuit. Since the number of transistors is reduced in the multiplexer, it results in reduced area as well as delay.

There are actually 214 transistors in a proposed carry skip adder out of which 107 are NMOS and 107 are PMOS.

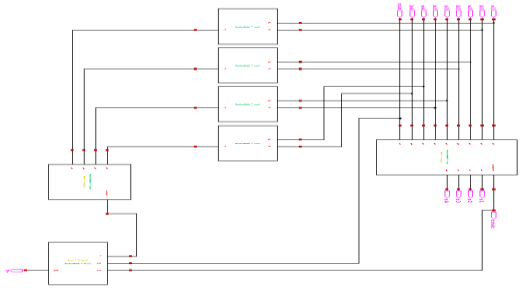

Fig.3 Proposed Carry skip adder

The multiplexer used in the proposed CSKA consists of 6 transistors which is comparatively lesser in number to the one used in a conventional CSKA. The reduced number of devices has the additional advantage of lower capacitance. Further, this multiplexer functions based on transmission gate logic. The transmission gate is an non mechanical relay built with CMOS technology. It is made by parallel combination of NMOS and PMOS transistors with the input at the gate of one transistor (C) being complementary to the input at the gate of the other. Fig.5 shows the output waveform of proposed carry skip adder.

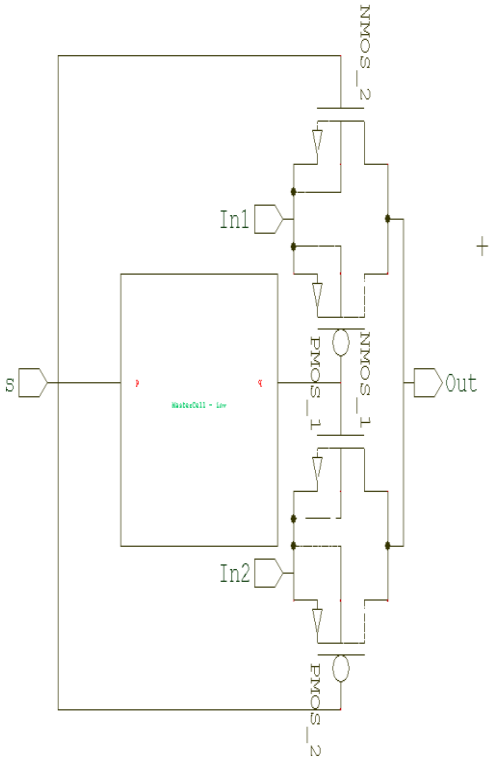

Fig.4 Schematic diagram of multiplexer used in a proposed CSKA

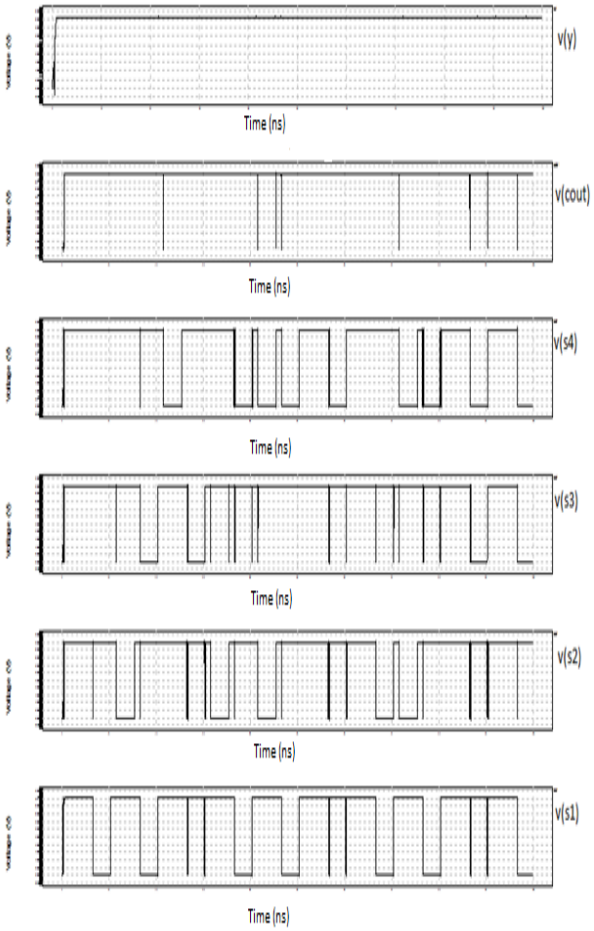

Fig.5 Output waveform of proposed carry skip adder

IV. SIMULATION AND COMPARISON OF EXISTING CSA AND PROPOSED CSA FULL ADDER

The graphs shown in Fig.6 and 7 depicts that the proposed 9T full adder design has better performance in comparison to the existing design

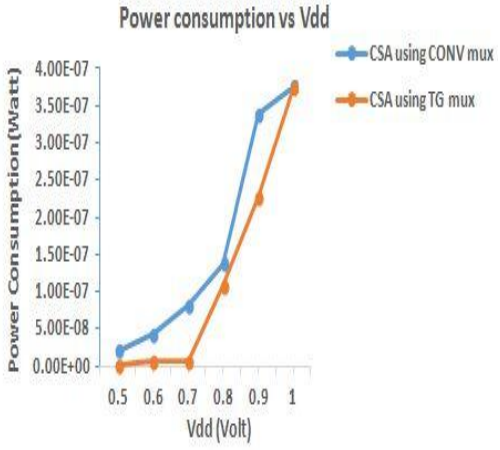

Fig.6 Power consumption with varying Vdd

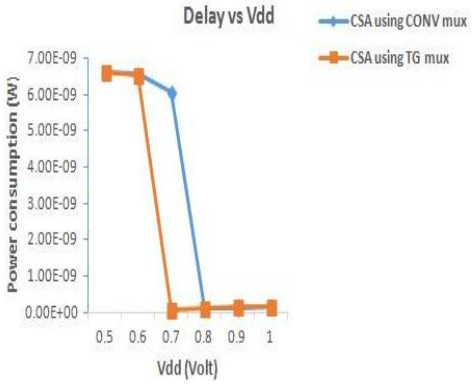

Fig.7 Delay with varying Vdd

It was found that proposed carry skip adder has 18-66% and 35-77% improvement in terms of power consumption and Delay with varying supply voltage as compared to the existing carry skip adder respectively.

Fig.8 and 9 shows the proposed design has 63-70% and 23-45% improvement in power consumption and delay with varying temperature in comparison to the existing design Thus, the proposed design is efficient in power consumption at various system temperature as seen below.

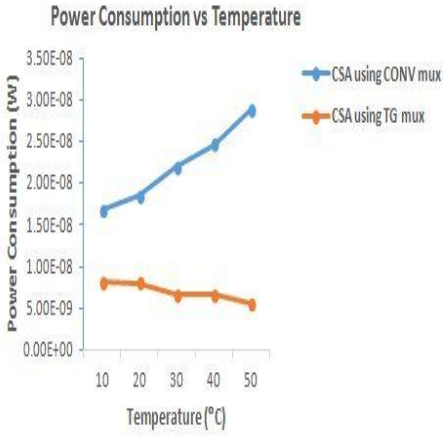

Fig.8 Power consumption with varying temperature

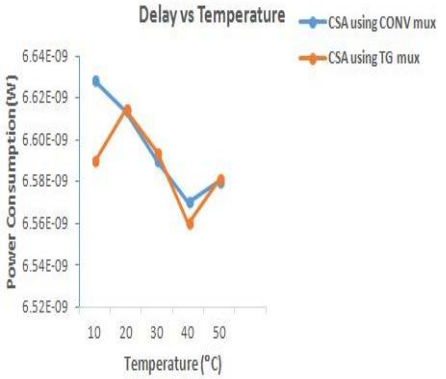

Fig.9 Delay with varying temperature

Comparison in terms of power consumption and delay with varying frequency is shown in Fig.9 and 10 which illustrates that the proposed design has lesser power consumption and delay as compared to the existing design. It should be noted that only till a frequency range of 5 MHz, the proposed design consumed much lesser power than the conventional design. However, after 5 MHz the power consumed by the proposed design increases significantly, nevertheless it is still lesser than the conventional design.

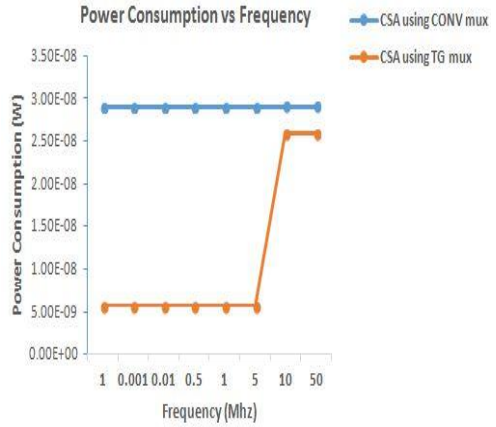

Fig.10 Power consumption with varying frequency

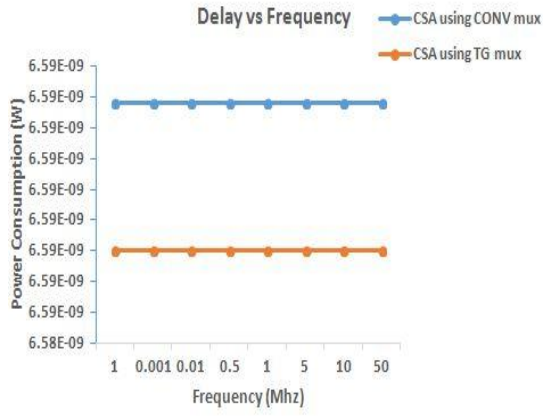

Fig.11 Delay with varying frequency

V. CONCLUSION

In this paper, a CSKA structure called TG-CSKA (transmission gate-carry skip adder) was proposed, which exhibits a higher speed and lower power consumption compared with those of the conventional one. The speed enhancement was achieved by modifying the structure through the complementary transmission gate logic. Conventional CSKA is good in reliability, but on the other side proposed CSKA has the benefits of hardware reduction having lesser number of transistors. The proposed circuit has been tested to have better temperature sustainability and significantly less power consumption. Again, the suggested structure showed the lowest delay and making itself as a better candidate for high-speed low-power applications.

REFERENCES

[1] R. Zlatanovici, S. Kao, B. Nikolic, "Energy–delay optimization of 64-bit carry-lookahead adders with a 240 ps 90 nm CMOS design example", *IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 569-583, Feb. 2009.*

[2] S. K. Mathew, M. A. Anders, B. Bloechel, T. Nguyen, R. K. Krishnamurthy, S. Borkar, "A 4-GHz 300-mW 64-bit integer execution ALU with dual supply voltages in 90-nm CMOS", *IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 44-51, Jan. 2005.*

[3] G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, R. Krishnamurthy, "Comparison of high-performance VLSI adders in the energy-delay space", *IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 754-758, Jun. 2005.*

[4] He, C.-H. Chang, "A power-delay efficient hybrid carry-look ahead /carry-select based redundant binary to two's complement converter", *IEEE Trans. Circuits Syst. I Reg. Papers, vol. 55, no. 1, pp. 336-346, Feb. 2008.*

[5] S. Jain et al., "A 280 mV-to-1.2 V wide-operating-range IA-32 processor in 32 nm CMOS", *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), pp. 66-68, Feb. 2012.*

[6] P. M. Kogge, H. S. Stone, "A parallel algorithm for the efficient solution of a general class of recurrence equations", *IEEE Trans. Comput. vol. C-22, no. 8, pp. 786-793, Aug. 1973*

[7] G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, and R. Krishnamurthy, "Comparison of high-performance VLSI adders in the energy-delay space," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 754–758, Jun. 2005.*

[8] Ramkumar and H. M. Kittur, "Low-power and area-efficient carry select adder," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 371–375, Feb. 2012.*

[9] Kantabutra, "Designing optimum one-level carry-skip adders," *IEEE Trans. Comput., vol. 42, no. 6, pp. 759–764, Jun. 1993.*

[10] Shamima Khatoon, "A Novel Design for Highly Compact Low Power Area Efficient 1-Bit Full Adders," *International Journal of Advances in Engineering & Technology, Vol. 4, pp. 464-473, 2012.*