RESEARCH ARTICLE OPEN ACCESS

Low Power And High Speed Sample And Hold For Adc Applications

Prity Yadav, Annu Saini
Corresponding Author: Prity Yadav

ABSTRACT
This Paper describes the improved design of low voltage sample and hold amplifier for analog to digital converter applications. The proposed design uses double sampling technique to increase the sampling rate, reliable bootstrap switch to reduce switch on resistance and to extend linear range of switch and better SFDR. The designed sample and hold operates at 100MS/s for input signal amplitude of 1.2Vpp.The circuits are designed using CSM 0.18µm technology incadence environment and power consumption estimated was 6.5 mwatt from 1.2V power supply.

Date of Submission: 23-10-2017 Date of acceptance: 04-11-2017

I. INTRODUCTION

With the explosive growth of wireless communicationsystem and portable devices, the power reduction ofintegrated circuits has become a major problem. An examplefor low power application is a wireless communicationsystem. With the rapid growth of internet and informationon demand, handheld wireless terminals are becoming increasingly popular. (i.e. UPS and handheld pad for packagedelivery.) With limited energy in a reasonable size battery, minimum power dissipation in integrated circuit isnecessary. Many of the communication systems today utilizedigital signal processing (DSP) to resolve the transmitted information. Therefore, an analog-to-digital interface isnecessary, between the received analog signal and DSPsystem. This interface achieves the digitization of receivedwaveform subject to a sampling rate requirement of the system. Being a part of communication system as mentioned above, the analog to digital interface also needs to adhere to the low power constraint.

Sample and hold (S/H) or track and hold circuits are important in signal processing circuits. They are used at thefront end of analog to digital converters (ADC) and at the backend of digital to analog converters (DAC). The signal to noiseratio of an ADC is usually limited by the performance of the sample and hold block. Precision analog integrated circuits aremostly implemented by sampled data circuits in which thebasic building block is sample and hold.As the supplyvoltage is scaling down with the technology analog samplingprocess becomes more challenging because of low power and for high speed application. This paper presents the design of low voltage sample and hold amplifier for ADC applications usingdouble sampling technique. In this paper the design and implementation of modified switch double sampling rate and low power sample and hold circuit has been described. The main application of this sample-and-hold circuit is in the low power and high speed pipelined ADCs.It has been designed in a 0.18µm CMOS process, which allows only a maximum supply voltage of 1 .2Volt.

II. SAMPLE AND HOLD ARCHITECTURES

Sample and hold architectures can be divided into open loopand closed loop architectures. The main difference between thearchitectures is in closedloop architectures the samplingcapacitor is enclosed in a feedback loop at least in hold mode.

A. Openloop Architecture

The basic open loop sample and hold architecture consists of a switch and a capacitor and is shown in figure l(a). the operation of the circuit is explained as follows, In sample mode the switch is closed and the voltage on the capacitor tracks the input signal. In hold mode switch is opened and the input voltage level at the switch opening instant will be held by capacitor. For practical implementation input and output buffers are added to reduce hold mode feed-through and to drive load and is shown in figure 1(b). The drawbacks of the open loop architecture are accuracy limitation and signal dependent charge injection from the switch. Some of the limitations of above circuits can be overcome by using bottom plate sampling technique and is shown in figure l(c) .[1,2,4,6].

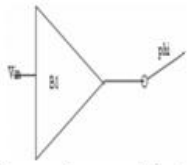

Figure1(a) Basic open loop architecture

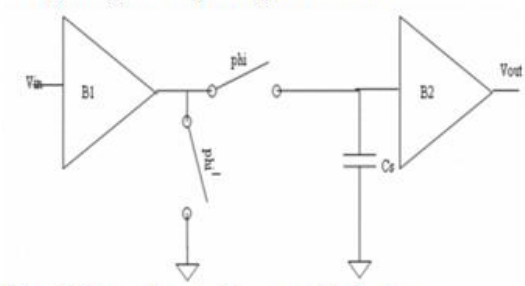

Figure 1(b) open loop architecture with buffers

B.Closed loop architecture

Closed loop architecture a feedback loop is includedbetween the input and output. Inclusion of feedback improvesthe accuracy. The basic closed loop sample and holdarchitecture is shown in figure. 2. 1n sample mode output tracksinput by the feedback loop. In hold mode feedback loop isbroken and capacitor held the value of the instant at whichswitch is opened. The drawback of the architecture shown infigure.2 is speed limitation due to stability requirements of thecircuit. Closed loop S/H architecture, commonly used in switchedcapacitor circuits is flip-around S/H, is shown in Fig. 3.

A simple close loop switch capacitor sample-and-holdarchitecture is used in this architectureFig. 3. Here Ø1 is delayedversion of Ø3, and Ø2 is the inverse of Ø3. Thus, it consistsbottom-plate sampling [3] to eliminate the signal dependentclock-feed through effect and hence reduces the harmonicdistortion significantly. During the sample phase (Ø1),capacitor Cs is connected between signal source and opam'sinput, which is connected to the corresponding output.Thus, Cs is charged to (Vin-Vos), where Vos is the outputcommon-mode level. In the following hold phase (Ø2) Cs isconnected to op-amp in feedback and output differentialvoltage becomes Vin, eliminating any op-amp offset voltage.

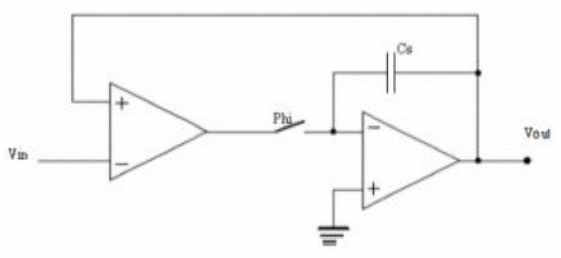

Figure 1 Closed loop sample and hold circuit

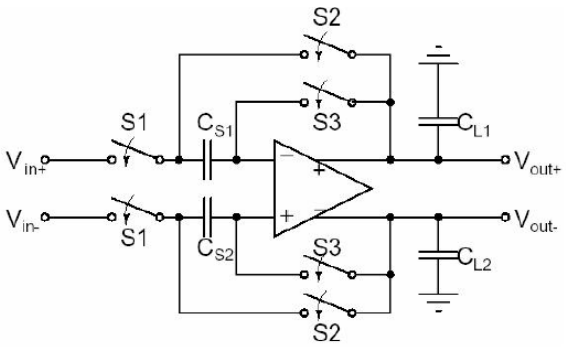

Figure 2(a): switched capacitor based sample and hold circuit

A disadvantage with the above architecture is that theoutput voltage varies considerably between sample and holdphases, since the differential output of op-amp is set to zeroin every sample phase. So, for high-speed application the op-amp'sslew-rate should be larger which increases the powerdissipation considerably. Also, op-amp remains in closedloopfor both phases. To solve these problems, thearchitecture has been modified as shown in Figure.3(b). In thisarchitecture the op-amp remains in open-loop configurationduring the sampling phase. So op-amp has not to settle down when switching from hold phase to sampling phase. Also thefalling edge of switch SI is delayed than S2 so that glitch atthe differential output can be significantly reduced whenswitching from sampling mode to hold mode.

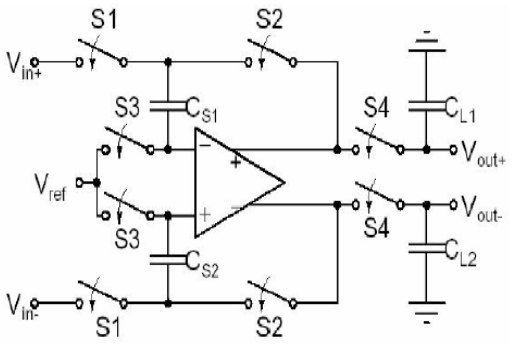

Figure 3(b) switch capacitor sample and hold circuit with modified clock

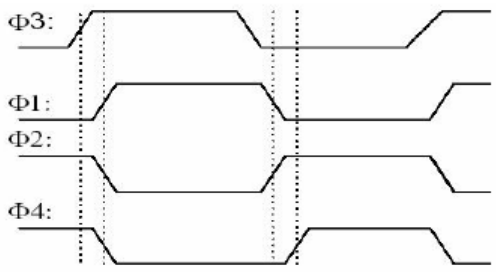

Figure .3 (c) Clock sequences

The speed of S/H block mainly depends on the time constant in the sampling and hold phase. During the sampling phase the time constant is given by,

$\tau_S = (R_{on1} + R_{on2}) * C_S$

Where, R_{on1} and R_{on2} are the equivalent resistances ofswitch S1 and S2 respectively. During the hold mode settlingtime constant of feedback amplifier is given by,

$$\tau_S = \frac{C_L.C_{IN} + C_L.C_S + C_s.C_{IN}}{G_m.C_H}$$

WhereC_s, Cs_1, C_{S2}, C_L= C_{L2}, L_2, Gm is the transconductance of op-amp and Cm, is the op-amp's inputcapacitance. For 10-bit accuracy the required settling time is approximately given by 7*h.

Thus the sampling speed is limited by low value of Cs(Equation 1) and input signal bandwidth is limited by highvalue of Cs (Equation 2). Also the sampling noise (KT/C)depends on the size of sampling capacitor (Cs). Since thisdesign is to be implemented in 0.18ptm CMOS technologythe trade-off between signal-to-noise ratio and speed is verycrucial. The switch can be realized as simple MOStransistor, transmission gate or bootstrapped type. Forlow distortion at given power consumption the switches oftransmission gate are used in this architecture. Since themaximum supply voltage is 1.8volt the maximum swing atsingle endis taken as 600mV. With this output swing theminimum value of sampling capacitor (Cs) is approximatelyl.lpf for signal-to-noise ratio of greater than 65dB. Themaximum value of load capacitance (input of pipelinedADC) is assumed as 1.5pf.

C. Double sampling architecture

In order to utilize op-amp efficiently different techniques proposed in literature one is double sampling and other is to employ non-resetting sample and hold topology. Double sampled architecture preferable for high speed applications.

Double sampled sample and hold architecture is shown in Figure 4. In this configuration op-amp is shared by two parallel sampling circuitry operated by opposite clock phases. The operation is as follows when input is sampled by one of the sampling circuitry other circuit will be in hold operation and the reverse is going to happen when clock is complemented. The advantage of double sampling is for the same op-amp specification we can achieve twice sampling rate.

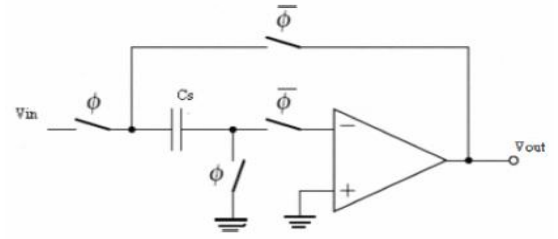

Figure 3Double sampled sampleand hold circuit

The double sampling approach introduces some unwantedphenomena in S/H circuit one is error due to finite op-amp gainand second is timing mismatch between the two signal pathsand finally error due to gain mismatches in signal paths. So a careful design approach is required to overcome the above problem mentioned issues.

III. IMPLEMENTATION

The designed Sample and hold is to be used as a front-end of a 10-bit 100MHz ADC. The basic blocks for the implementationare sampling capacitor, op-amp and switch. The size of the sampling capacitor is limited by KT/Cnoise. In order to reduce the KT/C noise the sampling capacitorvalue can be found using

$$C_S > \frac{KT.12}{2^{-2N}.V_{FS}^2}$$

Where N is the number of bits and V_{FS} is the Full-scale ADCvoltage, for a 10-bit ADC the required sampling capacitorvalue to reduce KT/C noise is greater than l.2pF.In thisimplementation a sampling capacitor of 1. 5pF value isselected.

A. Operational amplifier

The design of fully differential op-amp is critical in theabove architecture since it should meet the requiredspecifications such as open loop gain, slew rate, unity gainfrequency, common mode gain, output differential swing andinput common mode range. Now for 10-bit of accuracy thegain error of op-amp should be less than +/- 1/2 LSB. If theinput capacitance of op-amp is assumed to be less than 0.5pfthen value of feedback factor (D) will not be less than 0.75.This requires the open loop gain (A_0) of op-amp should begreater than 68dB which can be calculated by,

$$A_0 = \frac{2^{N+1}}{\beta}$$

Where N is the number of bits and β is the feedback factor. The architecture of op-amp can be of telescopic cascode, two-stage, regulated cascode or foldedcascode type. Two stage amplifier can give higher gain and output swing but at the cost of low speed and higher power consumption. Telescopic amplifier can give high gain and speed at the cost of lower output swing. Regulated cascade can have larger power consumption. So the final choice is folded cascode amplifier, which can give larger swing than telescopic amplifier for a given open-loop gain. Also the linearity of folded cascode is better than that of other types. The topology of selected op-amp is shown in Figure5. The gain boosters have been added to enhance the overall gain.The gain-boosters are of simple common source type so thatthe unity gain bandwidth of op-amp should not be affected.The common-mode feedback used is very simple and fast. The simulation results of op-amp are summarized in table 1.

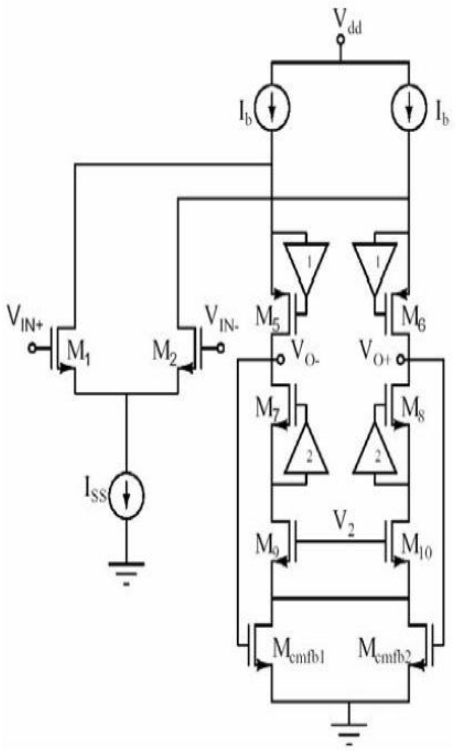

Figure 4 Schematic diagram of folded cascade

B.Switch

The switch in sample and hold can be implemented using simple NMOS transistor but it has several limitations like input dependent finite ON resistance and input dependent charge injection. In order toimprove the performance of switch NMOS transistor can be replaced by a CMOS switch; proper selection of transistors aspect ratio minimizes the distortion, but this is not an effective solution. One of the commonly used techniques to solve the above problems is bootstrap switch [5]. The basic bootstrap switch implementation is shown in figure 6. Here capacitor used as a floating battery with a valueV_{dd}. In holding phase sampling switch is off through switch s5 and capacitor C1is charged toV_{dd} through switches s_1 and s_2 . In sampling phase this voltagevalue is applied between gate and source of sampling switch using switches s_1 and s_2 [5]. Although the boosted NMOS switch has good distortion characteristics; the required boost voltage is a tradeoff. In addition to the increased circuit complexity the use of the boosted voltage may cause reliability problems and increase the switching noise on the substrate. In the present sample and hold implementation a reliable bootstrap technique is selected and is shown in figure7.

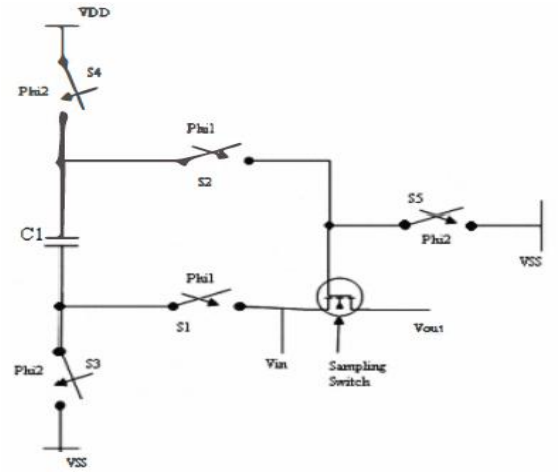

Figure 5 Basic bootstrapswitch

In the Fig .7 during S_1 phase the capacitorC_1 charges to V_{DD}-V_{th} In the other phase V_{DD} is applied to the bottom plate of the capacitor. The voltage on the top plate rises to V_{DD}- (V_{DD}-V_{th}). Thisarchitecture gives significant area improvements and reliability is also not an issue in this given architecture because terminal voltage of any transistor does notcross the maximum supply voltage [3].

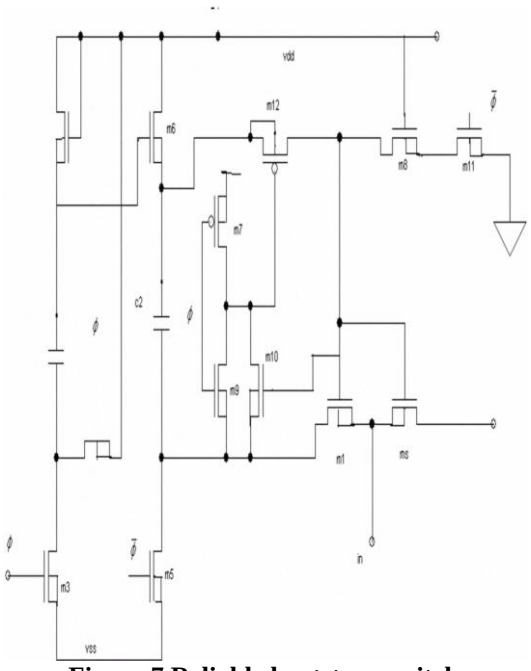

Figure 7 Reliable bootstrap switch

IV. SIMULATION RESULTS

All the circuits are designed using CSM O.18um technologyin cadence environment. The designed op-amp achieves rail torail operation and frequency response of the op-amp is shown inFigure.8 with a gain of 85db and phase margin of 54° and unitygain frequency around 450MHz.The implemented switch alsoachieves rail to rail operation

Figure7 and transient simulation ofswitch is shown in figure.9. In order to test sample and holdcircuit the method presented in [7] used. The transientsimulation result of the sample and hold is shown in figure. 10. Figure.11 shows the frequency spectrum for a l0 MHzinput sine wave sampled at 100MHz and the second harmonic is -60 db. Spectrum of output signal from sample and hold circuit is shown in figure.12.

Table-1

Parameter	Hold Phase
DC Gain	78 dB
Gain bandwidth	390 MHz
Phase Margin	75 degrees
Slew Rate(Differential)	340V/µsec
Output swing	0.6 volt

Simulated result of OTA
A C Response

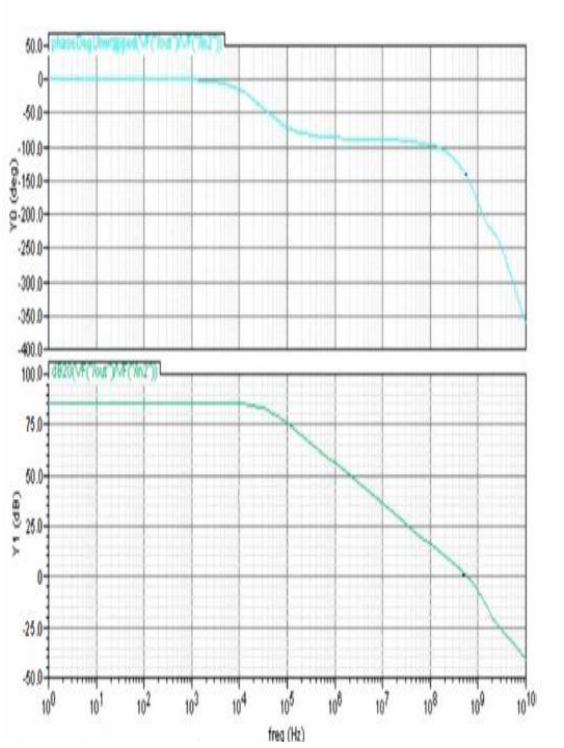

Figure 8 Operation amplifier frequency Response

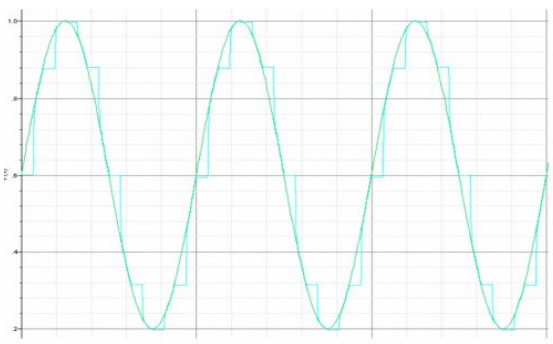

Figure 9 Transient simulation of switch at 10MHz

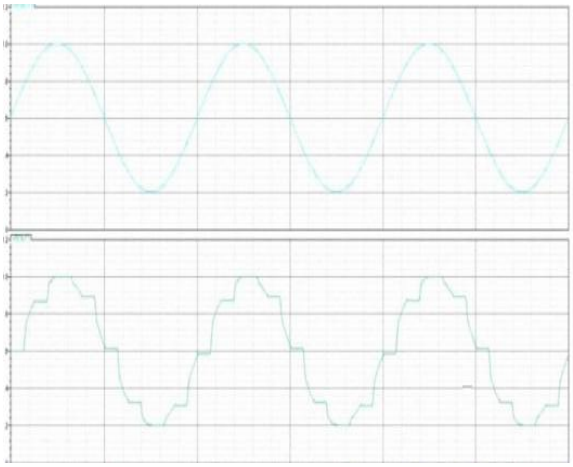

Figure 10 Transient simulation of S/H at an Input frequency 10 MHz

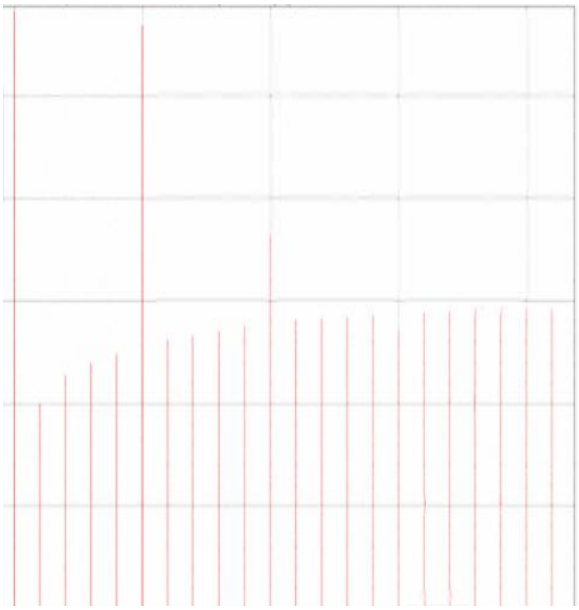

Figure 11 DFT spectrum with input frequency of input frequency and sampling frequency 100MHz

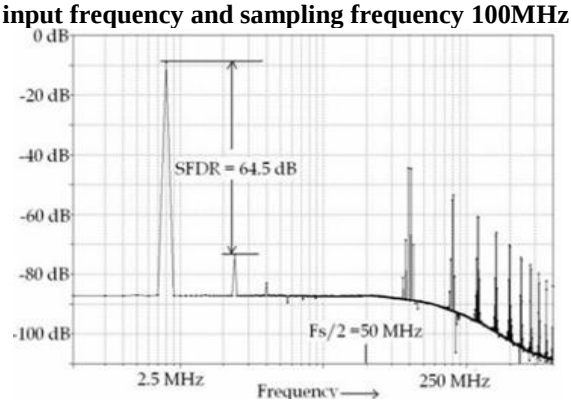

Figure 12 Spectrum of output signal from sample and hold circuit

A comparison of the designed Sample and hold with fewreported articles is given in Table 2

Parameter	Ref 10	Ref 11	Ref 12	Ref 13	This work
Technology	1.2	0.25	0.35	0.5	0.18
V_{DD}	5	1.5	1.2	1.2	1.2
No of bits	10	12	NA	NA	10
Fs(MS/Sec)	50	75	50	40	100
Power(mwatt)	47	16	2.6	12	6.5
THD@fin(dB)	-67@ 1MHz	NA	-58@ 1MHz	-50@ 2MHz	-60@ 10MHz
SFDR(dB)	70	NA	68.5	-	64.5

V. CONCLUSION

The design of sample and hold amplifier based on double sampling technique is presented. The simulation results show that the designed sample and hold works well with a supply voltage of l.2V and gives satisfactory performance up to 50MHz input signal frequency. This achieves the SFDR of 64.5dB at the sampling frequency of l00MS/s and consumes the power of 6.5mWfrom 1.8volt supply.Using bootstrapped switches and modifying the op-amp architecture can further increase the input dynamic range, SFDR and switch on resistance.

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Prity Yadav. "Low Power And High Speed Sample And Hold For Adc Applications." International Journal of Engineering Research and Applications (IJERA) , vol. 7, no. 11, 2017, pp. 33–38.