

CORDIC Algorithm for WLAN

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ABSTRACT

This research aims to implement CORDIC Algorithm for WLAN. The design is coded using VHDL language and for the hardware implementation XILINX Spartan-3FPGA is used. VHDL implementation is based on results obtained from Xilinx ISE simulation.

Keywords: CORDIC, FPGA, implementation, WLAN.

I. INTRODUCTION

CORDIC (for COordinate Rotation Digital Computer), also called as the digit-by-digit method and Volder's algorithm. It is a simple and efficient algorithm to calculate hyperbolic and trigonometric functions. It is commonly used when no hardware multiplier is available (e.g., simple microcontrollers and FPGAs) as the only operations it requires are addition, subtraction, bit shift and table lookup.

The CORDIC Algorithm calculates the angle of received vector in a signal constellation by means of arctangent function and it is used in receivers to find frequency offset and phase shift.

II. Wireless LAN

A wireless LAN (WLAN) is a wireless computer network that connects two or more devices using a wireless distribution method within a limited area such as a home, school, computer labs, or office building. By using this WLAN users can move around within a local coverage area and still be connected to the network, and can provide a connection to the wider Internet. Most modern WLANs are based on IEEE 802.11 standards, marketed under the Wi-Fi.

III. CORDIC ALGORITHM

3.1 Mode of operation

CORDIC rotator works in two modes: Rotation & Vectoring [3].

3.1.1 Rotation mode

This explanation shows how to use CORDIC in rotation mode to calculate the sine and cosine of an angle and assumes the desired angle is given in radians and represented in a fixed point format. To determine the sine or cosine for an angle, the y or x coordinate of a point on the unit circle corresponding to the desired angle must be found.

Using CORDIC, we would start with the

vector :

$$v_0 = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

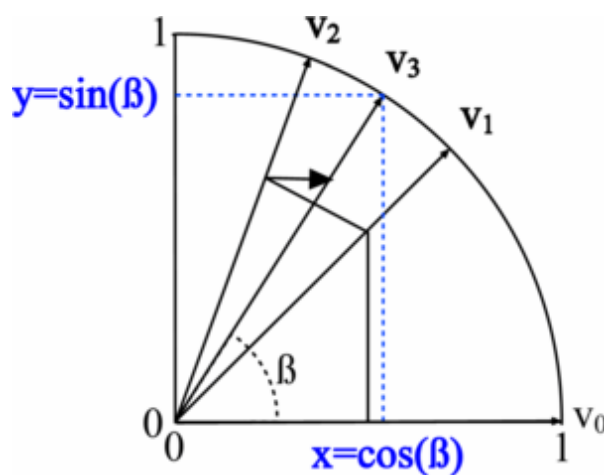


Fig. 1 An example for CORDIC algorithm

In the first iteration, this vector is rotated 45° counter clockwise to get the vector v_1 . Successive iterations rotate the vector in one or the other direction by size-decreasing steps, until the desired angle has been achieved. Step i size is $\arctan(1/(2^{i-1}))$ for $i = 1, 2, 3, \dots$

More formally, every iteration calculates a rotation, which is performed by multiplying the vector v_{i-1} with the rotation matrix R_i .

$$v_i = R_i v_{i-1}$$

The rotation matrix is given by:

$$R_i = \begin{bmatrix} \cos Y_i & -\sin Y_i \\ \sin Y_i & \cos Y_i \end{bmatrix}$$

Using the following two trigonometric identities:

$$\cos \alpha = \frac{1}{\sqrt{1 + \tan^2 \alpha}}$$

$$\sin \alpha = \frac{\tan \alpha}{\sqrt{1 + \tan^2 \alpha}}$$

the rotation matrix becomes:

$$R_i = \frac{1}{\sqrt{1 + \tan^2 Y_i}} \begin{bmatrix} 1 & -\tan Y_i \\ \tan Y_i & 1 \end{bmatrix}$$

The expression for the rotated vector then becomes:

$$v_i = \frac{1}{\sqrt{1 + \tan^2 Y_i}} \begin{bmatrix} 1 & -\tan Y_i \\ \tan Y_i & 1 \end{bmatrix} \begin{bmatrix} x_{i-1} \\ y_{i-1} \end{bmatrix}$$

Where x_{i-1} and y_{i-1} are the components of v_{i-1} . Restricting the angles y_i so that $\tan Y_i$ takes on the values $\pm 2^{-i}$, the multiplication with the tangent can be replaced by a division by a power of two, which is efficiently done in digital computer hardware using a bit shift. The expression then becomes:

$$v_i = K_i \begin{bmatrix} 1 & -\sigma_i 2^{-i} \\ \sigma_i 2^{-i} & 1 \end{bmatrix} \begin{bmatrix} x_{i-1} \\ y_{i-1} \end{bmatrix}$$

Where

$$K_i = \frac{1}{\sqrt{1 + 2^{-2i}}}$$

and σ_i can have the values of -1 or 1 , and is used to determine the direction of the rotation; if the angle β_{i+1} is positive then σ_i is $+1$, otherwise it is -1 .

K_i can be ignored in the iterative process and then applied afterward with a scaling factor:

$$K(n) = \prod_{i=0}^{n-1} K_i = \prod_{i=0}^{n-1} \frac{1}{\sqrt{1 + 2^{-2i}}}$$

which is calculated in advance and stored in a table, or as a single constant if the number of iterations is fixed. This correction could also be made in advance, by scaling v_0 and hence saving a multiplication. Additionally it can be noted that:

$$K = \lim_{n \rightarrow \infty} K(n) = 0.6072529350$$

to allow further reduction of the algorithm's complexity.

After a sufficient number of iterations, the vector's angle will be close to the wanted angle β . For most ordinary purposes, 40 iterations ($n = 40$) is sufficient to obtain the correct result to the 10th decimal place.

The only task left is to determine if the rotation should be clockwise or counterclockwise at each iteration (choosing the value of σ). This is done by keeping track of how much the angle was rotated at each iteration and subtracting that from the wanted angle; then in order to get closer to the wanted angle β , if β_{n-1} is positive, the rotation is clockwise, otherwise it is negative and the rotation is counter clockwise.

$$\beta_i = \beta_{i-1} - \sigma_i Y_i, \quad Y_i = \arctan 2^{-i}$$

The values of Y_n must also be recomputed and stored.

But for small angles,

$$\arctan(Y_n) = Y_n$$

In fixed point representation, reducing table size.

As can be seen in the illustration above, the sine of the angle β is the y coordinates of the final vector v_n , while the x coordinate is the cosine value.

After a sufficient number of iterations, the vector's angle will be close to the wanted angle β . For most ordinary purposes, 40 iterations ($n = 40$) is sufficient to obtain the correct result to the 10th decimal place.

IV. SCHEME OF IMPLEMENTATION

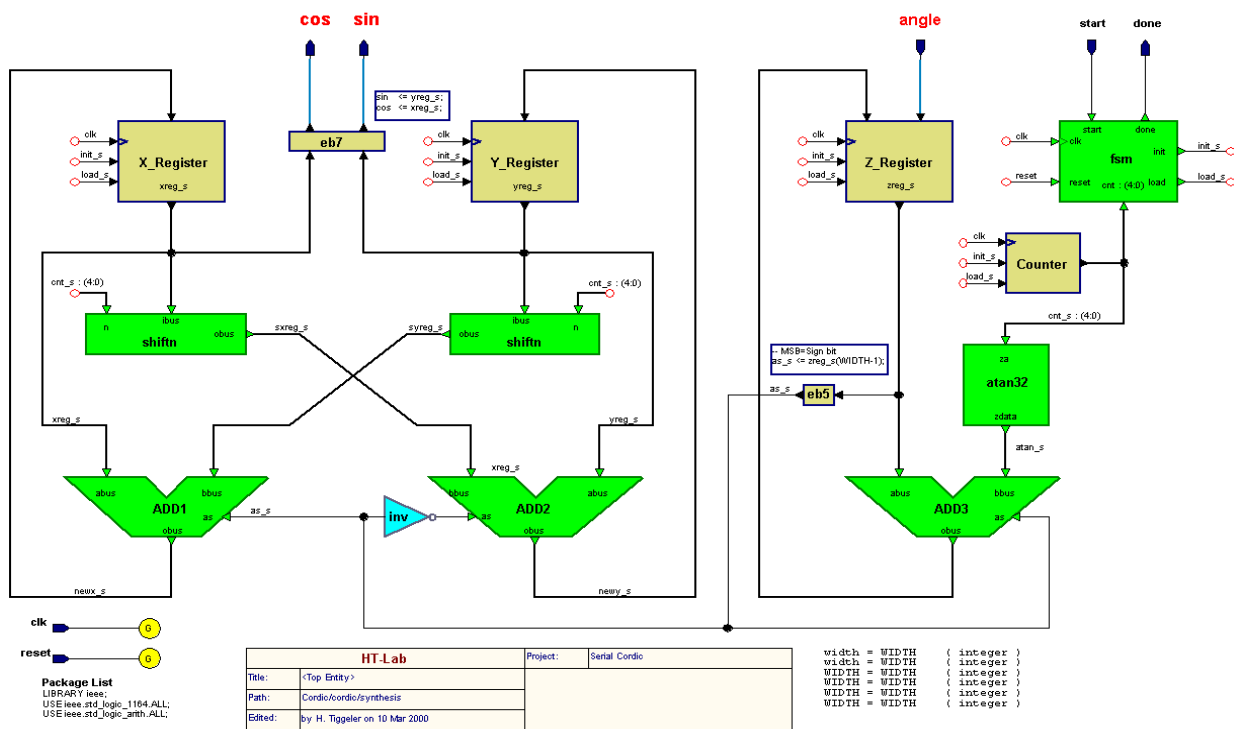
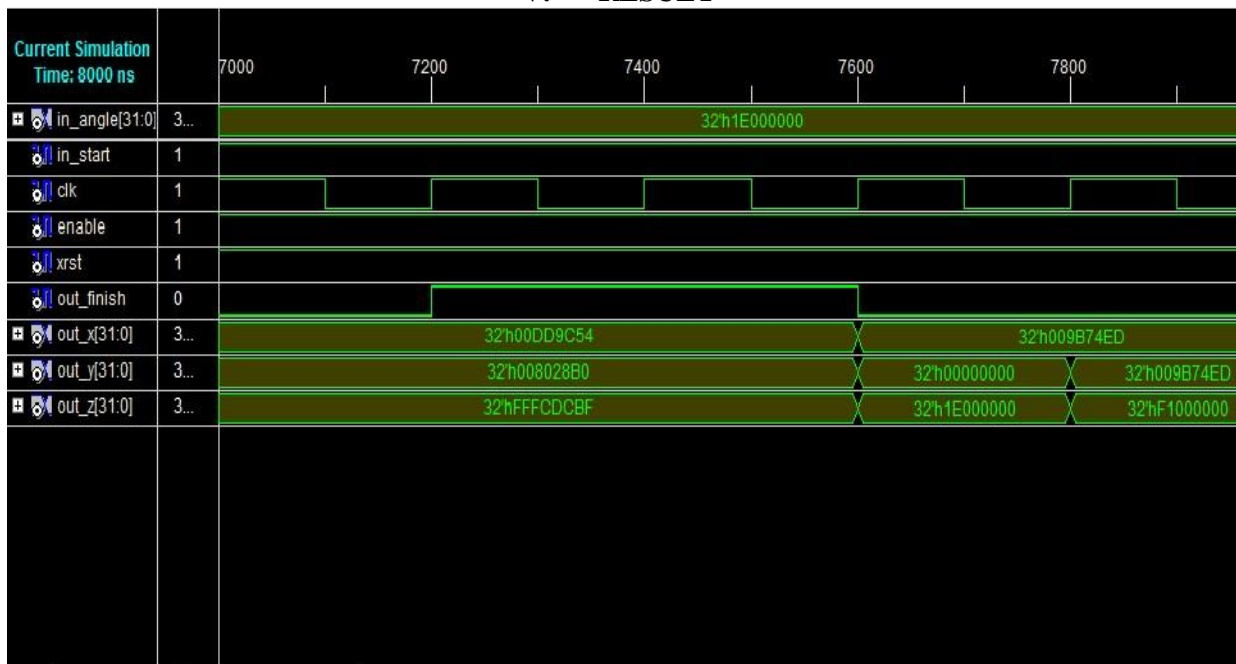


Fig. 2 Block diagram for CORDIC Algorithm.

V. RESULT



VI. CONCLUSION

This paper shows that CORDIC Algorithm is useful for use in WLAN technology. By the regularity, the CORDIC based architecture is very

suitable for implementation with pipelined VLSI array processors.

This paper represents method to calculate angle in wireless LAN receiver block by using CORDIC Algorithm.

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