RESEARCH ARTICLE OPEN ACCESS

# Comparative Analysis and Simulation of Diode Clamped & Cascaded H-Bridge Multilevel Inverter using SPWM Technique

Mohit Jain*, Anuradha Singh**, Suman Singh***
*(M.Tech Scholar, Department of EEE, Kamla Nehru Institute of Technology, Sultanpur (U. P.), India)
** (Senior Lecturer, Department of EEE, SP Memorial Institute of Technology, Allahabad (U. P.), India)
*** (M.Tech Scholar, Department of EEE, Amity University, Noida (U. P.), India)

**ABSTRACT**
Multilevel inverters have become more popular over the years in high power medium voltage applications without the use of a transformer and with promise of less disturbance & reduced harmonic distortion. In this paper, two types of multilevel converter in three phase configuration, cascaded H-Bridge multilevel inverter (CMLI) and diode clamped multilevel inverter (DCMLI) of 5 and 7-level are modelled and compared in the case of feeding of a three phase squirrel cage induction motor. Here, carrier based sinusoidal pulse width modulation (SPWM) technique is used as the modulation strategy. These modulation strategy include phase disposition technique (PD), phase opposition disposition technique (POD), and an alternative phase opposition disposition technique (APOD). A detailed study of the modulation technique has been carried out through MATLAB/SIMULINK for both multilevel converters and a comparative evaluation between DCMLI and CMLI using SPWM technique in terms of THD%.

***Keywords*** **–** Cascaded H-Bridge multilevel inverter (CMLI), Diode clamped multilevel inverter (DCMLI), MATLAB/SIMULINK, Sinusoidal pulse width modulation (SPWM) technique, Total harmonic distortion (THD).

## I. INTRODUCTION

In recent years, power semiconductor switches support around 6.5 kV and 2.5 kA high voltage and high current respectively. There are many problems like poor power quality, high stresses, high common mode noise, stresses on motor bearing etc. with the use of conventional power converter topologies and high-voltage semiconductors. So, there is a demand of new converter topologies for medium-voltage drives. Motor damage and failure have been noticed due to some conventional inverters, as high stress level rates produces a common mode voltage across the motor windings. The main problems are motor bearing and motor winding insulation breakdown. Multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors etc. Multilevel inverters solve problem with the present two-level PWM inverter as their rating of semiconductor switches is much lower. Output of multilevel inverter has good power quality. Multilevel inverter can be modulated at fundamental frequency to reduce switching losses.

High power inverters and medium voltage drives have been studied intensively since the mid-1980s for industrial applications [1] [2]. These inverters synthesize higher output voltage levels with a better harmonic spectrum and less motor winding insulation stress. Normally the medium voltage drives are available for ratings from 0.4MW to 40MW at the medium voltage level of 2.3kV to 13.8kV.

Multilevel inverters consist of a series of power semiconductor devices and capacitors with a single dc source or a multiple dc sources without a capacitor, which generate voltages with stepped waveforms in the output. Fig.1 shows one phase leg of multilevel inverters. In this schematic diagram, operations of semiconductors are shown by an ideal switch with several states.

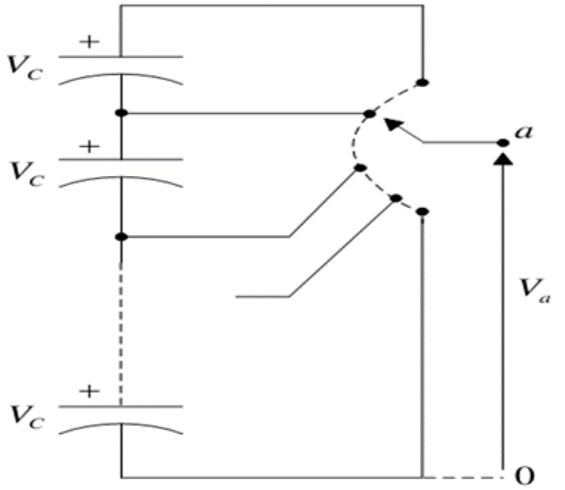



Fig.1 One phase leg of a multilevel inverter.

The switching algorithms of switches and commutation of them allow the addition of the capacitor voltages as temporary dc voltage sources, whereas the semiconductors should withstand limited voltages of capacitors. The large number of semiconductors in the multilevel inverters has a negative impact on the reliability and on the overall efficiency of these types of converters. On the other hand, using inverters with the low number of semiconductors needs large and expensive LC filters to limit insulation stress of motor windings or can be applied for motors that can withstand this stress.

## II. MULTILEVEL INVERTERS

Multilevel inverters are being used widely in static VAr compensators, active power filters and adjustable speed drives (ASDs) for medium voltage induction motors. By increase of the voltage levels to infinite value, THD of voltage waveform decreases to zero, since the waveform will be more sinusoidal; but, in practice the accessible voltage level is limited because of voltage unbalancing problems and power losses. In this part, the two most important topologies of multilevel inverters and their characteristics will be discussed.

### 2.1 Diode Clamped Multilevel Inverter

Fig. 2 & fig. 3 shows the power circuit of a 5-level and a 7-level diode-clamped multilevel inverter. For clarity of the figure, only one phase leg is shown. In this topology, semiconductor devices are connected in series and dc link is divided to smaller capacitors and connects to switches by clamp diodes. The clamp diode connections are necessary to block the current. The number of capacitors in each phase is proportional to the number of phase voltage levels.

The ground point shown in the figure is the common reference point and is connected to the middle of dc link. To generate N voltage levels by the aim of the diode-clamped inverter, N-1 capacitors are needed on the dc bus. Therefore, in a 5-level inverter shown in Fig. 2, dc bus voltage consists of four capacitors: C1, C2, C3, and C4 and in a 7-level inverter shown in fig. 3, dc bus voltage consists of six capacitors: C1, C2, C3, C4, C5, C6. If they are being fed by a dc link voltage of Vdc, the capacitors voltages will be Vdc/4 for 5-level and Vdc/6 for 7-level. Table.1 and Table. 2 presents switching pattern of a 5-level and a 7-level diode-clamped multilevel inverter. "1" indicates that the switch is ON and "0" indicates that the switch is OFF. It is obvious from this table that in each cycle just four switches should be ON for a 5-level and six switches should be ON for a 7-level diode-clamped multilevel inverter.

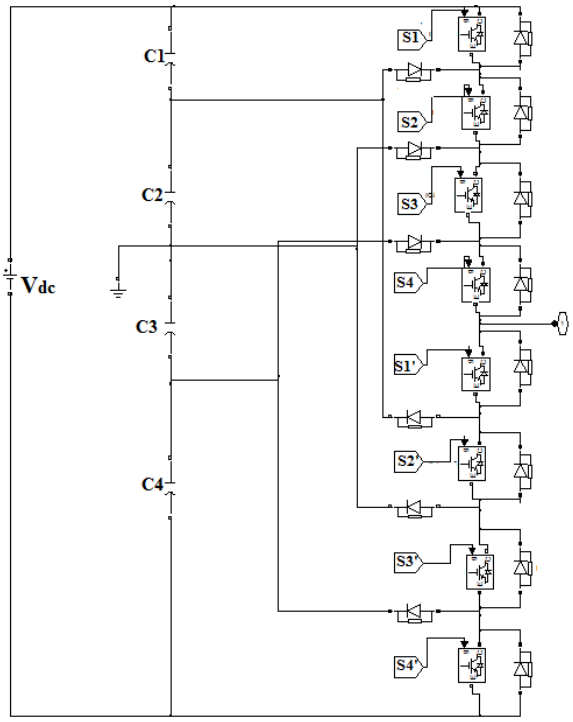



Fig. 2 Diode-clamped 5-level inverter power circuit

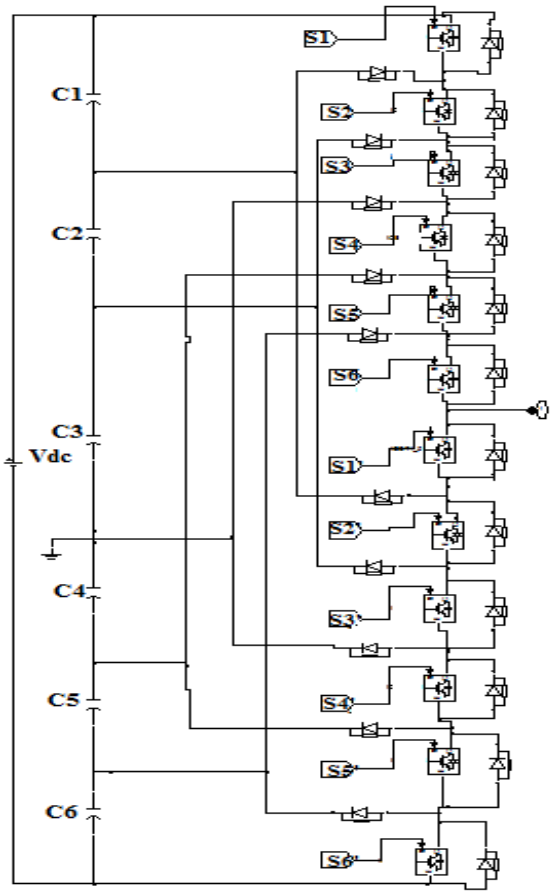



Fig. 3 Diode-clamped 7-level inverter power circuit

Table 1. Diode-clamped 5-level inverter switch states

| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_1'$ | $S_2'$ | $S_3'$ | $S_4'$ | $V_{an}$ |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | $V_{dc}/2$ |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | $V_{dc}/4$ |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | $-V_{dc}/4$ |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | $-V_{dc}/2$ |

Table 2. Diode-clamped 7-level inverter switch states

| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_1'$ | $S_2'$ | $S_3'$ | $S_4'$ | $S_5'$ | $S_6'$ | $V_{an}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | $V_{dc}/2$ |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | $V_{dc}/3$ |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | $V_{dc}/6$ |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | $-V_{dc}/6$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 9 | $-V_{dc}/3$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | $-V_{dc}/2$ |

### 2.2 CASCADED H-BRIDGE MULTILEVEL INVERTER

Fig. 4 & fig. 5 shows the power circuit of a 5-level and a 7-level cascaded H-bridge inverter. For clarity of the figure, only one phase leg is shown in the figure. In this topology power cells are in series and the number of phase voltage levels that can be obtained at the converter terminals is proportional to the number of cells. In other words, in this topology the number of phase voltage levels at the converter terminals is $2N+1$, where $N$ is the number of cells or dc link voltages.

In this topology, each cell has separate dc link voltages and the voltage is same among the cells. The number of dc link voltages is proportional to the number of phase voltage levels. The ground point shown in figure is a common reference point. Each H-bridge cell may have positive, negative or zero voltage. Final output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point, so the number of voltage levels is odd.

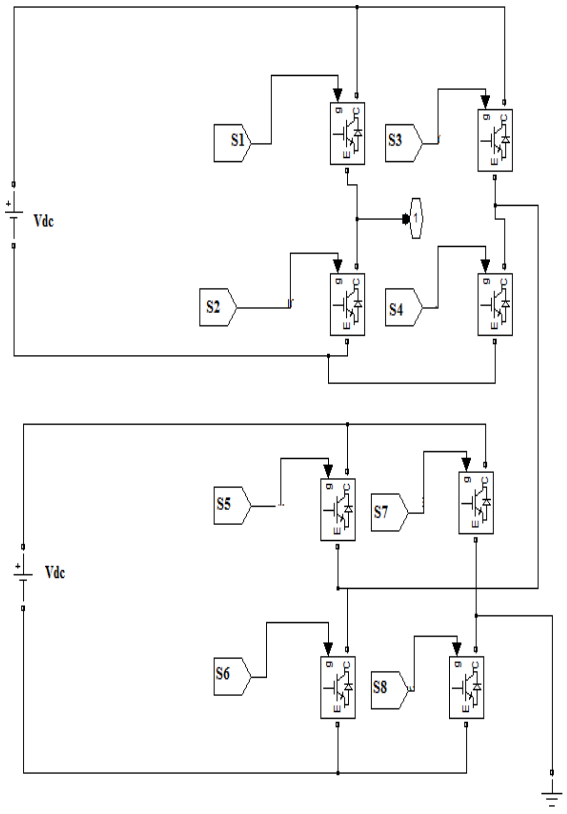



Fig. 4 Cascaded H-bridge 5-level power circuit

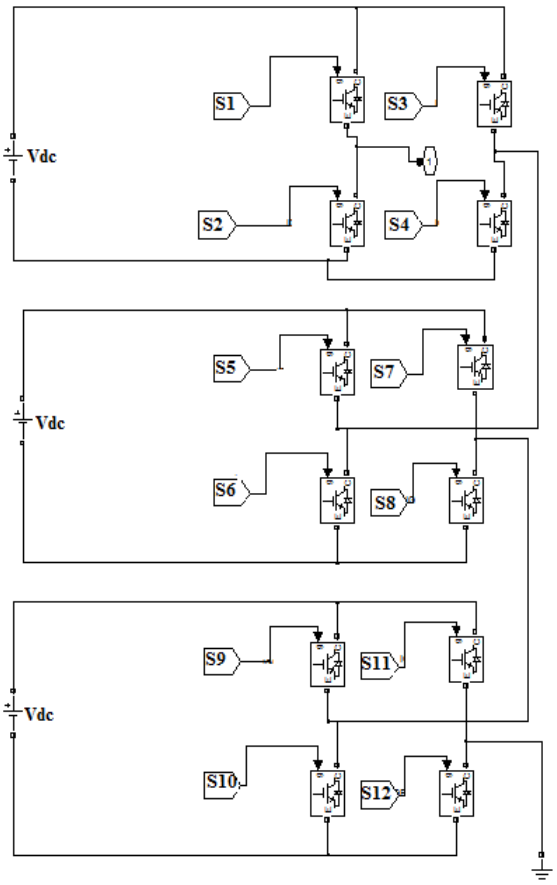



Fig. 5 Cascaded H-bridge 7-level power circuit

Table 3. Cascaded H-Bridge 5-level inverter switch states

| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $V_{an}$ |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 2 $V_{dc}$ |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | $V_{dc}$ |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | - $V_{dc}$ |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | -2 $V_{dc}$ |

Table 4. Cascaded H-Bridge 7-level inverter switch states

| S 1 | S 2 | S 3 | S 4 | S 5 | S 6 | S 7 | S 8 | S 9 | S 10 | S 11 | S 12 | $V_{an}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | +3$V_{dc}$ |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | +2$V_{dc}$ |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | +$V_{dc}$ |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | -$V_{dc}$ |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | -2$V_{dc}$ |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | -3$V_{dc}$ |

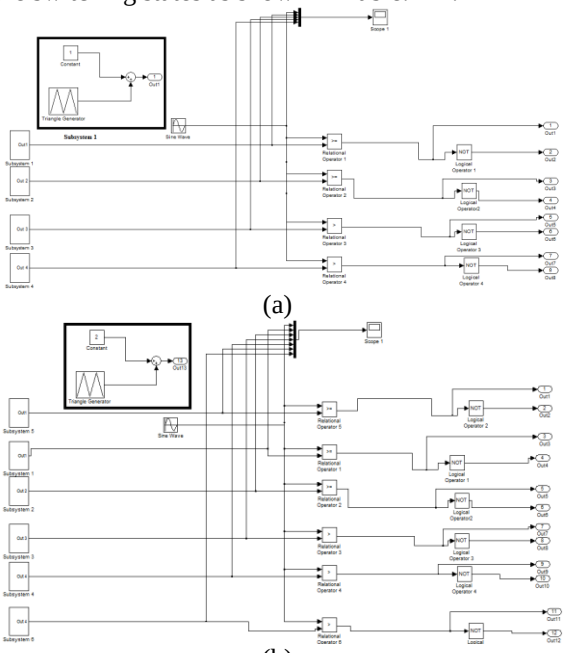
## III. CARRIER BASED PWM TECHNIQUE

The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. This highly conventional technique is based on the comparison of a sinusoidal reference with carrier signals which are usually selected triangular and modified in phase or vertical positions to reduce the output voltage harmonic content. Both modulation schemes can be applied to the MLI but the THD of phase shifted is much higher than level shifted modulation. Therefore we had considered level shifted modulation schemes. Due to simplicity and popularity of this technique, it will be analysed in this chapter in details and will be used as the modulator of the multilevel topologies.

In general, a multilevel inverter with $m$ voltage levels requires $(m-1)$ triangular carriers. In Level Shifted PWM, all the triangular carriers have the same frequency and the same amplitude. The frequency modulation index is given by $m_f = \frac{f_{cr}}{f_m}$, which remains the same as that for the phase-shifted modulation scheme whereas the amplitude modulation index is defined as:

$$m_a = \frac{U_m}{U_{cr}(m-1)} \text{ For } 0 \le m_a \le 1 \ldots\ldots\ldots\ldots\ldots (1)$$

Where $U_m$ is the peak amplitude of the modulating wave and $U_{cr}$ is the peak amplitude of the each carrier. In this paper the simulated waveforms for 5-level $U_m = 2$ and for 7-level $U_m = 3$ and $U_{cr} = 0.5$ for both 5 and 7-level. The logic to generate the gatings for the IGBTs by comparison of the modulating signal with the carrier waves, is described as shown in fig. 6 (a)-(b). For 5-level we need four carrier waves and for 7-level we need 6 carrier waves. The commutation of the switches for both multilevel converter according to the switching states as shown in Table. 1-4.

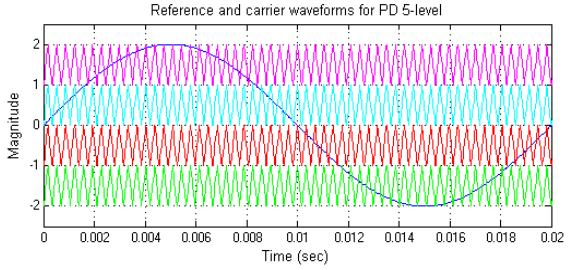


(a)

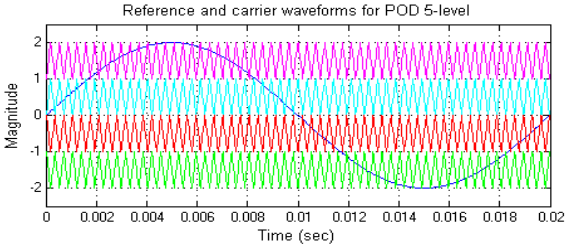
(b)

Fig. 6 Logic gates (a) 5-level; (b) 7-level

There are basically three types of schemes for the level-shifted modulation: (a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD), see Fig. 7:




(a)




(b)

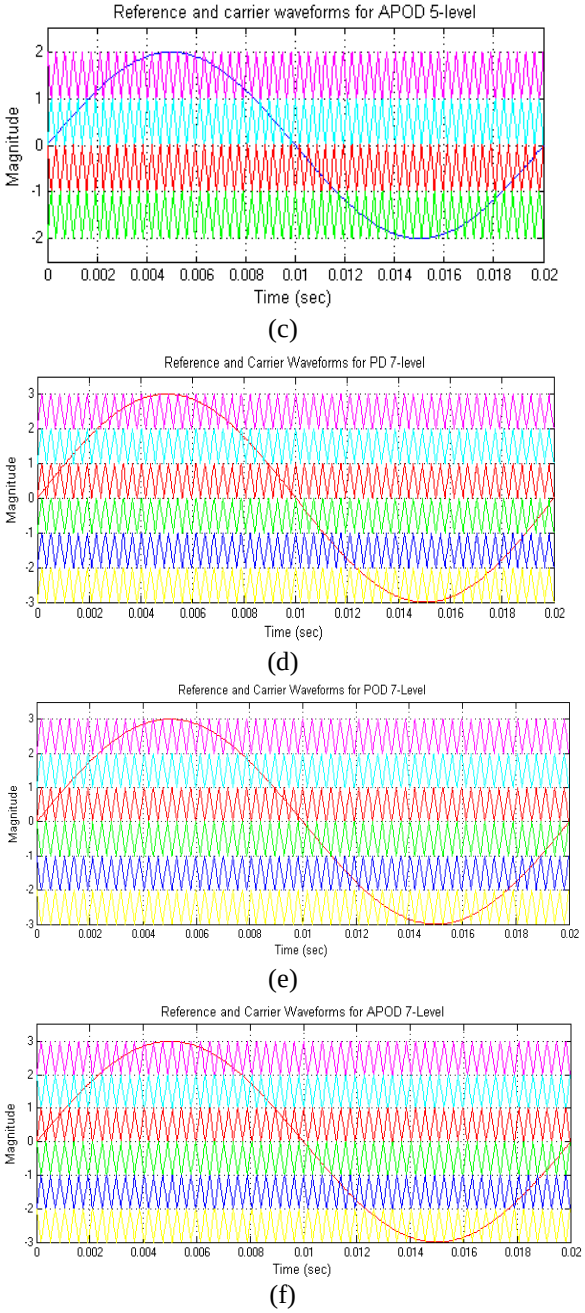



Fig. 7 Reference and carrier waveforms for (a) PD 5-level; (b) POD 5-level; (c) APOD 5-level; (d) PD 7-level; (e) POD 7-level; (f) APOD 7-level

## IV. SIMULATION RESULTS

To show the performance of the proposed DCMLI and CMLI, an adjustable-speed induction motor drive is studied. The proposed converter synthesizes a three-phase multilevel waveform from the calculated switching angles. The MATLAB /SIMULINK is used to simulate 5 & 7-Level DCMLI and CMLI fed induction motor drive, where all parameters and blocks are modeled based on basic concepts. Fig. 8 shows an overview of the simulation model utilized in this work.

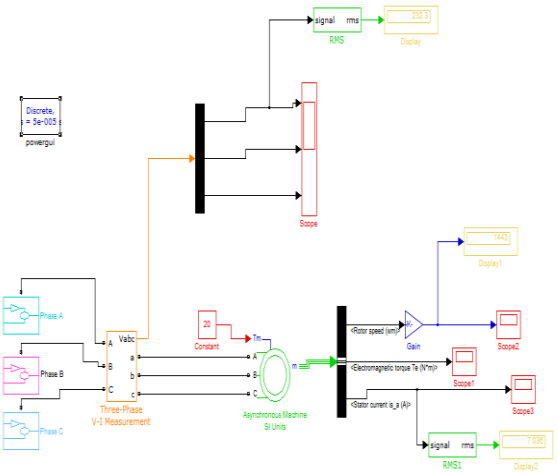


Fig. 8 Proposed Multilevel Inverter Fed Induction Motor Drive

A three phase induction motor is used as a prototype in this work. Parameters of three phase induction motor and the system is shown in Table. 5.

Table. 5 Parameters of three phase induction motor.

| **Parameters of Three Phase Induction Motor** | |
|---|---|
| Rated output power (KW) | 5.4HP (4KW) |
| Frequency (Hz) | 50 Hz |
| Rated Voltage (V) | 400 |
| Stator winding resistance ( Ω ) | 1.405 |
| Stator winding leakage inductance (mH) | 5.839 |
| Rotor winding resistance ( Ω ) | 1.395 |
| Rotor winding leakage inductance (mH) | 5.839 |
| Magnetizing inductance (mH) | 172.2 |
| No. of Poles | 4 |
| Moment of inertia (Kg-$m^2$) | 0.0131 |
| Load Torque Te | 20 Nm |
| Carrier Frequency fc | 2850 Hz |

The output voltage waveform of 5 and 7-level are shown in Fig. 9 and Fig. 10 respectively. The speed, stator winding current and the torque of the induction motor are observed and are shown in Fig. 11, Fig. 12, and Fig. 13 respectively.

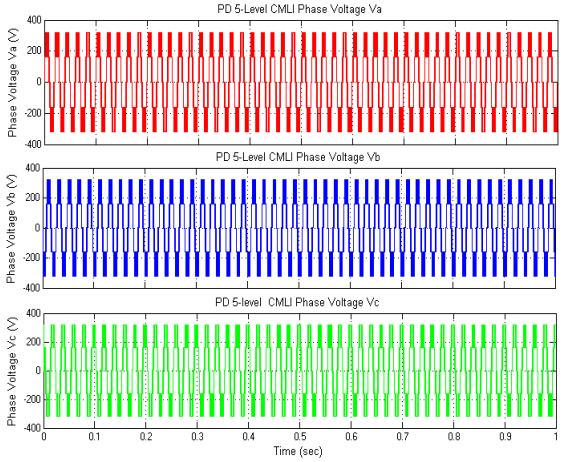



Fig. 9 5-level Output voltage waveform

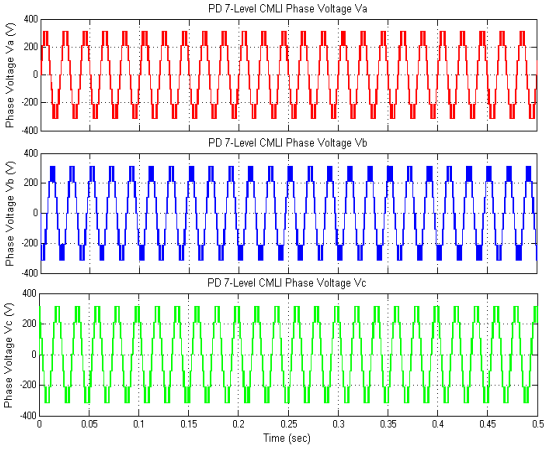



Fig. 10 7-level output voltage waveform

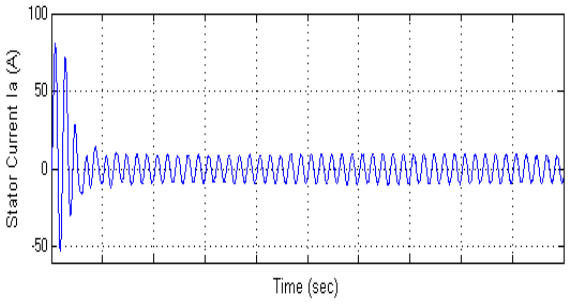



Fig.11 Stator winding current

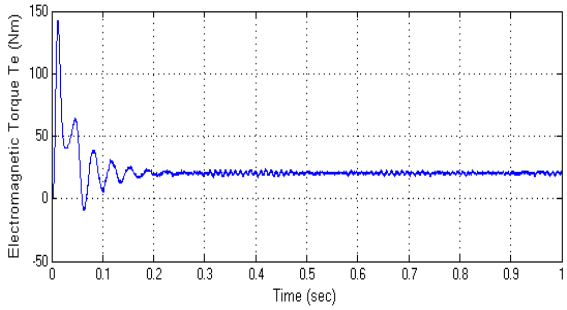



Fig. 12 Electromagnetic torque

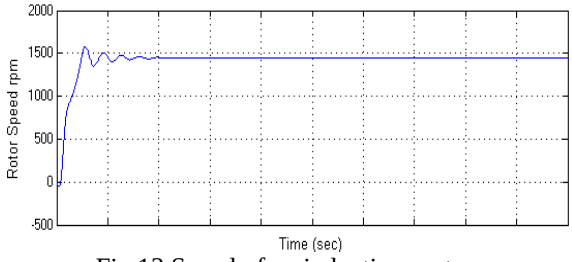



Fig.13 Speed of an induction motor

The THD of the phase voltage Va of both multilevel converter are compared for all the three SPWM technique i.e. PD, POD, APOD and are shown in Table. 6.

Table. 6 Comparison of both multilevel converter in terms of THD%

| Topologies | 5L DCMLI | | | 7L DCMLI | | |
|---|---|---|---|---|---|---|
| SPWM | PD | POD | APOD | PD | POD | APOD |
| THD% | 26.59 | 26.59 | 26.54 | 18.43 | 18.52 | 18.24 |
| Topologies | 5L CMLI | | | 7L CMLI | | |
| SPWM | PD | POD | APOD | PD | POD | APOD |
| THD% | 26.54 | 26.55 | 26.42 | 18.42 | 18.43 | 17.76 |

## V. CONCLUSION

Multilevel inverters can be used instead of two-level inverters to get lower THD and also to lower the switching power losses. However, a higher number of components must be used but these can be of a kind with lower voltage ratings, depending on the number of voltage levels used in the multilevel inverter. It has also been concluded that the CMLI, in general, is the best choice of MLI when it comes to component requirements, and less THD is observed for this topology. The THD of the phase voltage of both converter is studied under different SPWM modulation techniques such as PD, APOD, and POD and the less THD is observed for 7-level CMLI using APOD technique i.e. 17.76%.

## VI. ACKNOWLEDGEMENTS

The authors wish to thank the Management, Principal and the Department of Electrical and Electronics Engineering of KNIT, Sultanpur and Amity University, Noida for their whole hearted support and providing the laboratory facilities to carry out this work.

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