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Modeling and Implementation of Reliable Ternary Arithmetic and Logic Unit Design Using Vhdl

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ABSTRACT
Multivalve logic is a reliable method for defining, analyzing, testing and implementing the basic combinational circuitry with VHDL simulator. It offers better utilization of transmission channels because of its high speed for higher information carried out and it gives more efficient performance. One of the main realizing of the MVL (ternary logic) is that reduces the number of required computation steps, simplicity and energy efficiency in digital logic design. This paper using reliable method is brought out for implementing the basic combinational, sequential and TALU (Ternary Arithmetic and Logic Unit) circuitry with minimum number of ternary switching circuits (Multiplexers). In this the potential of VHDL modelling and simulation that can be applied to ternary switching circuits to verify its functionality and timing specifications. An intention is to show how proposed simulator can be used to simulate MVL circuits and to evaluate system performance.
Keywords: Gate count, MVL, reliability- unreliability model, ternary switching levels, VHDL, Xilinx ISE10.1i.

I. INTRODUCTION

Ternary (3-Valued) logic is operating at 3 switching levels, and it is one of logic in Multi-valued logic or many-value logic. The switch levels of ternary logic are denoted by X may assuming either X^0,X^Z,X^1 where 0,Z,1 signifies logic (voltage) levels per '0' as low voltage level corresponding to low level logic (logic-0), 'Z' corresponding to medium level logic (logic-Z as high impedance also called meta stable state) and '1' corresponding to high/maximum level logic (logic-1). Ternary logic based system have more and important advantage and less requiring computation steps than binary. It has high logic capacity than binary then these logic based design of VLSI circuits are more reliable than binary and in order to bring their full potential into many operational circuits. Here possible for ternary logic to achieve simple and energy efficient in digital logic design.

I.I Previous Design

Details of ternary logic based design by using novel method as multiplexer taking as to build logic blocks [1]. These method based design are more efficient for designing of VLSI circuits.

I.II Present Design

The present work in this paper deals with the use of Very High-Speed Integrated Circuit Hardware Description Language (VHDL) as a logic simulator for evaluate the performance of ternary logic based circuits. Future day's VLSI technology offers ways to realize MVL circuits in order to bring their full potential into many operational levels in circuits. Here presenting a concept to model the ternary combinational ternary arithmetic and logic unit circuits using with minimum number of multiplexers showing the potential and ease in the design of ternary circuits (the multiplexer based designs are also known as novel method for designing of digital circuits) as well as its modelling using Electronic Design Automation (EDA) tool for its performance with respecting to verification of desire functionality of MVL. In this paper Section II reliability and VHDL of ternary algebra. In Section III, Design of Ternary arithmetic and logic unit. Verification and Simulation results of TALU shows in section IV and Conclusion and future work is given in Section V.

I.III Benefits

These benefits have been shown to be useful for the design of ternary computers, for digital filtering. Ternary representation of admits sign convention also.

- Ternary logic is mainly applied in new transforms for encoding and more efficient for compression, error correction, and state assignment, representation of discrete information and in automatic telephony.
- Ternary logic also offers greater utilization of transmission channels because of the higher information content carried by every line. It gives exact and more efficient error detection and correction codes and possesses potentially higher density of information storage.

I.IV Applications

This is the reason for ternary is casting this serial, parallel, serial-parallel and some serial-serial operations can be carried out at higher speed its advantages have been confirmed in the applications field of memory, communication, Machine Learning, Fuzzy logic, Artificial Intelligence, Robotics, Data Mining, Digital signal processing, Digital control systems and Image Processing etc.,.

I.V Advantages

Ternary algebra is an evident advantage of a ternary representation over than binary is economy of digits. To represent a number in binary system, one needs 62.5% more digits than that of ternary and memory of circuit designing is less than binary.

- The main advantage of ternary logic is that it reduces the number of required computation steps for developing digital design.
- Furthermore memory, control unit, and processor can be carried out faster if the ternary logic is easily employed and memory utilization also less than binary [2].

For Example: To represent a 20-digit decimal number one requires 40 ternary digits instead of 65 binary digits.

II. RELIABILITY AND VHDL FOR TERNARY ALGEBRA

II.I Reliability for Ternary Algebra:

The Reliability-Unreliability model is sufficient enough to support the decision methodology statistically as shown in Fig. 1 Mathematically, it implies that reliability will be interpreted by the inequality $0 \leq R \leq 1$. If R=1, it is interpreted to be absolutely true and if R=0, it is interpreted to be absolutely false. If R being in the vicinity of 0.5 could be interpreted as neither true nor false and above 0.5 is said to be reliability level and below 0.5 is said to be unreliability level. In VLSI circuits' designing of basic formula,

$$P = (V_{dd} C F)/2 \text{-----}> \quad (1)$$

The equation (1) is applied to ternary logic then the reducing number of logic gates as per representation of computation steps of logic circuits then reducing chip area, chip delay and power utilization.

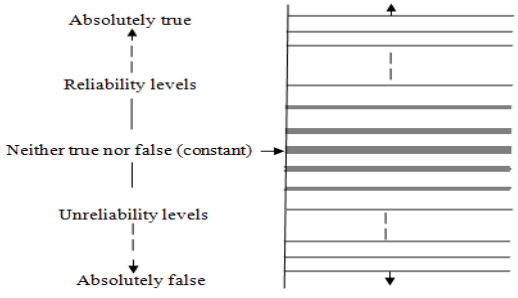


Figure 1: Truth value based on reliability-unreliability model

II.II VHDL for Ternary Algebra:

Table 1: Nine-State logic system

Symbols	Values
U	Uninitialized
X	Unknown
-	Don't care
L	Weak 0
H	Weak 1
W	Weak unknown
0	Logic 0
1	Logic 1
Z	High impedance/Meta stable

In present work VHDL can be used to model, simulate and describe ternary system where signals inside the circuit can take tri state logic. The present VHDL simulator are only provide to develop and it can be used to synthesize & to verify the performance of ternary logic circuits with the help of technology dependent package called Nine-state StdLogic_1164 package whose levels are listed in Table 1 which allows the description of circuits based on TTL, CMOS, GaAs, NMOS, PMOS and ECL devices. To demonstrate the use of VHDL as a ternary logic simulator, we have used Logic-0 to represent 0 volt, High impendence Z to represent 0.5 volt and Logic-1 to represent 1 volt.

VHDL provides an effective way to connect several logic outputs to a single input, where all but one is forced to the high impedance state, allowing the remaining outputs to operate in the normal binary sense [3]. This concept is commonly used for memory bank for connection in computers and other similar devices to a common data bus where a large number of devices can communicate over the same channel, simply by ensuring only one is enabled at a time.

III. DESIGN OF TERNARY ALU

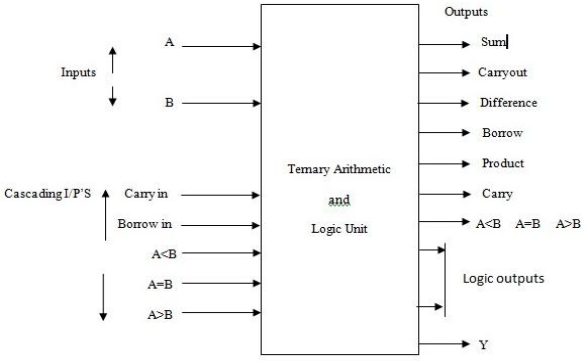


Figure 2: Block diagram of Ternary ALU

In this paper, TALU (ternary arithmetic and logic unit) is develop by using logic unit as overall (complete) logic gates and arithmetic unit for performance of addition, subtraction, multiplication, comparison from adder part, sub tractor part,

multiplier, comparator are 3x1 MUX is taken as a basic building block to explore the realization of circuits with minimum number of ternary 3X1 MUX (Multiplexer) and the outputs of two unit parts are represents in 81x1 MUX with techniques of Electronic Design Automation tools. The design concept is implemented based on ternary K-map method for ternary function minimization.

Here Design of Realized TALU is based on ternary Multiplexers for logic gates minimization. The block diagram of Ternary ALU is shown in Fig. 2 Here A, B are inputs and carry in, borrow in, A<B, A=B, A>B are cascading inputs (in outs) then getting Sum (S1), Carry out (C out), Subtraction (D0, D1), Borrow (B out), Multiplication (product), C out (Carry), A<B A>B A=B as comparator responses and Logical outputs as responses of ternary basic logic gates [4].

III.I Design of Arithmetic Unit

In this paper arithmetic unit consider to follow by some rules, previous paper worked on its design. But here verifying its design, functionality and simulation results are shown in section V.

III.I.I Design of Ternary Adder and Ternary Subtractor

In this paper considering for addition and subtraction performances should taking 2 bit inputs and in these one are ternary adder circuit that will add 2 ternary full adders and generate outputs Sum0 (S0), Sum1 (S1), Carry out(C out) and Carry in(C in) as inout for ternary full adder 1 to ternary full adder 2. Fig. 3 shows block diagram of ternary adder module. Similarly, Ternary full subtractor circuit that will add 2 ternary full subtractors and generate outputs difference0 (D0), difference1 (D1), borrow out (B out) and borrow in (B in) as in out for ternary full subtractor 1 to ternary full subtractor 2. Fig. 4 shows block diagram of ternary subtractor module.

III.I.I.I Design of Full Adder & Full Subtractor using 3x1 Multiplexer

A full adder (FA) is a circuit that will add three bits and generates a sum and a carry, Fig. 5 shows the design of FA. Similarly, Full Subtractor (FS) is a circuit that will subtract three bits (i.e., (A_1-(B_1-Bin)), and generates a difference and borrow. Fig. 6 shows the design of FS.

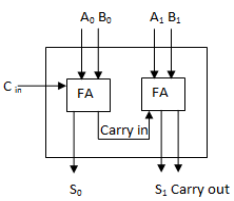


Figure 3: Ternary Adder

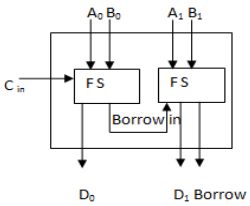


Figure 4: Ternary Subtractor

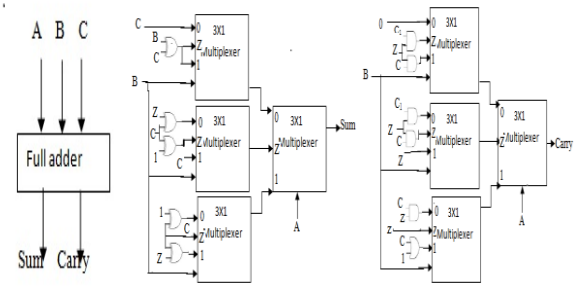


Figure 5: Block and circuit Diagrams for Ternary Full adder

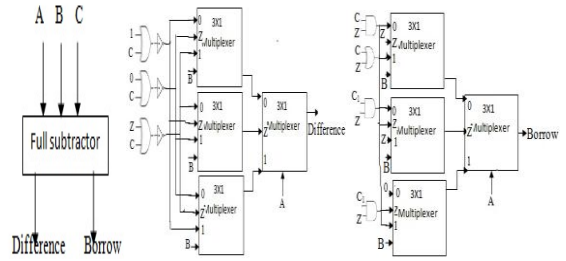


Figure 6: Block and circuit Diagrams for Ternary Full subtractor

III.I.II Design of Multiplier using 3x1 Multiplexer

In this Multiplier multiplies two bits and generates the product and carry as shown in the structural modelling is design using 3x1 multiplexer in Fig. 7.

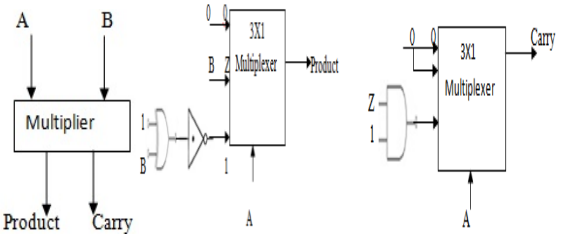


Figure 7: Block and circuit diagrams for one bit Ternary Multiplier

III.I.III Design of Comparator using 3x1 Multiplexer

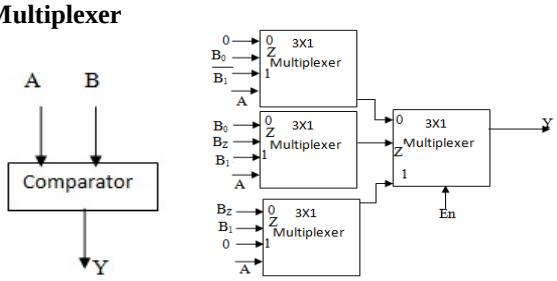


Figure 8: Block and circuit diagram for one bit Ternary comparator

In this is a magnitude comparator is a combinational circuit that compares two bits A & B and determines their relative magnitudes. The comparison of two bits is an operation that determines if one number is greater than, less than or

equal to other number. The design of 1-bit comparator is shown in Fig. 8. It gives Y=f(A>B) when en=0, Y=f(A=B) when en=1 and Y=f(A<B) when en=2.

III.II Design of 3x1 Multiplexer

These are multiplexer based designing also known as novel method for Digital logic design. In ternary algebra it is an approach for implementing ternary function is to convert given ternary variable into unary variable using ternary to unary decoder as shown in Fig. 9. A decoder shown in Fig. 10 is a combinational circuit that converts the ternary information from n input lines to a maximum of 3^n unique output line and its functionality was verified.

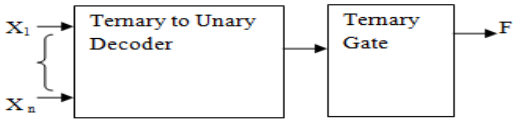


Figure 9: Implementation of ternary function

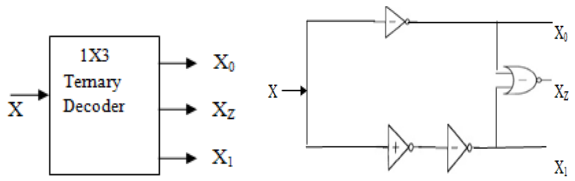


Figure 10: Block and Circuit diagram for 1X3 Ternary Decoder

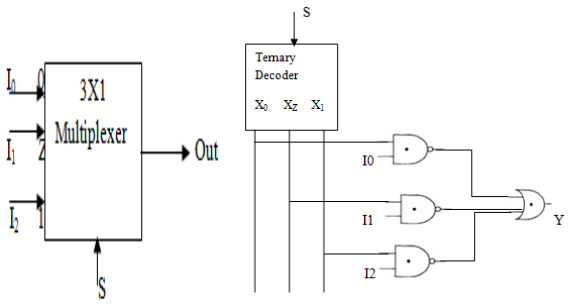


Figure 11: Block and circuit diagrams of 3X1 Ternary Multiplexer

A ternary multiplexer is a combinational circuit that selects one of the 3^n input lines based, on a set of n selection lines and directs it to a single output line. Normally, there are 3^n inputs which come from a decoder and n select lines whose bit combinations determine which input to select. The design of 3X1 multiplexer (MUX) is as presented in Fig. 11.

III.III Design of Logic Unit

Previous papers are developed some of ternary logic gates. But here, to proposed complete logic gates in ternary algebra and these are shown in Fig. 12 and the logic unit performs complete logic gates in ternary algebra. These are analyzing to developing by previous papers.

III.IV Design of 81x1 Multiplexer using 3x1 Multiplexer

In this project 3x1 MUX is taken as a basic building block to explore the realization of 81x1 MUX in which we have the four selection lines and Fig. 13 shows the 81x1 MUX. This is using for representing the outputs of ternary arithmetic and logic unit.

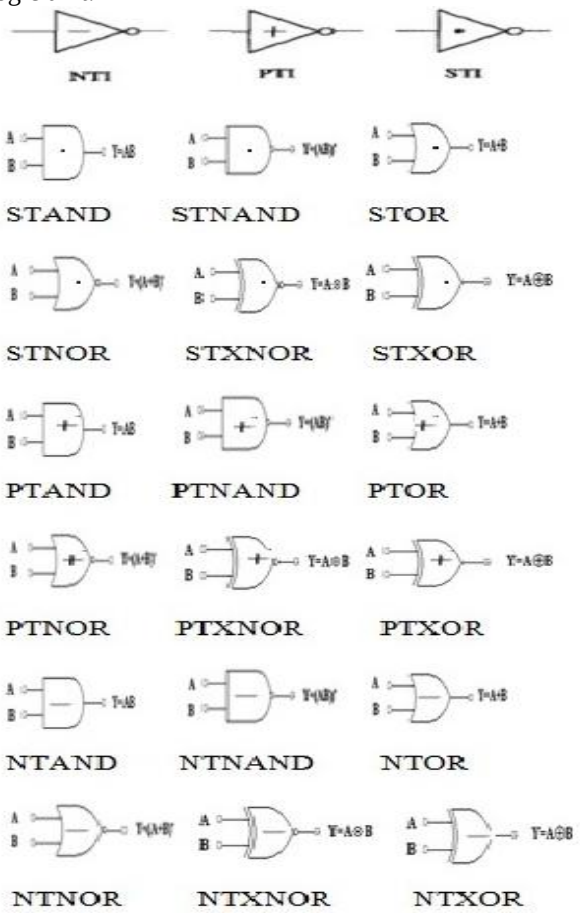


Figure 12: Symbols for basic ternary logic gates

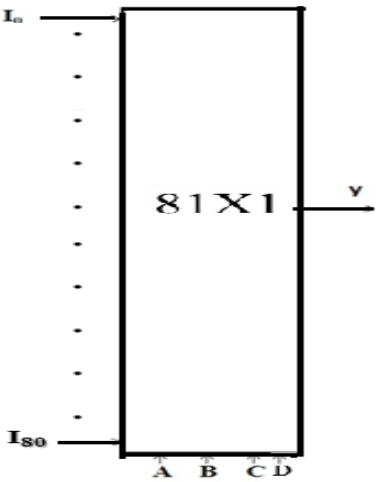
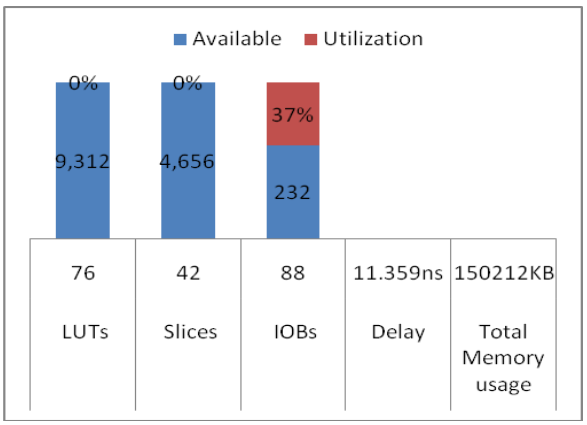


Figure 13: Block diagram of 81x1Ternary Multiplexer

III.V Utilization of Reliable TALU

Table 2: Utilization levels of TALU

Logic utilization	Used	Available	Utilization
Number of 4 input LUTs	76	9,312	0%
Number of occupied Slices	42	4,656	0%
Number of bonded IOBs	88	232	37%
Delay	11.359ns		
Delay for Logic	7.891ns	11.359ns	69.50%
Delay for Route	3.468ns	11.359ns	30.50%
Total Memory usage	150212KB		



Graph 1: Utilization of reliable TALU

Here calculating device utilization level in terms of percentage and time taken execution (delay) for the outputs also delay for logic and routing as shown in Table 2. In above table represents details for calculation utilization of reliable TALU and graph1 is shows the representation of utilization of reliable TALU.

IV. SIMULATION RESULTS FOR TERNARY ALU

The proposal design of Ternary Arithmetic and Logic unit (TALU) is verifying by its functionality using Xilinx ISE 10.1i, ISIM simulator. The package of ternary types is developed by using previous paper [5]. Here A, B and C $_{in}$ giving inputs are to verifying functionality of Ternary basic logic gates as A, B is (‘z’ ‘0’) and (‘z‘ ’0’) then getting response at the current simulation time 300ns subtractor part of D0, D1and B1 responses are ‘z’, ‘1’ and ‘z’ respectively as shown in Fig. 14.

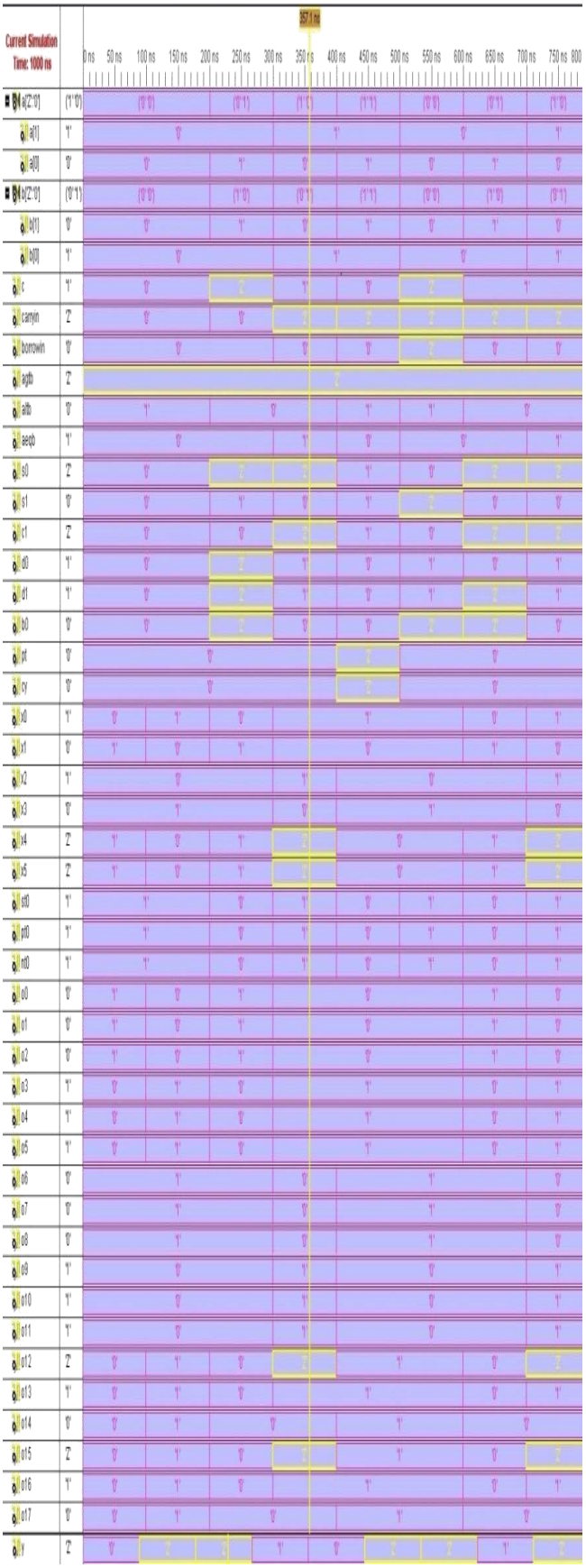


Figure 14: Simulation results of Ternary Arithmetic and Logic Unit

V. CONCLUSION

Ternary logic based design are having higher information carrying capacity than binary. Thus, ternary logic gate design technique also provides an excellent speed and power consumption characteristics in data path circuit such as full subtractor and full adder. Ternary logic provides means of increasing data processing capability per unit chip area. The main advantages of ternary logic are that it reduces the number of required computation steps. The number of digits required in a ternary family is $\log_3 2$ times less than that required in binary logic. In this paper, reliable TALU (Ternary Arithmetic Logic Unit) are designed with minimum number of ternary multiplexers. In these work confirmed to say ternary logic based designs are having less memory, power and delay than binary for addition, subtraction, multiplication and comparisons are should involving number of operations to verifying the functionality. But in binary logic based those operation should perform simply only one operation having more memory and slight greater delay. In this proposed work developed complete ternary algebra basic logic gates, 81X1 multiplexer and also synthesizes delay for logic and routing of TALU, device utilization. VHDL simulator has been used to simulate Ternary logic based Systems which provide enough information to verify functionality and timing specifications.

VI. ACKNOWLEDGEMENT

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BIOGRAPHIES

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