RESEARCH ARTICLE OPEN ACCESS

Two Stage Fully Differential Sample and Hold Circuit Using .18µm Technology

Dharmendra Dongardiye*, Rajesh Khatri **
*. M. Tech Scholar, Department of Electronics & Instrumentation, Shree G.S.I.T.S Indore, India
**Associate Professor, Department of Electronics & Instrumentation, Shree G.S.I.T.S Indore, India

Abstract
This paper presents a well-established Fully Differential sample & hold circuitry, implemented in 180-nm CMOS technology. In this two stage method the first stage give us very high gain and second stage gives large voltage swing. The proposed opamp provides 149MHz unity-gain bandwidth , 78 degree phase margin and a differential peak to peak output swing more than 2.4v. using the improved fully differential two stage operational amplifier of 76.7dB gain. Although the sample and hold circuit meets the requirements of SNR specifications.

I. Introduction

Sample-and-hold (S/H) circuits play an important role in the design of data-converter systems. They can greatly minimize errors due to slightly different delay times. However, when designing S/H circuit for low supply voltage operation, quite quickly we encounter a severe difficulty: the switch-driving problem. In the literature, there are several solutions to solve the problem. These approaches include using on-chip clock voltage doublers, multi-threshold voltage process, bootstrapped switch circuit, and switched-opamp technique.

However, when the threshold voltage of device is lowered, it will suffer from an unacceptable amount of leakage current during off state of the switch. A second approach is the use of on-chip clock voltage doubler. At first it is necessary to mention some factors which affect the performance of the SHA circuit.

1. Sampling pedestal (hold step): this error occurs when the circuit switches from sampling mode to the holding mode. It is important to know that this error must be independent from input signal. This error may cause nonlinear distortion.
2. The speed at which a sample and hold can track an input signal in sample mode. This parameter is limited by the slew rate and the -3db bandwidth in both small signals and large signals. It is necessary to maximize SR and 3*db* for high speed performance.
3. Aperture jitter (aperture uncertainty): this error is the result of effective sampling time changing from one sampling instance to the next and becomes more pronounced for high speed signals. Specifically, when high speed signals are being sampled, the input signal changes rapidly, resulting in small amounts of aperture uncertainty causing the held voltage to be significantly different from the ideal held voltage.

In this paper, we present a new design strategy to develop a CMOS Fully differential sample-and-hold circuit. The architecture is the extension and modification of opamp-reset switching technique. The organization of this paper is as follows: the design of the conventional Sample and Hold circuit is explained in section I and the circuit implementation with 0.18µm CMOS process is presented in section II and III. In section IV we discuses about the switched capacitance common mode feedback circuit , the simulation results are given and discussed in section V .The conclusions are presented in section VI.

A conventional S/H circuit shown below

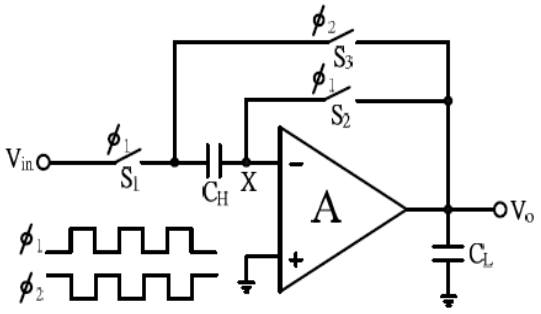


Fig No. 1 conventional Sample and Hold circuit

II. CIRCUIT DESIGN

To choose the appropriate architecture for opamp, one should first notice the requirements of the system.

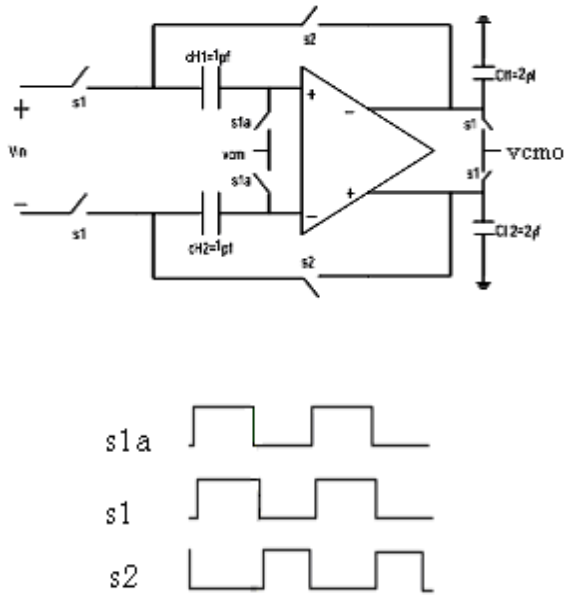


Fig No. 2 Proposed fully differential Sample and Hold Circuit

A. The proposed two stage cascode opamp

The gain of this topology is limited to the product of the input pair transconductance and the output impedance. It has also observed that cascoding in such circuits increases the gain while limiting the out put swings.

B. One Stage Folded Cascode

This architecture provides better input common mode range and better output swing. Furthermore, this structure provides the capability of selecting the required overdrive voltage for input transistors to achieve the unity-gain frequency without the output swing limitation. Higher input referred noise and higher power dissipation are some of its disadvantages.

C. Two Stage Opamp

In two stage opamps, the first stage provides a high gain and the second large swings. In contrast to cascode opamps, a two stage configuration isolates the gain and swing requirements. Each stage can incorporate various amplifier topologies, but in order to allow the maximum output swings, the second stage is typically configured as a simple common source stage.

It is important that the structure has less power dissipation rather than folded cascode. For the main body of the two stage opamp both fully differential telescopic cascode and fully differential folded cascode are possible; but each of them has advantages and defects.

Due to the advantages and disadvantages of the structures mentioned above, a two stage cascode fully differential opamp is considered.

Generally, in two stage circuits, when transistors of the first stage are Pmos, transistors of the second stage are selected Nmos type and vice versa. But in the proposed opamp, both stages are selected Nmos. This structure leads to higher gain, desired output swing and acceptable bandwidth; but it has its own challenges such as: high impedance nodes that limit the unity gain bandwidth and increase the complexity of compensation techniques and biasing. Therefore, in this paper Miller compensation is applied.

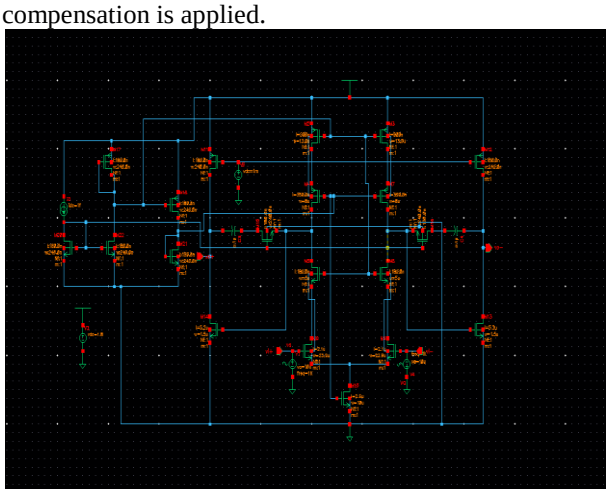


Fig No 3. The proposed two stage cascode opamp

III. DESIGN PROCEDURE

For high gain designs, two-stage configuration might be the appropriate choice; however, the speed of this configuration is the bottleneck. In this design, a fully differential folded cascode that has two fully differential folded cascode boosting amplifiers has been implemented as shown in Fig.3. In the design process, NMOS transistors give about 4 times better transconductance compared to the same size PMOS transistors; this motivates us to reduce the number of PMOS transistors as much as possible. Since low common mode input is desired to avoid extra digital power consumption due to big PMOS switches, the input differential pair of the opamp was chosen to be PMOS transistors. It has a switched capacitor CMFB circuit that is active when the opamp is in the holding mode and a continuous time CMFB that is active when the opamp is in the sampling mode. The boosting amplifiers have a continuous time CMFB circuits. The boosting amplifiers are of two types: the AN gain boosting amplifier has an NMOS differential input stage, while the AP has a PMOS differential input stage. The ideal effect of the auxiliary op amp is to increase the output impedance of the main op amp by auxiliary times so as to improve the dc gain of the

main op amp; at the same time, the dominant pole of the main opamp is pushed down by auxiliary opamp.

The sizing of the proposed fully differential opapm are shown

Transistor	Width(µm)	Length(µm)
M1,M2	23.9	2.1
M3,M4	5	.18
M5.M6	8	.35
M7,M8	13	.9
M9	10	2.6
M10,M11	.24	.18
M12,M13	1.5	5.2
M14,M15	.24	.18

IV. DESIGN OF CMFB CIRCUIT

Fully differential opamp has much advantage, for example, greater output swing, avoid mirror poles eliminating even order distortion and reject noise from the substrate, it has a drawback that it must have a common-mode feedback (CMFB) circuit. The CMFB circuit will enable the op amp to have a common mode output voltage that is immune to variations in the process as well as temperature. It is often the most difficult part of the op amp to design. CMFB circuits can be divided into two general categories: switched capacitor CMFB (SC-CMFB) circuits and continuous-time CMFB circuits. Compare to continuous time CMFB, SCCMFB consumes less power. Because the opamp is used in sample and hold circuit, non overlapping phase clocks are available. The SC-CMFB is adopted which is shown in Fig 4

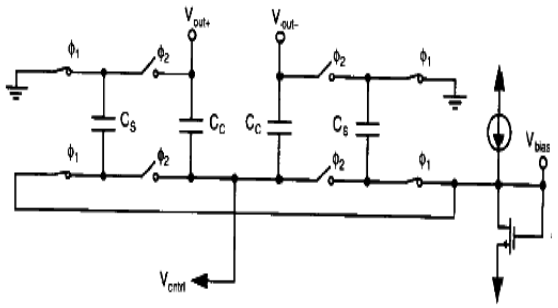
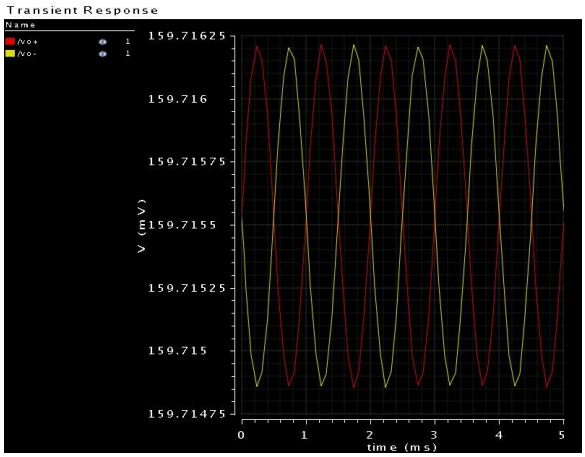
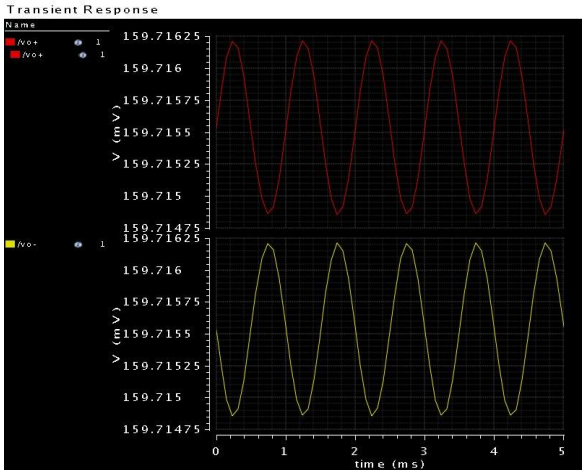


Fig no 4.switched capacitance common mode feedback circuit

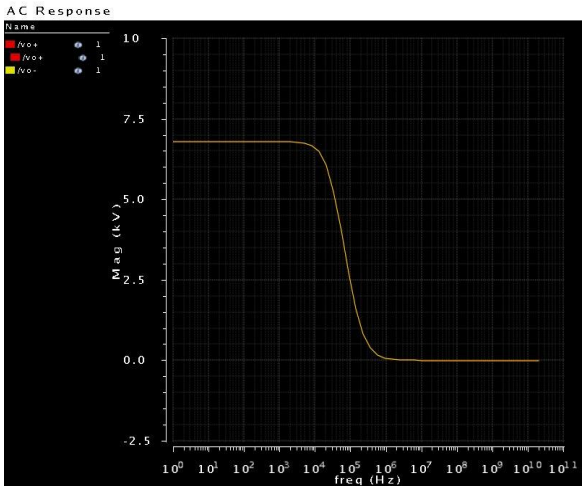
V. SIMULATION RESULTS USED OPAMP

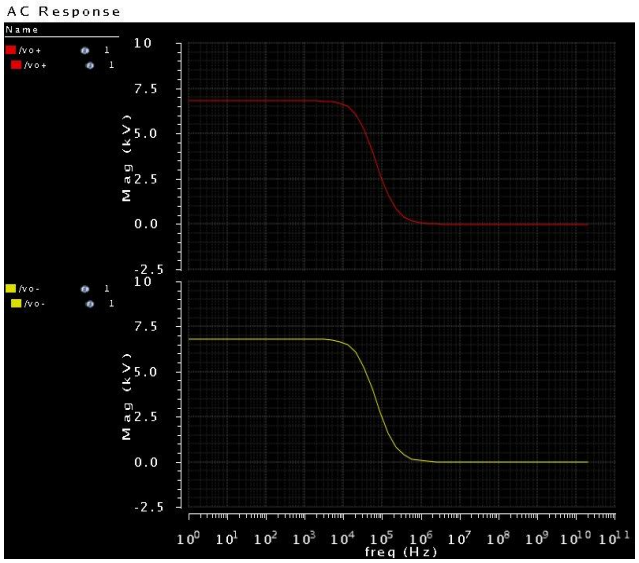
A. TRANSIENT ANALYSIS



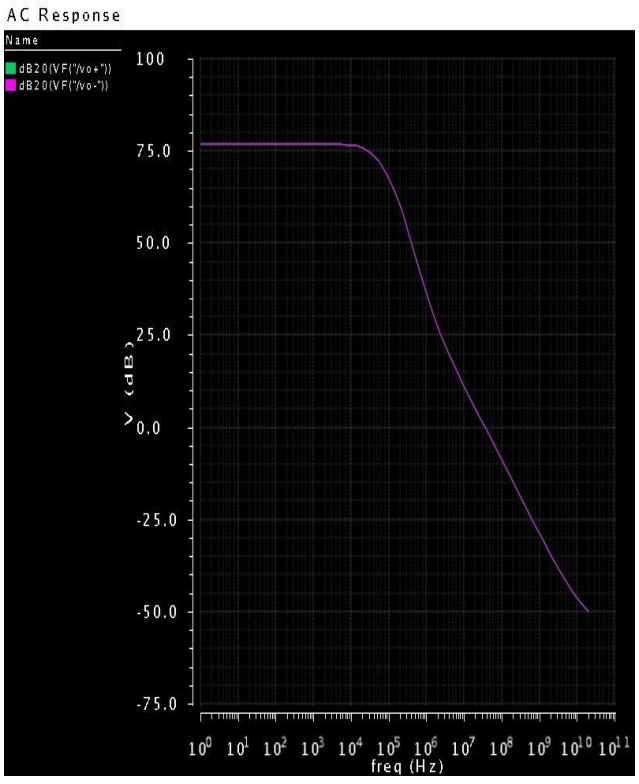


B.AC ANALYSIS





C. GAIN PLOT



VI. CONCLUSION

In a Two stage Fully differential sample and hold architecture we recover the problem of the lower gain and the higher voltage swing issue. In this architecture we get 68 db dc gain and the CMRR of the propose opapm is around 50db. It has larger voltage swing. This architecture with some modifications can be used for low-voltage algorithmic A/D converter and pipelined A/D converter. Further research of this architecture is in progress.

VII. ACKNOWLEDGMENT

The authors would like to thank SGSITS INDORE and SMDP to provide the license of the CADENCE software.

REFERENCES

[1] DAI, L., and HARJANI, R.: 'CMOS switched-op-amp-based sample-and-hold Circuit', IEEE J. Solid-State Circuits, January 2000, vol. SC-35, pp. 109-113.

[2] M. Keskin, U. Moon, and G. Temes, "A 1-V 10MHz clock-rate 13-bitCMOS Δ Σ modulator using uni ty-gain-reset opamps," IEEE J. Solid-State Circuits, vol.37, pp. 817-824, Jul. 2002.

[3] M. Waltari and K. Halonen, "Bootstrapped switch without bulk effect in standard CMOS technology," Electron. Lett., 2002, 38, (12), pp. 555-557

[4] D. Chang and U. Moon, "A 1.4-V 10-bit 25-MS/s pipelined ADC using opamp-reset switching technique," IEEE J. Solid-State Circuits, vol.38, pp. 1401-1404, Aug. 2003.

[5] B. Razavi, Principles of Data Conversion System Design, IEEE Press, 1995.

[6] R. Schreier, J. Silva, J. Steensgaard, and G. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 11, pp. 2358–2368, Nov. 2005.

[7] Baschirotto, R. Castello, and G. Montagna, "Active series switch for switched-opamp circuits," Electron. Lett., vol. 34, no. 14, pp. 1365-1366, Jul. 1998.

[8] Sai-Weng Sin, Seng-Pan U, and R. P. Martins, "A novel low-voltage cross-coupled passive sampling branch for reset- and switched-opamp circuits," in Proc. IEEE International Symposium on Circuits and Systems, vol. 2,May 2005, pp. 1585-1588.

[9] P. W. Li, M. J. Chin, P. R. Gray and R. Castello, "A ratio-independent algorithmic analog-to-digital conversion technique," IEEE Journal of Solid-State Circuits, vol. 19, no. 6, pp. 828-836, Dec 1984.

[10] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," IEEE Trans. Circuits and Systems-II, vol. 45, pp. 769-780, July 1998.

[11] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog

Integrated Circuits, 4th ed., New York: John Wiley & Sons, Inc., 2001, pp. 849-850.

[12] Loloee, A. Zanchi, H. Jin, S. Shehata, E. Bartolome, "A 12b 80MSps Pipelined ADC Core with 190mV Consumption from 3 V in 0.18um Digital CMOS'', ESSCIRC, 2002.

[13] T. S. Lee, C. C. Lu, S. H. Yu, and J. T. Zhan, "A very-high-speed low-power low-voltage fully differential CMOS sample-and-hold circuit with low hold pedestal ," Proceedings of 2005 IEEE International Symposium on Circuits and Systems, Kobe, Japan, vol. 4, pp. 3111-3114, 2005.

[14] B. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. Pister, "An ultra-low power 2.4 GHz RF transceiver for wireless sensor networks in 0.13 _m CMOS with 400 mV supply and an integrated passive RX front-end," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2006, pp. 1460–1469.

[15] A 0.5-V 1-Msps Track-and-Hold CircuitWith 60-dB SNDR Shouri Chatterjee and Peter R. Kinget, Senior Member, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 4, APRIL 2007

[16] S. Narendra, J. Tschanz, J. Hofsheier, B. Bloechel, S. Vangal, Y. Hoskote, S. Tang, D. Somasekhar, A. Keshavarzi, V. Erraguntla, G. Dermer, N. Borkar, S. Borkar, and V. De, "Ultra-low voltage circuits and processor in 180 nm to 90 nm technologies with a swapped-body biasing technique," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, 2004, pp. 156–157.

AUTHORS

Dharmendra Dongardiye has 1 years of Teaching experience and presently pursuing MTech in Micro Electronics & VLSI Design in SGSITS Indore, India .He received his Bachelor of Engineering in Electronics and Communication from Globus Engineering college Bhopal,India in 2011.

Mr. Rajesh Khatri has 20 years of Teaching experience and presently working as Associate Professor in Department of Electronics & Instrumentation Engineering at SGSITS Indore. He received his Bachelor of Engineering in Electronics and Communication from SGGS Institute of Technology Nanded, India in 1990. He received his Master of Engineering in Instrumentation from SGGS Institute of Technology Nanded, India in 1995.