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Recovery Boosting Technique for Improving Nbti Recovery in 6t Sram Cells

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ABSTRACT
Negative bias temperature instability (NBTI) is an important lifetime reliability problem in microprocessors. SRAM based structures within the processor are especially susceptible to NBTI since one of the pMOS devices in the memory cell always has an input of "0". Previously proposed recovery techniques for SRAM cells aim to balance the degradation of the two pMOS devices by attempting to keep their inputs at a logic "0" exactly 50% of the time. However, one of the devices is always in the negative bias condition at any given time. In this paper, proposed technique called Recovery Boosting that allows both pMOS devices in the memory cell to be put into the recovery mode by slightly modifying to the design of conventional SRAM cells. To evaluate the circuit-level design of a physical register file and an issue queue that use such cells through SPICE-level simulations. To conduct an architecture-level evaluation of the performance and reliability of using area-neutral designs of these two structures. To show that Recovery Boosting provides significant improvement in the static noise margins of the register file and issue queue while having very little impact on power consumption and performance

Keywords: NBTI, PMOS, SRAM, Recovery boosting,SPICE-level simulation

I. INTRODUCTION

Computers and many electronic gadgets usually rely on stored information which is mainly data which can be used to direct circuit affections. The digital information is stored in memory devices. There are two types of memories based on what memory cells can be accessed at a given instant. SAM (Sequentially Access Memory) is accessed by stepping through each memory location until the desired location is reached. Magnetic tape is an example of SAM. The second category of memory devices is called RAM (Random Access Memory) where the memory can be randomly accessed at any instant. Compared to SAM the access time is to be faster. Most of the electronic gadgets memories are of RAM type.

One important hard error phenomenon is negative bias temperature instability (NBTI), the lifetime of the pMOS transistor is affected.

NBTI occurs when a negative bias (i.e., a logic input of "0") is applied at the gate of a pMOS transistor.

The negative bias can lead to the generation of interface traps at the Si/SiO2. Interface, which cause an increase in the threshold voltage of the device. This increase in the threshold voltage degrades the speed of the device and reduces the noise margin of the circuit. One interesting aspect of NBTI is that some of the interface traps can be eliminated by applying a logic input of "1" at the gate of the pMOS device. This puts the device into what is known as the recovery mode. Memory arrays that use static random access memory (SRAM) cells are especially susceptible toNBTI. SRAM cells consist of cross-coupled inverters that contain pMOS devices. Since each memory cell stores either a "0" or a "1" at all times, one of the pMOS devices in each cell always has a logic input of "0." All modern processor cores are composed of several critical SRAM-based structures, such as the register file and the issue queue, so there is an important impact of NBTI on these structures to maximize their lifetimes.

II. OVERVIEW OF NBTI

At the time of oxidation of silicon, most of the Si atoms at the surface of the wafer bond with oxygen while a few atoms bond with hydrogen. When a negative bias (i.e., a logic input of "0") is applied at the gate of a pMOS transistor (Vgs=-Vdd), the relatively weak Si-H bonds get disassociated, leading to the generation of interface traps at the Si/SiO2 interface. These interface traps cause the threshold voltage (Vt) of the pMOS increase, which in turn degrades the speed of the device and the noise margin of the circuit, eventually causing the circuit to fail. The period of time when the pMOS transistor is negatively biased is known as the stress phase or stress mode.

The main contributions of this paper are given here.

- SRAM cells can be modified to support recovery boosting and discuss several circuit and microarchitecture-level design considerations when using such cells to build SRAM arrays.

• We present the circuit-level design of two large SRAM arrays in a four-wide issue processor core—the physical register file and the issue queue—that use the modified cells to provide recovery boosting. We verify the functionality of these designs and quantify their area and power consumption through SPICE-level simulation using the Cadence Virtuoso Spectre Circuit Simulator1 for the 32-nm process technology. We show that the modified SRAM structures impose only a 3%–4% area overhead over the baseline non recovery boost designs and that their maximum power consumption is less than 2% over the baseline.

• We then evaluate the performance and reliability of area neutral designs of these modified structures at the architecture-level via execution-driven simulation using the M5 simulator and the SPEC CPU2000 benchmark suite2in nominal operating condition. We show that recovery boosting provides a 56% improvement in the static noise margin of the register file cells and a 48% improvement for the issue queue across the benchmark suite while having a negligible impact on performance.

III. EFFECT OF NBTI

Negative Bias Temperature Instability (NBTI) is a key reliability issue in MOSFET. It is of immediate concern in p-channel devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism affects also NMOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate too. NBTI manifests as an increase in the threshold devices and consequent decrease in drain current and transconductance. The degradation exhibits logarithmic dependence on time.

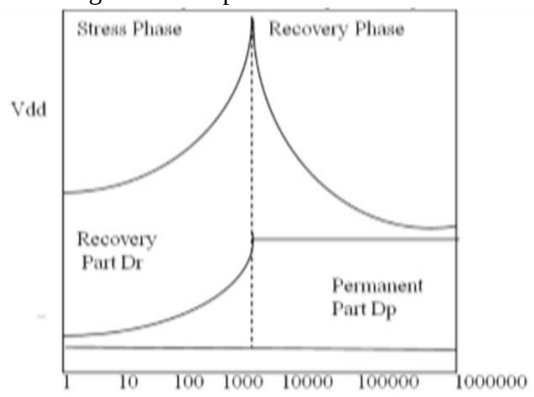

Fig.1.Vth increase with negative bias,Vgs= -Vdd but recover with zero bias,Vgs=0

In the sub-micrometer devices nitrogen is incorporated into the silicon gate oxide to reduce the gate leakage current density and prevent the boron penetration. However, incorporating nitrogen enhances NBTI. For new technologies (32 nm and shorter nominal channel lengths), high-k metal gate stacks are used as an alternative to improve the gate current density for a given equivalent oxide thickness (EOT). Even with the introduction of new materials like hafnium oxides .It is possible that the interfacial layer composed of nitride silicon dioxide is responsible for those instabilities. This interfacial layer results from the spontaneous oxidation of the silicon substrate when the HK is deposited. To limit this oxidation, the silicon interface is saturated with N resulting in a very thin and nitrided oxide layer It is commonly accepted that two kinds of trap contribute to NBTI:

3.1Interface traps- These traps cannot be recovered over a reasonable time of operation. Some authors refer to them as permanent traps. Those traps are the same as the one created by Channel Hot Carrier. In the case of NBTI, it is believed that the electric field is able to break Si-H bonds located at the Silicon-oxide interface. H is released in the substrate where it migrates. The remaining dangling bond Si-(Pb center) contributes to the threshold voltage degradation.

3.2Preexisting traps-on top of the interface states generation some preexisting traps located in the bulk of the dielectric (nitrogen related), are filled with holes coming from the channel of PMOS. Those traps can be emptied when the stress voltage is removed. This Vth degradation can be recovered over time.

The existence of two coexisting mechanisms created a large controversy, with the main controversial point being e for hole trapping in the bulk of dielectrics. A tight coupling between two mechanisms may exist but nothing is demonstrated clearly. With the introduction of High K Metal gates, a new degradation mechanism appeared. The PBTI for Positive Bias Temperature Instabilities affects nMOS transistor when positively biased. In this particular case, no interface states are generated and 100% of the Vth degradation may be recovered. Those results suggest that there is no need to have interface state generation to trapped carrier in the bulk of the dielectric.

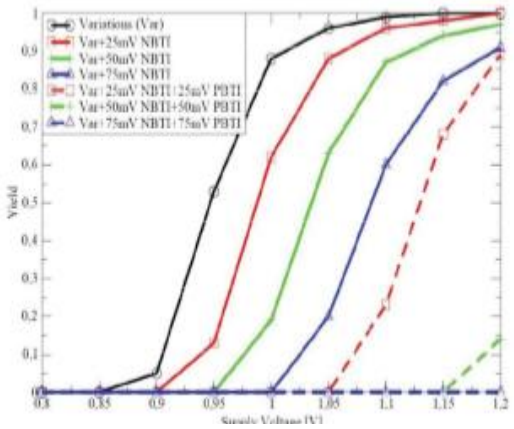

Fig.2. Impact on SRAM

IV. SOLUTIONS FOR NBTI

There are two basic solutions for NBTI:

1) Reduce the stress on the pMOS transistors

2) Enhance the recovery process.

Stress reduction techniques aim to reduce the aging rate by controlling Vdd, Vt and temperature. And recovery enhancement techniques aim to increase the recovery time for the pMOS devices. Recovery boosting is a recovery- enhancement technique for SRAM structures.

4.1Stress Reduction Technique

Stress reduction technique shows that aging mechanisms at runtime based on the operating conditions and use dynamic reliability management (DRM) to stay within the reliability budget. The use of stress reduction techniques is orthogonal to the use of recovery enhancement. Stress reduction techniques aim to reduce the aging rate by controlling Vgs, Vt and temperature. The another technique is recovery enhancement technique.

4.2.Recovery Enhancement Technique

In these devices is used to increase the recovery time for pMOS transistors in logic structures during idle periods and balance the degradation of the pMOS devices in SRAM- based memory structures when they hold invalid data. In this technique to periodically flip the contents of SRAM cells to balance the wear on the pMOS transistors. Recovery enhancement technique for caches where SRAM cells are put into the recovery mode. They reverse bias the pMOS devices to put them into a deep recovery state. When an array is put into the recovery mode, all the pMOS devices in any one of the inverters in all of the cells are put into the recovery mode followed by those in the other array. All of these recovery enhancement techniques aim to balance the degradation of the two pMOS devices in the memory cell by attempting to keep the inputs to each device at a logic input of "0" exactly 50% of the time. In recovery boost mode, one of the devices is always negative biased condition. And also to connect the one of the inverter. The input of the inverter is to be "0 "and the output of the inverter is "1".With this we can find out the recovery boost mode condition. Due to the power and delay problem we go for Fine Grained Recovery Boosting. In this recovery boosting, we have to add two extra pMOS transistors which is connected to Vdd. And the output of the inverter is connected to ground of the SRAM cell i.e., Vdd. In Recovery Boosting technique that allows both pMOS devices in the memory cell to be put into the recovery mode by slightly modifying to the design of conventional SRAM cells. In this we have to found the circuit-level design of a physical register file and an issue queue that use such cells through SPICE-level simulation. After that we perform the architectural simulation.

V. FUNCTION OF FINE GRAINED RECOVERY BOOSTING

In this Fine Grained Recovery Boosting CR signal serves as the modified SRAM cell function. When a value of "0" is input to the CR line to transition the cell into the recovery boost mode, for raising the ground voltage, the two extra pMOS devices connected to the rail are also turned on. Therefore, by raising the ground and connecting the bitcell to , the cell can be transitioned into the recovery boost mode without affecting cells in other rows of the array.

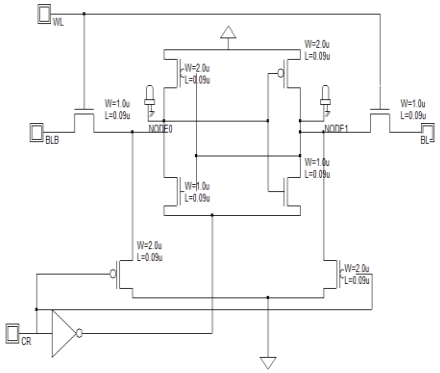

Fig.3. Modified 6T SRAM cell

5.1Power And Delay Calculation

If the extra pMOS devices resilient against NBTI by using high Vt- transistors. Although high-Vt devices are slower, these devices are used only when transitioning the cell into the recovery boost mode and not when transitioning to the normal operating mode. These devices do not affect the performance but may delay the transition into the recovery boost mode. Since these devices do not lie on the performance critical path, they are sized so as to minimize the overall area. However, the pMOS devices do consume leakage power. The power consumption of SRAM varies widely depending on how frequently it is accessed it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. The static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have a nearly negligible power consumption.

VI. SIMULATION RESULTS

6.1Operation Of Basic 6T SRAM write

Write operation performs the charging and discharging of the cell nodes. Here WL is the word line and BL is the bit line. WL is used to control the two access transistors. BL is used to transfer data for both read and write operation. It have two bit lines. Both the signal and its inverse are provided in order to increase the noise margin. In case of writing logic 1 to a 6T SRAM cell. We need to keep the bit line increase. Which in turn transfer to the cross coupled inverters and get stored there. Similarly logic 0 is stored to the 6T SRAM cell we need to keep the bit line increase. Which in turn transfer to the cross coupled inverters and get stored there.

6.2Modified 6T SRAM read Operation

In this modified 6T SRAM cell we have to add an extra inverter. In this inverter cr is the control signal. In normal SRAM cell input of the control signal is 1. But in the case of Recovery boosting we have to add the control signal as 0.So we get the output as 1.With this we can find out the read and write operation. In this Fine Grained Recovery boosting cr,wl,q and qbar are the inputs and the b and bbar is the outputs are the outputs. Here we have to add two extra pMOS transistors and an inverter. Here also we give the input of the control signal as 0.So we get the output as 1.In this also wl,cr,b and bbar are the inputs and the q and qbar are the output for the write operation.After that 4T sram array was constructed and comparing to 6T fine Grained Recovery Boosting and 4T Fine Grained Recovery Boosting.As a result we get as 4T Fine Grained Recovery Boosting is better. Because in 4T SRAM the delay is to be decreased.

6.3Waveforms

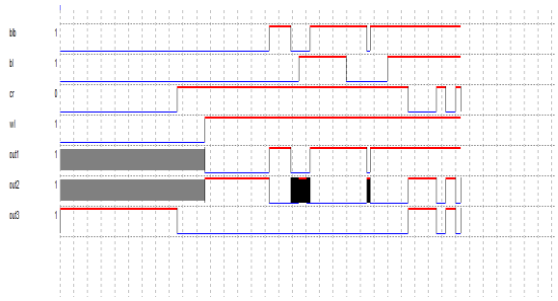

Fig 4.Wave Form for 6T SRAM Recovery Boosting

6.4TABLE

COMPARISON TABLE FOR SRAM CELL

SRAM CELL	POWER	AREA	DELAY
NORMAL SRAM	0.425um	Layout Width=64 um,Height =43um	56ps
RECOVERY BOOSTING SRAM	0.909um	Layout Width=65 um,Height =53um	36ps

VII. CONCLUTION

NBTI is one of the most important silicon reliability problems facing processor designers. SRAM memory cells are especially vulnerable to NBTI since the input to one of the pMOS devices in the cell is always at logic "0." In this paper, we propose recovery boosting, this technique that allows both pMOS devices in the cell to be put into the recovery mode by raising the ground voltage and the bitline to Vdd. First we go for designing a basic 6T SRAM array. In this we find out the read and write operation. Next we design the Modified Recovery boosting. In this case the power and delay gets increased. In order to overcome this problem we go for Fine grained Recovery boosting. After that 6T array is designed and also design a4T SRAM and its Recovery Boosting. By using this, the power and delay gets decreased.In my future work To design a MAC unit by replacing the register with Fine Grain SRAM memory system.

VIII. ACKNOWLEDGEMENT

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Biography

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