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UPQC Controlled Capable Of Mitigating Unbalance In Source Voltage And Load Current

B. Santhosh Kumar[1] K. Vijay Kumar[2]
[1]PG Research Student Dadi Institute Of Engineering And Technoogy,Anakapalli Visakhapatnam
[2]PROFESSOR Dadi Institute Of Engineering And Technoogy, Anakapalli Visakhapatnam

Abstract
This paper reports the development of a laboratory prototype of a fully digital DSP-controlled 12-kVA unified power quality conditioner (UPQC), capable of compensating for both the supply voltage and the load current imperfections. A fully digital controller based on the TMS320F2812 DSP platform is implemented for the reference generation as well as control purposes. The delay problem in the digital controller is overcome by application of a fast DSP, a compact control technique and proper flow of control steps in the DSP software. A phase-locked loop- less software grid synchronization method has been implemented for the effective operation of the UPQC under conditions of grid frequency variation. A sequence-based compensation strategy has been developed to compensate for balanced and unbalanced sags while accommodating the fact that the voltage injection capability of the UPQC is limited. The prototype UPQC power circuit, control features, and control algorithm along with experimental results are presented in this paper.

Index Terms—Current unbalance and nonlinear load, DSP- based control, power quality conditioning (PQC), unbalanced volt- age sag, unified power quality conditioner (UPQC).

I. INTRODUCTION

The Proliferation of power electronics-based equipment has produced a significant impact on the quality of electric power supply. Nowadays, much of the equipment is based on power electronic devices, often leading to problems of power quality (PQ) [1]. At the same time, this equipment is typically equipped with microprocessor-based controllers, which are quite sensitive to deviations from the ideal sinusoidal line voltage. In such conditions, both electric utilities and end users of electric power are increasingly concerned about the quality of electric power. Conventional PQ mitigation equipment is proving to be inadequate for an increasing number of applications, and this fact has attracted the attention of power engineers to develop dynamic and adjustable solutions to power quality problems. Thus, between the different technical options avail- able to improve PQ, active power filters (APFs) have proved to be an important alternative to minimize the financial impacts of PQ problems [2], [20]–[26]. One modern and very promising solution is the unified power quality conditioner (UPQC)—a power conditioning device that consists of two APFs connected back-to-back on the dc side and deals with both load current and supply voltage imperfections [3], [4]. Although the APFs have higher cost and complex control, they are much superior in filtering performance than the passive filters. Therefore, APFs are preferred over passive filters as the solution to various PQ problems arising from the load or the supply side. Few obvious reasons for this are [2], [20] described in the following.

1. Design of the active filters is almost independent of power system parameters.
2. No lengthy tuning effort is required in the design of active filters, which is usual in the case of passive filters.
3. Possibility of resonance is excluded in the active filter application

In [4] and [5], various configurations of APFs are reported. The application of DSP in control of APFs is reported in [6]–[11]. The reference generation and tracking are two identified tasks under any type of control. In [6], DSP is applied to generate the reference source current based on measurement of the source voltage and dc-link voltage. A fully digital controller is implemented in [7]. An attempt has been made to damp the propagation of voltage harmonics in the distribution line. It applies a synchronous rotating frame technique to generate the compensator reference current, and hence, the compensator voltage. Sine pulse width modulation (PWM) technique is used to generate the switching for the voltage source inverter (VSI). In [8], the source current reference is generated as an in-phase component of the fundamental positive sequence component of the source voltage, calculated by applying synchronous reference frame transformations. However, in order to avoid the inherent delay introduced by a digital current controller, an analog hysteresis controller is applied to generate switching pulses based on source current reference and measured source current. In [9], four different control techniques of a shunt active power filter are compared at a lower switching frequency of the voltage source converter. In

[10], a controller based on a Lagrange multiplier optimization technique to generate the compensator reference current in DSP has been developed. An external hysteresis current controller is implemented to track the compensator reference current. In [11], selective harmonic compensation is implemented to generate the compensator reference current. The delay in the measurement and control action, aliasing effect in digitized voltage and current signals due to switching noise are major concerns in any DSP-based controller. Synchronous sampling and calculation methods are suggested in [7] to eliminate these effects. Additionally, a fast DSP with an A–D converter (ADC) of high conversion rate should be chosen for fast control action. Source current reference generation and control instead of the compensator current is suggested in [8] to avoid the spikes in the source current, when sharp changes occur in nonlinear load current.

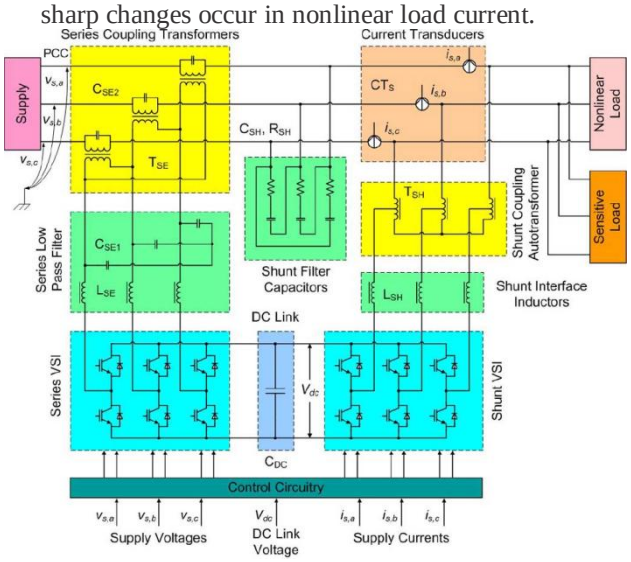

Fig. 1. Power circuit of the prototype UPQC.

But delay in the control decision and switching can also cause the source current to go out of bands in the case of hysteresis current control. This remains a problem even if direct source current control is used, but a fast DSP and a com- pact control technique is not chosen. Fully digital DSP-based series and shunt active power filters have been presented in [12] and [13], respectively.

This paper presents the development of a laboratory prototype of a fully digital DSP-based 12-kVA UPQC, as shown in Fig. 1. A compact digital controller to compensate for both load current imperfections (harmonics, reactive power and unbalance) and supply voltage disturbances (sags, unbalance) is implemented with a ezDSP F2812 development kit (TMS320F2812 32-bit fixed point processor). The controller performs well, both under balance and unbalance supply conditions. A simple soft- ware zero-crossing detection-based line frequency synchroning method has been applied in the control of UPQC. There- fore, a phase-locked loop (PLL)-less control has been achieved, which saves the processor time and does not involve additional hardware. Also, a sequence-based compensation strategy has been developed to compensate for balanced and unbalanced sags considering that the voltage injection capability of the UPQC is limited.

II. POWER CIRCUIT

The UPQC is a combination of series and parallel APFs connected back-to-back to a common dc energy storage capacitor [4]. The power circuit layout of the prototype UPQC is shown in Fig. 1. The prototype UPQC is intended to be used in three-phase three-wire systems. The ratings of the prototype UPQC are: 133 (line–neutral)/230 V (line–line) and 17.4 A for the shunt compensator, and 115 V and 34.8 A for the series compensator.

The shunt active filter is responsible for power factor correction and compensation of load current harmonics and unbalances. Also, it maintains constant average voltage across the dc storage capacitor C_{dc} . The shunt part of the UPQC consists of a VSI connected to the common dc storage capacitor C_{dc} on the dc side and on the ac side it is connected in parallel with the load through the shunt interface inductors L_{SH} and a star-connected three-phase shunt coupling auto-transformer T_{SH} . The shunt interface inductors L_{SH} , together with the shunt filter capacitors C_{SH} are used to filter out the switching frequency harmonics produced by the shunt VSI. T_{SH} is used for matching the net- work and VSI voltages.

The series active filter is responsible for voltage compensation during supply side disturbances, such as voltage sag and unbalance. The series part of the UPQC also consists of a VSI connected on the dc side to the same energy storage capacitor C_{dc} , and on the ac side it is connected in series with the feeder, through the series low-pass filter (LPF) and three individual single-phase series coupling transformers T_{SE} . The series LPF prevents the switching frequency harmonics produced by the series VSI entering the distribution system. T_{SE} provide voltage matching and isolation between the distribution network and the series VSI.

The series and shunt inverters are standard six-switch VSIs based on *TOSHIBA MG150J2YS50* IGBT devices (150 A, 600 V). Across the dc link, a 2200 μF, 500 V electrolytic capacitor is connected (C_{dc}). The initial values of the dc-link capacitor ratings have been estimated based on the recommendations presented in [1, p. 1084 and pp. 1087–1088], [14], [16], [17], and [18, Section 25.2.3.3]. Then, these values have been refined through simulations and experimentally validated. The selection of the shunt coupling inductors, and series LPF has been performed in the same way. The parameters of the series and shunt coupling transformers are given in Table I.

In order to remove the triplen harmonics in the voltages injected by the series transformers T_{SE} , caused by the transformer core nonlinearity, the

secondary windings of the series trans- formers are connected in delta. Also, the delta connection of the inverter-side windings maximizes the utilization of the dc-link voltage.

The filter inductors of both shunt and series compensators (L_{SH} and L_{SE}, respectively) have the following parameters: $L = 1.245$ mH and $R = 0.1$ Ω.

The filter capacitors $C_{SE\,1}$ connected in star on the secondary side of the series transformers are of 10 μF, and those connected across the primary of the series transformer $C_{SE\,2}$ are of 300 μF.

TABLE I
TRANSFORMERS PARAMETERS

Parameters	Series transf.	Shunt auto-transf.
Number of phases	1-phase	3-phase
Power, kVA	4	12
Voltages (primary/secondary), V	115/130	230/130
Core Resistance, Ω	363.7	1547.3
Core inductance, mH	945	10441
Winding resistance, Ω	0.1322	0.1588
Winding leakage inductance, mH	0.42	0.1684

of the series transformer to cancel out the low-frequency harmonics, which appear in the injected voltage, mostly due to the blanking time during commutation of the series inverter switches.

The filter capacitors of the shunt compensator C_{SH} are of 20 μF and they are connected in delta. A 4 Ω damping resistor R_{SH} is connected in series with each shunt filter capacitor C_{SH}

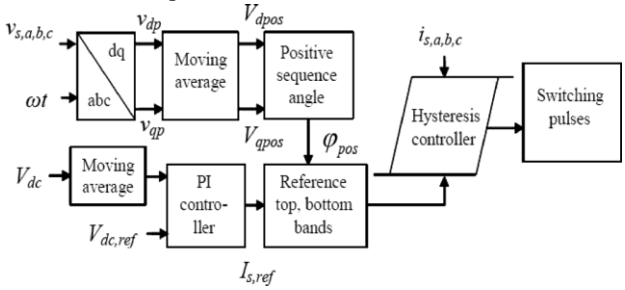

Fig. 2. Control block of the shunt APF.

This resistor plus proper choice of the shunt inverter switching frequency (hysteresis band) help to avoid resonance at switching frequencies.

III. CONTROL SCHEME OF THE UPQC

The DSP implementation of the UPQC control is explained in detail in this section. The choice of DSP kit is very suitable for UPQC control as it contains 16 12-bit ADC channels, 56 general purpose digital ports of which 12 can also act as inbuilt PWM channels, ample on-chip memory as well as external memory, and processing speed of 150 MHz. The parameters of the developed laboratory prototype of the UPQC, control details, and experimental results are presented in the following parts of the paper.

A. Control of Shunt Active Power Filter

The shunt active power filter is controlled as a current- controlled VSI. The measured source current is controlled to remain within the reference band generated with the help of a hysteresis current controller. The control objective can be explained with the block diagram shown in Fig. 2. When the UPQC supplies a nonlinear/inductive load, the objective of the shunt converter is to compensate for the load current harmonics, reactive power and unbalance, such that the supply currents are balanced sinusoids (i.e., the distortion is within the limits prescribed by standards) in-phase with the voltages at the point of common coupling (PCC). PCC is the point, where the UPQC is connected to the grid, as shown in Fig. 1. The shunt APF current is controlled indirectly by con- trolling the source current to be sinusoidal and in-phase with the fundamental positive sequence component of the source voltage. Thus, the system tracks the source current instead of tracking the shunt APF current. Combined with a hysteresis current controller, this control technique involves only the source current measurement. The fundamental positive sequence in-phase and quadrature components of the source voltage and the phase angle are calculated with (1)–(4)

$$\begin{bmatrix} v_{\mathrm{dp}} \\ v_{\mathrm{qp}} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \end{bmatrix} \times \begin{bmatrix} v_{s,a} \\ v_{s,b} \\ v_{s,c} \end{bmatrix} \quad (1)$$

$$V_{\mathrm{dpos}} = \frac{1}{T} \int_{t-T}^{T} v_{\mathrm{dp}}\, dt \quad (2a)$$

$$V_{\mathrm{qpos}} = \frac{1}{T} \int_{t-T}^{T} v_{\mathrm{qp}}\, dt \quad (2b)$$

$$\varphi_{\mathrm{pos}} = \tan^{-1}\left(\frac{V_{\mathrm{qpos}}}{V_{\mathrm{dpos}}}\right) \quad (3)$$

$$\varphi_{\mathrm{pos}} = \tan^{-1}\left(\frac{V_{\mathrm{qpos}}}{V_{\mathrm{dpos}}}\right) + \pi, \quad \text{if } V_{\mathrm{dpos}} < 0 \text{ and } V_{\mathrm{qpos}} < 0. \quad (4)$$

The phase angle ϕ_{pos} obtained with (1)–(4) is used for calculating the sine template, which is in-phase with the fundamental positive sequence component of the source voltage. The voltage across the dc-link capacitor C_{dc} is maintained at the reference value 350 V. The dc voltage regulation is achieved by using a proportional and integral (PI) controller. The parameters of the PI controller are: $K_P = 0.2$ A/V and $K_I = 2.8$ A/(V · rad). First, these were calculated applying the Ziegler–Nichols tuning rules [19], and then refined through simulations and experimentally validated. The voltage measured across the dc-link

capacitor C_{dc} is compared with the reference value and the voltage error is processed by the PI controller (see Fig. 2). Any variation in the dc-link capacitor voltage is a direct measure of the change in real power requirement of the load. Therefore, the output of the PI controller applied to maintain the dc-link voltage constant is the magnitude of the reference source current, as implemented in [6] and [14]. The current magnitude is multiplied by the sine template to generate the source reference current. A hysteresis band is constructed by adding and subtracting appropriate offset values to the reference. The measured source current is continuously compared against the hysteresis top and bottom bands to generate the switching pulses. More details on the hysteresis controller can be found in [4].

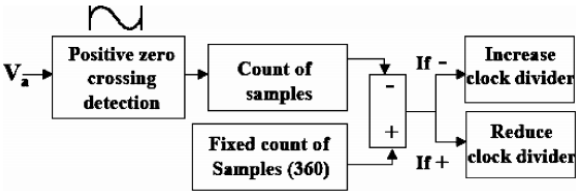

Fig. 3. Frequency locking control block.

The compactness of the control and flexibility to work under all load current and source voltage circumstances makes it a very attractive choice to implement in a DSP. The current transducers CT_S for measuring the source currents are installed between the points of connection of the shunt coupling autotransformer T_{SH} and shunt filter capacitors C_{SH}, as shown in Fig. 1. Such a connection arrangement is dictated by the use of the hysteresis current controller. If the current transducers CT_S were installed to the left of the point of connection of the shunt filter capacitors C_{SH}, the implementation of the hysteresis control strategy would be unsuccessful[15].
The control software is developed in C programming lan- guage using code composer studio environment and loaded into DSP. The interrupt service routine (ISR), where switching decisions are made, is operated at around 18 kHz. A frequency- locking algorithm is implemented as shown in Fig. 3.

The program is started with a 50-Hz approximation of the source frequency. For this purpose, the supply voltage is measured and passed through a scaling and filter circuit for proper ADC interface and to eliminate the high frequency noise. The zero crossing of the "A" phase source voltage at negative to positive half-cycle transition is detected with a simple thresh- old comparison method. A noisy zero crossing is a potential threat for this method of synchronization. To avoid detection of multiple zero crossing, any successive zero crossing detected is discarded for next 30 samples after the first one is detected. The number of samples for one power cycle is counted. This is compared with a fixed number of samples every time the zero crossing is detected (360 samples in this paper, consider- ing 18 kHz as the sampling frequency). If the grid frequency is higher than 50 Hz, a positive difference is calculated. Therefore, the speed of the clock synchronized with the ISR and ADC sampling should be increased to synchronize with the grid frequency. Therefore, the clock dividing register value is reduced to increase ISR and ADC sampling frequency. The clock divider is updated in the other way, if the grid frequency falls below 50 Hz.
The clock divider is adjusted gradually in several steps (considering a slow variation of the supply frequency), such that the difference between the sample count and the fixed count reduces to zero. Therefore, the ISR and ADC sampling frequency will be around 18 kHz to take into consideration the supply frequency variations. The register associated with the ISR timer is shad- owed in F2812 DSP, which means the register can be updated anywhere in the ISR and can be made effective with different events of the timer (period match and overflow/underflow of counter register). Faulty frequency variation detection is avoided by gradually adjusting the clock divider and by setting upper and lower limits of frequency variation. The details are also provided in [13].

The ADC sampling remains synchronized with the supply frequency, since supply frequency is tracked continuously. The inherent delay caused by the ADC sensing and calculations in the digital hysteresis controller is of great concern, when these types of current controllers are designed. To avoid the delay in switching decisions, the measured source current is compared with the reference value of the current calculated in the previous ISR time. This avoids the delay in switching that can be caused by the calculation time (about 30 μs). The switching decision is
sent to six inbuilt general-purpose I/O ports.

B. Control of the Series Active Power Filter

The series active power filter is controlled as a voltage- controlled VSI. It maintains the load voltage at a predetermined level during source voltage abnormal conditions, such as volt- age sag and unbalance. The series APF of the prototype UPQC has restricted voltage injection capability (injection limited to 50% of the supply voltage). The upper limit of injection in any voltage-conditioning device is determined by the rating of the inverter and associated injection transformer. The rating of the inverter and transformer are determined by the requirement to keep the cost of the equipment low. Therefore, it is necessary to take the rating factor of the device into consideration while designing the controller in order to perform optimally with the available rating of the device. A sequence analysis-based compensation strategy has been developed to compensate balanced and/or unbalanced incoming voltage to regulate the load voltage. The advantage of the scheme is that under most of the practical cases of unbalance, the series APF controller is able to fully compensate the unbalance, provided the voltage rating of the series APF is higher than the negative sequence voltage magnitude. This sequence analysis-based control strategy is

implemented with a control-optimized fixed-point TI DSP (TMS320F2812) mentioned earlier. A feed-forward control loop measures the source voltage continuously, and it is compared with the reference voltage to be maintained at the load. The voltage to be injected is calculated and the appropriate switching signals are sent to the insulated gate bipolar transistor (IGBT) switches. The inbuilt PWM ports of the DSP provide switching pulses at 18 kHz frequency. The control block is given in Fig. 4.

Three phase voltages are sensed and converted to positive and negative sequence in-phase and quadrature components as shown in (1) and (5).

$$\begin{bmatrix} v_{\mathrm{dn}} \\ v_{\mathrm{qn}} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t + 2\pi/3) & \sin(\omega t - 2\pi/3) \\ \cos(\omega t) & \cos(\omega t + 2\pi/3) & \cos(\omega t - 2\pi/3) \end{bmatrix} \times \begin{bmatrix} v_{s,a} \\ v_{s,b} \\ v_{s,c} \end{bmatrix} \quad (5)$$

Then, the fundamental positive and negative sequence components [which are transformed to dc in (1) and (5)] are extracted with the help of a moving average filter (acts as a low-pass filter).

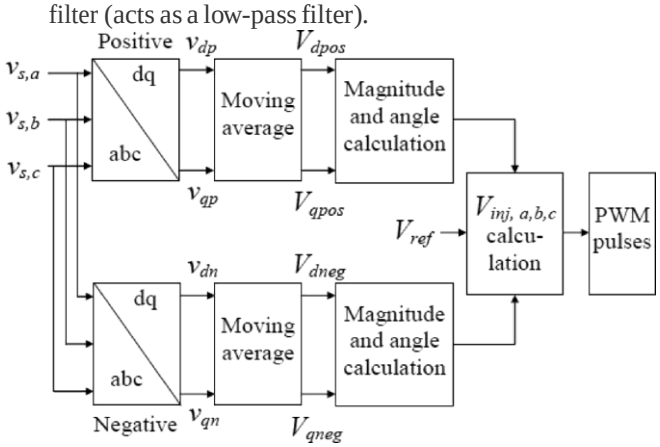

Fig. 4. Control block of series APF.

over a period of one power frequency cycle as shown in (2a), (6a), (2b), and (6b).

$$V_{\mathrm{dneg}} = \frac{1}{T} \int_{t-T}^{t} v_{\mathrm{dn}}\, dt \quad (6a)$$

$$V_{\mathrm{qneg}} = \frac{1}{T} \int_{t-T}^{T} v_{\mathrm{qn}}\, dt. \quad (6b)$$

The magnitude and phase angle of the positive and negative sequence components are calculated with (7a) and (7b), and (3) and (8), respectively. When determining ϕ_{pos}, if both V_{qpos} and V_{dpos} are negative values, π should be added to the value obtained with (3). The same rule applies for determining ϕ_{neg}. If both V_{qneg} and V_{dneg} are negative values, π should be added to the value obtained with (8).

$$V_{\mathrm{pos}} = \sqrt{V_{\mathrm{dpos}}^2 + V_{\mathrm{qpos}}^2} \quad (7a)$$

$$V_{\mathrm{neg}} = \sqrt{V_{\mathrm{dneg}}^2 + V_{\mathrm{qneg}}^2} \quad (7b)$$

$$\varphi_{\mathrm{neg}} = \tan^{-1}\left(\frac{V_{\mathrm{qneg}}}{V_{\mathrm{dneg}}}\right). \quad (8)$$

The series APF control aims to maintain the positive sequence component at a predetermined value, and to reduce the negative sequence and zero-sequence components to zero. In a three- phase three-wire system (which is the case in this paper) the zero-sequence component is zero. Therefore, the voltage to be injected in a particular phase is the vector difference of the reference load voltage $V_{\mathrm{ref},k}$, and positive $V_{\mathrm{pos},k}$ and negative $V_{\mathrm{neg},k}$ sequences of the supply voltage, as shown in (9). The reference load voltage $V_{\mathrm{ref},k}$ is in-phase with the positive sequence of the supply voltage $V_{\mathrm{pos},k}$. Therefore, in (9), their magnitudes are subtracted from each other.

$$\vec{V}_{\mathrm{inj},k} = V_{\mathrm{inj},k}\angle\varphi_{\mathrm{inj},k} = \vec{V}_{\mathrm{ref},k} - \vec{V}_{\mathrm{pos},k} - \vec{V}_{\mathrm{neg},k} = (V_{\mathrm{ref}} - V_{\mathrm{pos}})\angle(\varphi_{\mathrm{pos}} + \alpha_k) - V_{\mathrm{neg}}\angle(\varphi_{\mathrm{neg}} - \alpha_k) \quad (9)$$

Where k = a,b,c, $\alpha_a = 0$, $\alpha_b = -2\pi/3$, $\alpha_c = 2\pi/3$, and The injected voltage $V_{\mathrm{inj},k}$ is added to the source voltage to regulate the load voltage at the desired level. The voltage that can be injected by the series APF in order to establish a balanced three-phase system on the load side is determined by the rating of its inverter. If the desired magnitude $V_{\mathrm{inj},k}$ of the injected voltage $V_{\mathrm{inj},k}$ calculated with (9) is beyond the capacity of the series APF, it has to be limited to the maximum voltage capacity $V_{\mathrm{inj,max}}$ of the series APF.

The injected voltage $V_{\mathrm{inj},k}$ for each phase is calculated with (9). Then, the phase that requires maximum injection is selected, i.e., the phase having the greatest injected voltage magnitude. Let us mark that phase with m (if for example phase c has the greatest injected voltage magnitude, then $m = c$). The magnitude of the injected voltage for that phase $V_{\mathrm{inj},m}$ is compared with the maximum possible value $V_{\mathrm{inj,max}}$. The following three cases are identified:

Case 1: $V_{\mathrm{inj},m} \leq V_{\mathrm{inj,max}}$. The magnitude of the injected voltages $V_{\mathrm{inj},k}$ calculated with (9) is within the capacity of the series APF and no further calculation is required. Thus, the series APF injects the voltages calculated with (9). The resulting load voltages are fully balanced and their magnitudes are equal to the reference load voltage V_{ref}.

Case 2: $V_{\mathrm{inj},m} > V_{\mathrm{inj,max}}$ and $V_{\mathrm{neg}} \leq V_{\mathrm{inj,max}}$

In order to ensure the absolute balancing of the load voltages, the negative sequence component has to be fully compensated, which is possible in this case. Thus, the injected voltage will contain the negative sequence component ($-V_{neg,k}$ $(\phi_{neg} - \alpha_k)$). Also, it will contain the positive sequence component, but its magnitude (V $- V_{pos}$) will be lower than the desired one ($V_{ref} - V_{pos}$), in order to keep the injected voltage magnitude $v_{inj,max}$. This means that the reference load voltage has to be appro- priately reduced from the desired value V_{ref} to a lower value v'_{ref}. such that $v_{iinj,m} = v_{iinj,max}$.. Thus has to be written for phase m (phase which requires maximum injection) as shown in (10).

$$\vec{V}_{inj,m} = V_{inj,max}\angle\varphi_{inj,m} = (V'_{ref} - V_{pos})\angle(\varphi_{pos} + \alpha_m) - V_{neg}\angle(\varphi_{neg} - \alpha_m). \quad (10)$$

The new reference load voltage v'_{ref} is calculated as follows. First, (10) is multiplied by 1 ($-\phi_{pos} - \alpha_m$); then, the negative sequence component is presented in rectangular form. The result of these transformations is (11) from which (12) is derived. Taking into account that $2\alpha_m = -\alpha_m$, appropriate substitution is made in (11) in order to avoid spending the valuable processor time on performing unnecessary mathematical operations

$$\begin{aligned} &V_{inj,max}\angle(\varphi_{inj,m} - \varphi_{pos} - \alpha_m) \\ &= V'_{ref} - V_{pos} - V_{neg}\angle(\varphi_{neg} - \varphi_{pos} - 2\alpha_m) \\ &= V'_{ref} - V_{pos} - V_{neg}\angle(\varphi_{neg} - \varphi_{pos} + \alpha_m) \\ &= V'_{ref} - V_{pos} - V_{neg}\cos(\varphi_{neg} - \varphi_{pos} + \alpha_m) \\ &\quad - jV_{neg}\sin(\varphi_{neg} - \varphi_{pos} + \alpha_m) \end{aligned} \quad (11)$$

$$V^2_{inj,max} = [V'_{ref} - V_{pos} - V_{neg}\cos(\varphi_{neg} - \varphi_{pos} + \alpha_m)]^2 + V^2_{neg}\sin^2(\varphi_{neg} - \varphi_{pos} + \alpha_m). \quad (12)$$

$$V'_{ref} = V_{pos} + V_{neg}\cos(\varphi_{neg} - \varphi_{pos} + \alpha_m) + \sqrt{V^2_{inj,max} - V^2_{neg}\sin^2(\varphi_{neg} - \varphi_{pos} + \alpha_m)}. \quad (13)$$

Solving (12) for v'_{ref} the new reference load voltage v'_{ref} is obtained as shown in (13).

The injected $_{ref}$voltages have to be recalculated using (9) in which V_{ref} is substituted by V Thus, the injected voltage is restricted to a combination of negative sequence component and reduced positive sequence component in all phases in order to stay within the limit of the series APF. The resulting load voltages are fully balanced, but their magnitudes are less than the desired value (reference load voltage V_{ref}).

Case 3: $V_{inj,m} > V_{inj,max}$ and $V_{neg} > V_{inj,max}$. In this case, in order to balance the load voltage as much as possible, the maximum possible negative sequence voltage is injected, i.e., the injected voltages are recalculated to be $V_{inj,k} = -V_{inj,max}$ $(\phi_{neg} - \alpha_k)$. This is the case when the absolute balancing of the load voltages cannot be achieved. Thus, in this worst case, the resulting load voltages are not fully balanced and their magnitudes are less than the desired value (reference load voltage V_{ref})

C. Control of the Integrated UPQC

Fig. 5 shows the integrated flowchart for the full digital control and operation of the UPQC that is implemented through the DSP. From the flowchart it can be seen that the algorithm is integrated with digital protection of dc-link overvoltage, and offsets the measurement errors of the ADCs.

IV. EXPERIMENTAL RESULTS

A. Steady-State results

The prototype UPQC presented in Section II and Section III is implemented and the following experimental results have been obtained. The nominal supply voltage of the experimental setup is 230 Vrms line-to-line. An ac power source of type 4500Ls produced by California Instruments has been used throughout the experiment.

Three loads are connected to the UPQC: resistive, inductive, and nonlinear (resistor connected to a three-phase diode bridge rectifier). The total currents drawn by these three loads are shown in Fig. 6(a), where total harmonic distortion (THD) per phase is 15.8%.

In Fig. 6(b) the supply currents are shown. These are balanced sinusoids containing some admissible ripple (THD = 4.45%, whereas the limit recommended by IEEE Standard 519–1992 is8%).

A 40% supply voltage sag has been created. The supply volt- ages are shown in Fig. 7(a). Due to series injection, the load wit- nesses the voltages presented in Fig. 7(b), which are balanced sinusoids with the magnitude equal to 188 V peak per phase

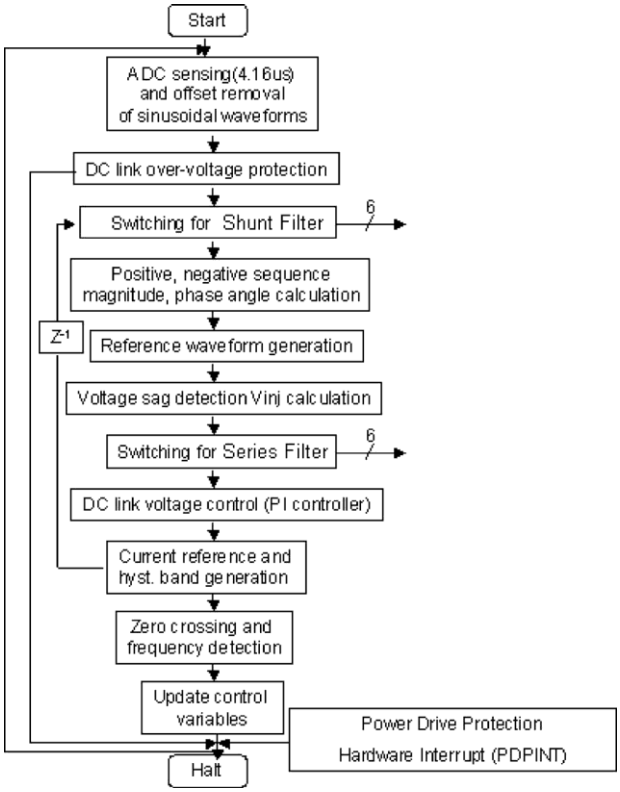

Fig. 5. Complete flowchart of UPQC control.

(corresponds to 230 Vrms line–line), as desired. The THDs of both the supply (2.3%) and the load (1.5%) voltages are below the 5% limit, recommended by IEEE Standard 519–1992.

It can be seen in Fig. 7(c) that the supply voltage and current are in-phase, which means that no reactive power is drawn from the supply. The supply, injected, and load voltages are all in- phase, as shown in Fig. 7(d).

B. Dynamic Condition Results

In the steady state, the shunt compensator maintains the dc- link voltage constant at 350 V. The dc-link voltage dynamics after connection of the nonlinear load is shown in Fig. 8(a). The dc-link voltage drops down by about 50 V, when the nonlinear load is switched ON. In this case, the dc-link capacitor has to supply the real power to the load until a new supply current reference suitable for new load condition is calculated.

Fig. 8(b) shows another dynamic condition for the dc-link voltage at the occurrence of supply voltage sag (a 40% sag has been created). The sag occurrence results in a sudden increase of the supply current. Before a new supply current reference is determined, the dc-link capacitor is supplying real power to the load causing the dc-link voltage drop (about 50 V). The dc-link voltage is stabilized soon after the controller sets the new supply current reference.

A load unbalance has been created while having normal sup- ply voltages. The load currents are both distorted and unbalanced [see Fig. 9(a)]. However, due to the action of the shunt compensator, the source currents [see Fig. 9(b)] are balanced sinusoids (containing some acceptable ripple, THD = 4.5%).

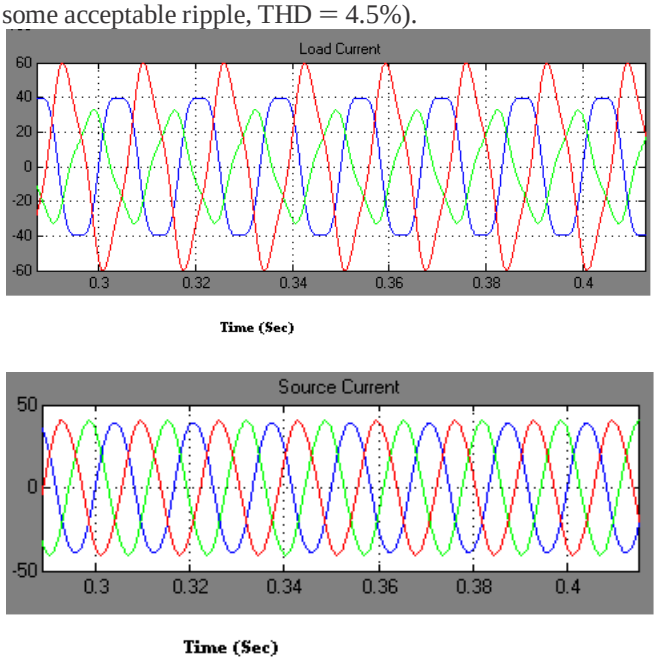

Fig. 6. Load currents and supply currents. (a) Load currents (THD = 15.8%). (b) Supply currents (THD = 4.45%)

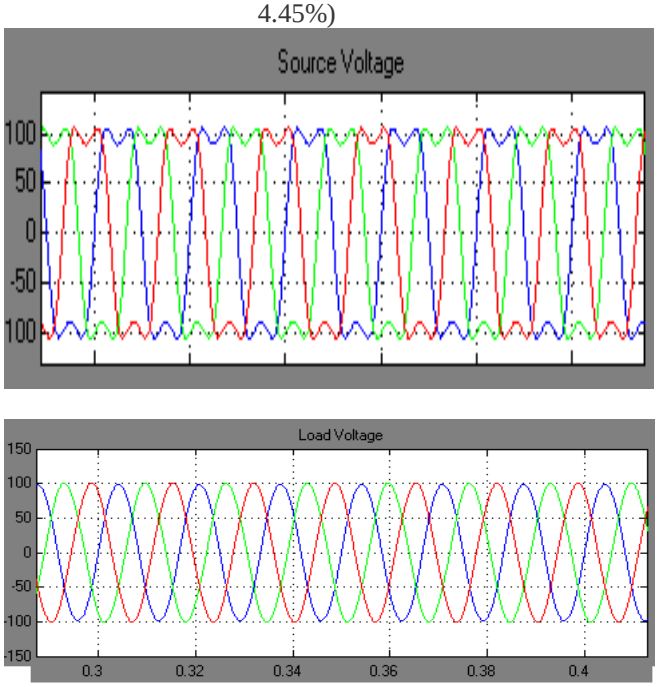

Fig. 7. Voltages at various points. (a) Supply voltages (THD = 2.3%). (b) Load voltages (THD = 1.5%).

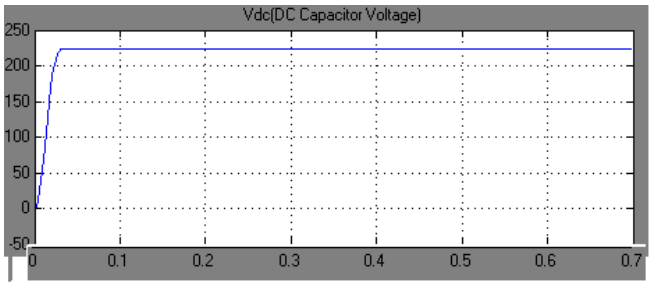

Fig. 8. Dynamic performance of the dc link voltage

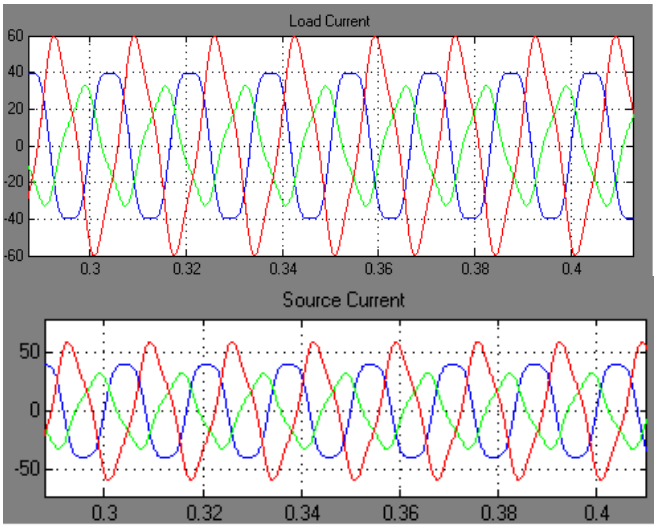

Fig. 9. Load unbalance. (a) Load currents. (b) Supply currents(THD = 4.5%).

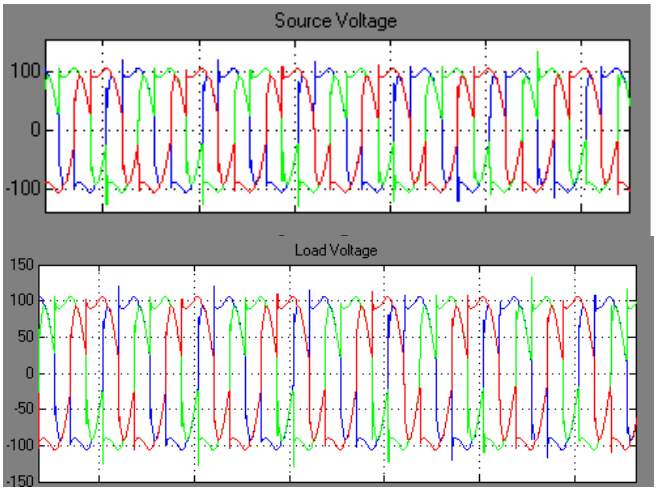

Fig. 10. Supply voltage unbalance. (a) Supply voltages (THD = 2.3%). (b) Load voltages (THD = 1.7%).

Also, an unbalanced supply voltage sag has been created as shown in Fig. 10(a), where the supply voltages are unbalanced sinusoids with the magnitudes below the nominal level. Due to appropriate series injection, the load voltages [see Fig. 10(b)] are balanced sinusoids (THD = 1.7%) with magnitudes equal to 188 V peak per phase (corresponding to 230 Vrms, line–line) as specified in the design.

V. CONCLUSION

A fully digital controller for a UPQC has been implemented with a DSP. A PLL-less grid synchronization method applicable in a digital controller of the UPQC has been implemented. The delay problem in digital controller has been overcome by the application of a fast DSP, a compact control technique, and proper flow of control steps in the DSP software. A sequence component-based controller has been developed for the series APF, which is simple and elegant to implement with a DSP. The proposed control scheme takes into consideration the injected voltage limitation of the series APF and ensures the unbalance compensation under different unbalance conditions. The advantage of the mitigation scheme is that under most of the practical cases of unbalance, the series APF controller is able to fully compensate the unbalance, provided the voltage rating of the series APF is higher than the negative sequence voltage magnitude. Based on experimental results presented earlier, it can be concluded that the performance of the DSP-based controller proved to be very satisfactory for the steady-state as well as dynamic conditions for the UPQC.

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