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Design and Implementation of CMOS VLSI Digital Circuits Using Self-Adjustable Voltage Level Technique

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ABSTRACT
In present scenario, an increasing demand for mobile electronic devices such as cellular phones, laptop computers and personal digital assistants requires the use of power efficient circuits. To minimize the power dissipation and to increase the battery lifetime, the supply voltage, V_{DD} has been scaled down continuously. So, scaling down the supply voltage, without scaling down the threshold voltage increases the propagation delay. However the threshold voltage scaling results in substantial increases of sub-threshold leakage current, which increases the leakage or static power dissipation of the circuits. Therefore, the main aim of this work is to minimize the power dissipation by reducing leakage power. In this work, some of the combinational and sequential circuits are designed with CMOS transistors using self-Adjustable Voltage Level (SAL) technique to optimize the power dissipation. The circuits are implemented using the Mentor Graphics Backend Tool to analyze the power dissipation. With this SAL technique less than 50% of the power dissipation can be reduced for designed circuits which lead to improve performance of the circuits.

Keywords- Pass Transistors, Transmission Gate, Gate Diffusion Input, Power Dissipation, Self Adjustable Voltage Level circuit.

I. Introduction

As day by day rapid growth in semiconductor device industry has led to the development of portable systems with high performance and enhanced reliability [1]. In such portable applications, power management has become a major issue due to the limited battery life time [2]. Consequently, at the same time power dissipation is also becoming a major issue for VLSI circuit design. In today's high performance processors leakage power makes up to 50% of the total power consumption [3]. Therefore reduction of the leakage power becomes a vital role in low power design. Leakage power dissipation means that power dissipated by the circuit when it is in sleep or standby mode.

The leakage power (P_{leak}) and the propagation delay (Tpd) of a circuit are given by [4] [5].

$$p_{leak} = I_{leak} * V_{DD} \qquad (1)$$

$$T_{Pd} \alpha \, V_{DD} / (V_{DD} - V_{th})^2 \qquad (2)$$

Where I_{leak} is the leakage current that flows in a transistor when it is in off state, V_{DD} is the supply voltage, V_{th} is the threshold voltage of the transistor. The leakage power dominates the dynamic power especially in deep submicron circuits. At the same time, technology scaling also leads to increase in leakage power and sub threshold leakage power. In general, the leakage current consists of different components, such as sub-threshold, gate, reverse-biased junction, gate-induced drain leakage [6]. Among all these leakages, sub threshold leakage and gate-leakage are dominant. In this work, some of the digital circuits such as 4×1 Multiplexer, 8×3 Encoder, BCD Counter and Mealy Machine were designed and implemented by using Pass Transistors (PT), Transmission Gate (TG) and Gate Diffusion Input (GDI) techniques. Further, these circuits are designed using Self Adjustable Voltage Level (SAL) technique to minimize leakage power. The paper is organized as follows: section 1 gives about different CMOS techniques for the implementation of a digital circuit. In section 2 implementation of digital circuits using GDI technique is given. Section 3 describes about self-adjustable voltage level technique that are applied to the above designs. Section 4 presents the results of the designed circuits with and without SAL techniques and section 5 gives the conclusion.

II. Different CMOS implementation techniques

There are different techniques such as Pass Transistors (PT), Transmission Gate (TG) and Gate Diffusion Input (GDI) are existed in literature to design various digital circuits. Pass transistor

design have small nodal capacitance which results in high speed. To realize any function logically, PT design uses less number of transistors so that there is low power dissipation. Reduced number of transistors occupies small area which leads to low interconnection effect [7-10]. There are two main disadvantages with this PT design, one is the threshold voltage across the single channel pass transistors results in reduced drive and hence slow operation which increase delay. Other one is, since the high input voltage level is not V_{DD} the PMOS device in inverter is not fully turned off. Where as, Transmission gate design is another method used to realize complex logic functions it uses less number of transistors as compared to normal CMOS logic. It solves the problem of output logic swing by using PMOS as well as NMOS used as pass transistor. There are some drawbacks with this technique which requires more area than NMOS pass circuitry and requires complemented control signals. The next technique is Gate Diffusion Input (GDI), here one of the inputs are directly diffused into the gates of the transistors of N-type and P-type devices so it is called as gate diffused input technique. GDI technique reduces power dissipation, propagation delay, and area of digital circuits [11-14]. This method is based on the simple cell. A basic GDI cell contains four terminals they are G (common gate input of NMOS and PMOS transistors), P (the outer diffusion node of MOS transistor), N (the outer diffusion node of NMOS transistor), and D (common diffusion node of both transistors). The basic GDI cell is shown in fig. 1. The different logic functions implemented with GDI cell is given in table1.

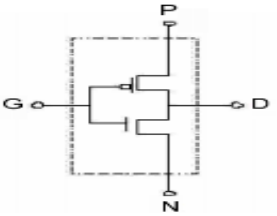

Fig. 1: Basic GDI cell

Table 1. Logic function implemented with GDI cell

N	P	G	D	Function
0	B	A	A*B	F1
B	1	A	A+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	AB+AC	MUX
0	1	A	A	NOT

With the basic logics of AND and OR any digital logic circuit can be developed. So, these functions are designed by using PT, TG and GDI techniques. The AND logic using pass transistors is shown in fig. 2.

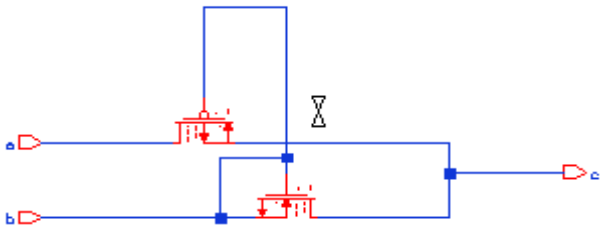

Fig. 2: AND logic using Pass Transistors

Pass transistors consists of two MOS devices one is P-type another is N-type. When the logic '1' is applied to the inputs then PMOS will turn off, logic '1' of 'b' goes to output. If logic '0' is given to the input 'a' then PMOS turns on then that zero goes to the gate of NMOS and drain of PMOS then whatever logic comes from b multiplies with logic '0' and finally the result will be zero. So, here the two inputs are logic '1' then the output will be '1'. If any of inputs are '0' output will be zero which is nothing but AND Logic. The OR logic using Pass Transistors is shown in fig. 3. When the logic '0' is applied to the gate inputs then NMOS will turn off then input 'b' goes to output. If logic '1' is given to the gate input and input 'a' is '0' then NMOS turns on then that zero goes to the gate of PMOS and drain of NMOS then what ever logic comes from 'b' multiplies with logic '1' and finally the result is '1'. So, here the two inputs are logic '0' then the output is '0'. If any one of inputs is '1' then the output as '1' which is nothing but OR Logic.

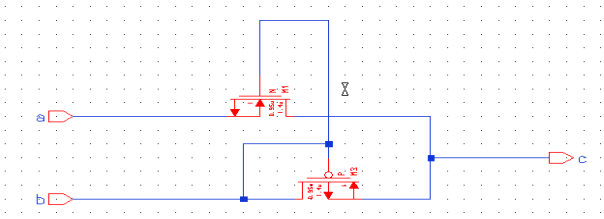

Fig. 3: OR logic using PT Logic

The AND logic can also be implemented by using transmission gate and it is shown in fig. 4.

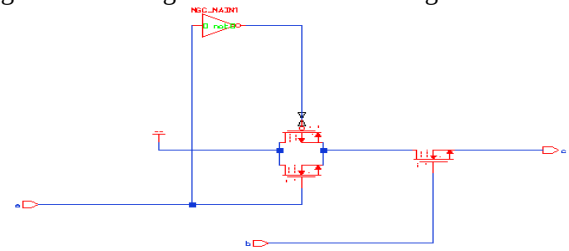

Fig. 4: AND logic using TG Logic.

The transmission gate consists of two NMOS and one PMOS devices. In addition to that of inverter control signals are also present. The control signals

abolishes signal degradation when logic'0' is applied to the input 'a' then through NMOS device turns off and PMOS device turns on and the logic '0' is passed as logic '1' to another NMOS. The gate of the second NMOS device will take the another input through 'b' if that is one then the output will be '1' or logic is zero then the output will be zero irrespective of the input from 'a', which is AND operation. The implementation of OR logic using the transmission gate is shown in fig. 5.

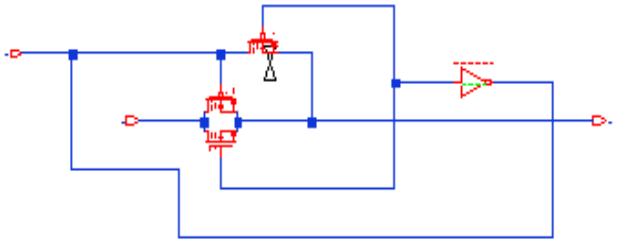

Fig. 5: OR logic using TG Logic

To realize OR logic, uses same devices as AND logic using transmission gate in which it uses one PMOS and two NMOS. When logic '1' is applied to 'a' then passes the same logic to output 'I' irrespective of the input from 'b' hence this is similar to the logic function of OR. The different logic functions can be implemented using this technique. The operation of GDI based AND gate can be explained with respect to basic GDI cell 'P' of the transistor is given '0' it will cut-off from its operation, hence the logic either '1' or '0' at the input 'a' will be reflected at the output 'z'. Thus the output will be z =a*b. The AND logic using the GDI technique is shown in fig. 6.

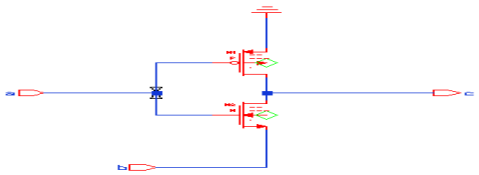

Fig. 6: AND logic using GDI Cell

The GDI cell based OR gate is given in fig. 7. When N of the transistor is given high logic the OR function will be evaluated as follows, when 'a' is '1' the output will be PMOS of the transistor since is given high logic.

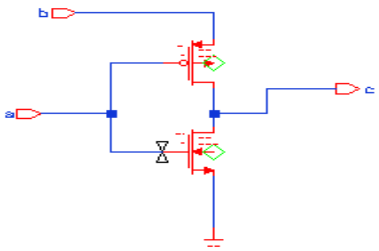

Fig. 7: OR logic using GDI Cell

By using this technique, different digital circuits can be designed with low transistor count as compared with CMOS designs which results in low power dissipation.

2. **Implementation of digital circuits using GDI**

Multiplexers are used as data selectors where as counters are used in timer circuits both of them are very important in digital systems. Since, the power dissipation of these circuits is a major factor it should be as minimum as possible. So, these circuits are implemented with the GDI technique. In this paper, the 4×1 multiplexers 8×3 encoder, BCD counter and mealy machine are implemented with the pass transistor, transmission gate and gate diffusion input technique and their power dissipations are tabulated.

A Multiplexer is a device that selects one of several input signals and forwards the selected input into a single output line. A multiplexer has n select lines of 2n inputs. They are used to select the input line to send the output with the help of selection lines. The development of the 4×1 Multiplexers using GDI Technique is shown in fig. 8.

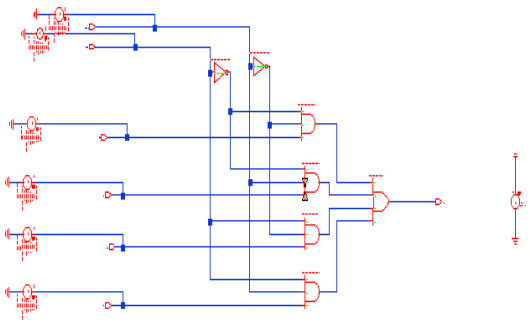

Fig. 8: 4×1 Multiplexer using GDI Cell

Encoder is another digital combinational circuit whose function is quite opposite to that of decoder. It is having 2^n inputs and n number of outputs. Here 8×3 encoder is developed by using PT, TG and GDI. This encoder is used to convert data from octal to binary data. The developed circuit is simulated for power dissipation and the values are tabulated. The development of 8x3 encoder using GDI is shown in fig. 9.

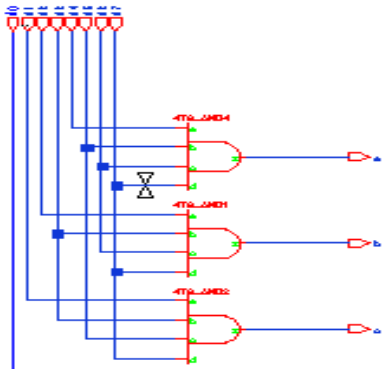

Fig. 9: 8×3 Encoder using GDI Cell

A counter is a device which stores and sometimes displays the number of times a particular event or process has occurred, often in relationship to a clock signal. The counter is a sequential circuit for which optimization of power dissipation is very essential. The power analysis of this circuit is done with pass transistors, transmission gates and gate diffusion input techniques. The BCD counter using GDI is given in fig. 10.

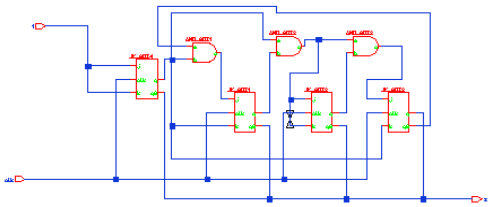

Fig. 10: BCD Counter using GDI Cell

Mealy machine is one of the finite state machine in which the output depends upon the state and inputs. The main advantage with this state machine is, used to reduce the number of states. The mealy machine is developed by using Pass Transistors, Transmission Gates and Gate Diffusion Input. The power dissipation of the Mealy Machine is compared and tabulated. The Mealy machine is shown in the fig. 11.

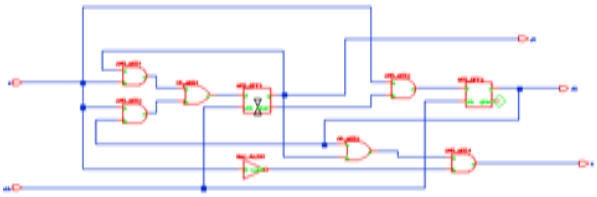

Fig. 11: Melay Machine using GDI Cell

III. Self adjustable voltage level technique

The Self-Adjustable Voltage Level (SAL) circuit can supply a maximum DC voltage to an active load circuit on request or can decrease the DC voltage supplied to the load circuit in standby mode. This technique decrease the leakage current of CMOS logic circuits [5], [15]. Further, this technique can also be extended to the memories and registers because they can retain data even in the stand-by mode.

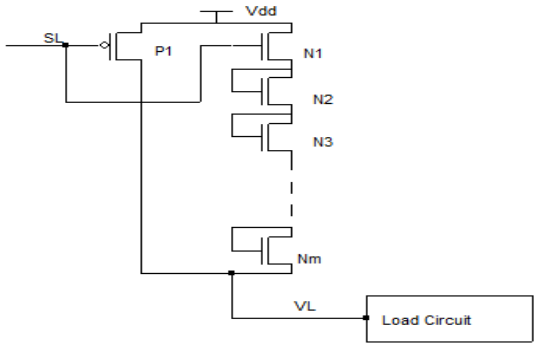

Fig. 12: Self adjustable voltage level circuit

The self adjustable voltage level circuit is given in fig. 12. This circuit consists of a single PMOSFET switch (p-SW) and NMOSFET switches (n-SWs) connected in series. The "on p-SW" (i.e., p-SW that is turned on) connects a power supply and the load circuit in the active mode on request, and "weakly on n-SWs" (i.e., n-SWs that are turned on) connect and the load circuit in standby mode. It should be noted that a gate and a drain of the n-SW1 could be connected. In this work, the load circuits are the digital circuits which are developed by using pass transistors, transmission gates and gate diffusion input. Power dissipations are calculated for each circuit using mentor graphics back end tool and are tabulated in the below Tables 2, 3, 4 and 5 respectively.

IV. Results

The power dissipation of designed digital circuits is analyzed and they are compared with each other with and without self-adjustable voltage level technique. The circuits dissipates less amount of power using pass transistors than transmission gate as it uses less number of transistors.

Table 2. Power dissipation of 4×1 Multiplexer with and without SAL technique

S.No	4×1 Multiplexer	Power dissipation (µW)	
		Without SAL	With SAL
1	Pass Transistors	5.6909	5.2056
2	Transmission Gate	18.8684	15.386
3	Gate diffusion input	2.7740	1.8658

Table 3. Power dissipation of 8×3 Encoder with and without SAL Technique

S.No	8×3 Encoder	Power dissipation (pW)	
		Without SAL	With SAL
1	Pass Transistors	4.5084	2.586
2	Transmission Gate	22.4860	20.847
3	Gate diffusion input	1.2569	1.124

Table 4. Power dissipation of BCD Counter with and without SAL Technique

S.No	BCD Counter	Power dissipation (µW)	
		Without SAL	With SAL
1	Pass Transistors	15.1506	12.365
2	Transmission Gate	36.221	29.3892
3	Gate diffusion input	11.8373	10.8653

Table 5. Power dissipation for Mealy Machine with and without SAL Technique

S.No	Mealy Machine	Power dissipation (W)	
		Without SAL	With SAL
1	Pass Transistors	10.1605 µ	9.657 µ
2	Transmission Gate	15.0023 µ	12.369 µ
3	Gate diffusion input	185.7001p	170.786p

Among the above mentioned three techniques GDI technique dissipates less amount of power as compared with other techniques. The power dissipation of combinational circuits such as multiplexer and encoder, BCD counter are given for three different techniques in figs.13 and 14 respectively. It was observed that, the amount of power dissipated with SAL technique is reduced as compared to without SAL technique. As considered, mealy machine using GDI technique with and without SAL technique dissipates very less amount of power in terms of pWatts; therefore the relation between techniques with power dissipation is not shown in graph representation.

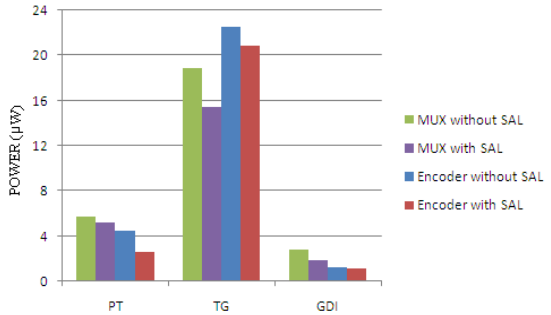

Fig. 13: Power dissipation of combinational circuits

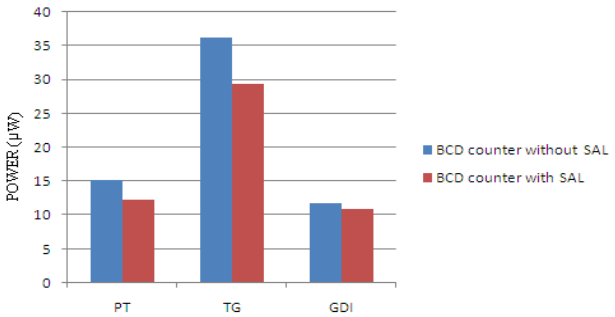

Fig. 14: Power dissipation of BCD counter

V. Conclusion

The digital circuits 4×1 Multiplexer, 8×3 Encoder, BCD Counters and Mealy Machine were developed by using pass transistors, transmission gates and gate diffusion input techniques. The power dissipations are compared and then the self adjustable voltage level technique is applied. This SAL circuit can dynamically reduce drain-source voltages and increase substrate biases of "off MOSFETs" in the standby load circuits. It can therefore increase the sub-threshold voltage of the "off MOSFETs" so that as little standby leakage power as possible. Further, this technique can also be extended to other level circuits for their minimum power dissipation and for optimization of delay, area of the high level circuits.

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