

A Simplified Topology for Seven Level Modified Multilevel Inverter with Reduced Switch Count Technique

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ABSTRACT

In this paper, a seven level modified cascaded multilevel inverter is proposed for industrial drive applications. Apart from selecting the conventional level inverters, Multi level inverters has been chosen for the industrial drive applications as it reduces the total harmonic distortion. The involvement of higher number of switches increases the complexity of the system, which leads to losses in switching, producing huge harmonics and in the end, it entirely reduces the efficiency of the system. The cascaded multilevel inverter involves only fewer switches, where it reduces the complexity of the system which in turn reduces the harmonics and reduces the complexity of the system and in total it reduces the total harmonics distortion.

Keywords – Cascaded Multilevel Inverter, Insulated Gate Bipolar Transistor, Pulse Width Modulation, Total Harmonic Distortion.

I. INTRODUCTION

In recent years, huge industrial applications require high power rating apparatus to improve the efficiency of the system. In conventional two level inverter, it is found that there are many problems in accordance with the high power applications. Owing to this, the implementation of Multi level inverters takes place, which in turn reduces the total harmonic distortion of the entire system. The multi level inverters can be operated at higher switching frequencies while producing lower order harmonic components. In this technique, a H-bridge inverter is introduced (full bridge inverter). The total output voltage is the sum of the outputs produced at each H-bridge cell. For a single phase system, only one H-bridge cell is required, which involves one switch and a diode for each voltage source.

II. CASCADED MULTI LEVEL INVERTER

For a single phase system, the general structure of cascaded multilevel inverter is shown in Figure 1. In this structure, each voltage source is connected in cascade with other sources (V_{dc1} , V_{dc2} , and V_{dc3}) via a H-bridge circuit. Here each H-bridge circuit consists of four active switching elements,

which in turn decides whether the output is to be of positive or negative polarity. The MLI inverter topology employs three voltage sources of equal magnitudes, where it is easy to generalize the number of distinct levels.

Based on the number of stages or sources, the associated number of output level can be written as follows:

$$N_{level} = 2S+1 \text{ ----- (1)}$$

As the proposed level is the seven level multilevel inverter, the value for 'S' is taken as 3 and the output voltage levels can be identified as 3Vdc, 2Vdc, 1Vdc and 0.

In this topology, the numbers of controlled switches are given by the equation

$$N_{switch} = 4S \text{ ----- (2)}$$

The output voltage is given by $V_o = A_1 + A_2 + A_3$ where A_1 , A_2 and A_3 are the DC voltage sources.

The cascaded multilevel inverter is well known for its excellent layout and its packing. The only disadvantage of this topology is that each H-bridge circuit requires separate DC source, which finally leads to high number of semi conductor switches. The output voltage waveform of a seven level cascaded inverter with separate DC source is given in Figure 2.

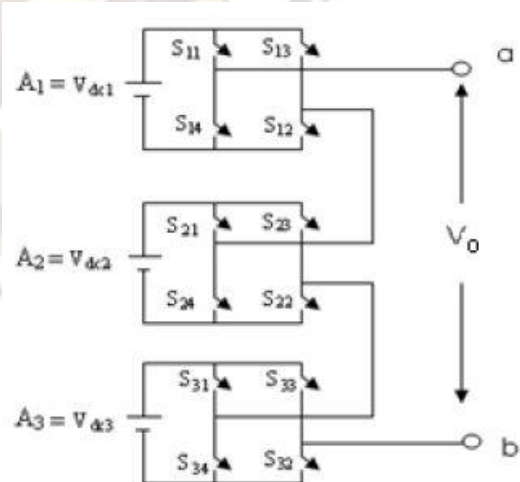


Figure 1. Topology of Cascaded Multilevel Inverter

III. MODIFIED CASCADED MULTI LEVEL INVERTER

The modified cascaded multilevel inverter is a combination of a multi conversion cell and a H-bridge. The proposed multilevel inverter is shown in Figure 3. Here the multi conversion cell consists of three separate voltage sources (V_{dc1} , V_{dc2} , and V_{dc3}). With the help of one active switching element and a diode, each voltage source is connected in cascade with the other source, which leads to the output voltage only in the positive level with several levels. A different control pattern is followed in this topology. First the switch S1 is turned on to obtain the voltage level of $+1V_{dc}$. At this instant switch S2 and S3 are turned off. Similarly, the switches S1 and S2 are turned on to obtain the voltage level of $+2V_{dc}$. Now the switch S3 is turned off. Now the switched S1, S2 and S3 are turned on to obtain the voltage level of $+3V_{dc}$. Apart from producing all the voltage levels at the output stage, a unique procedure of calculating the required dc voltage source is proposed. Pulse Width Modulation is proposed in this topology.

The main advantage of this proposed multi level inverter is obtaining seven level with reduces number of switches.

Based upon the number of DC Sources taken and the associated number output level can be calculated by using the equation

$$N_{level} = 2S+1 \text{----- (3)}$$

As the proposed multilevel inverter is designed for seven level, taking $S=3$, the output will have seven levels as follows: $3V_{dc}$, $2V_{dc}$, $1V_{dc}$ and 0

In this topology, the numbers of controlled switches are given by the equation

$$N_{switch} = 2S+4 \text{----- (4)}$$

The output voltage is given by $V_0 = A_1+A_2+A_3$

where A_1 , A_2 and A_3 are the DC voltage sources.

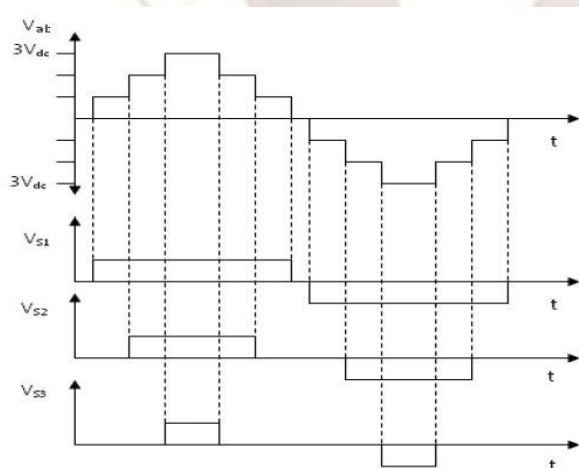


Figure 2. Typical Output Waveform for Cascaded Multilevel Inverter

IV. REDUCTION OF HARMONICS BY PULSE WIDTH MODULATION TECHNIQUE

The most extensively used method for reducing the harmonics in the inverters is the Pulse Width Modulation Technique. In this control, the selected switches are turned ON and OFF several times during the half cycle and the output voltage is controlled by varying the pulse width. Among the existing modulation techniques, sinusoidal PWM is the most widely used method in controlling the motor and inverter application. In order to verify the proposed multilevel inverter topology, programmed SPWM technique is applied in order to determine the required switching angles. This method is applied in order to synthesize the output voltage with desired amplitude and to obtain better harmonic spectrum. It is clearly evident that in order to control the fundamental output voltage and to eliminate the harmonics, 'n+1' equations are needed.

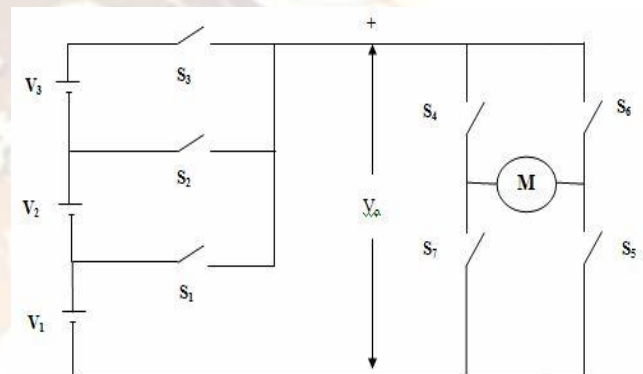


Figure 3. Proposed Topology of the Modified Cascaded Multilevel Inverter

V. TOTAL HARMONIC DISTORTION

Generally harmonics have frequencies that are integer multiples of the waveform's fundamental frequency. The ideal sine wave has zero harmonic components. The Total Harmonic Distortion is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current waveform. The general equation for THD is given by

$$THD = \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2)}}{V_1} * 100\%$$

VI. SIMULATION RESULT ANALYSIS

The proposed modified multilevel inverter for induction motor drive is simulated using MATLAB. The simulated diagram for the induction motor drive using MATLAB is shown in Figure 4. The switching pulse sequence for single phase is given in Figure 5. The output voltage waveform of three phase line to ground voltage and line to line voltages are given in 6a and 6b. For the proposed inverter, the phase voltage is 212 V and line voltage is 370 V. Figure 7a and 7b shows the output waveform of speed and torque curve of induction motor. It is seen that the motor attains the rated speed at 0.8 msec and the torque gets settled down at 0.5 msec. Figure 8 shows the detailed simulink diagram for an individual phase. The output is obtained for the permanent magnet asynchronous machine. Figure 9 shows the FFT analysis. From the FFT analysis it is seen that when the number of levels are getting increased, the harmonics and the total harmonic distortion is reduced. At load conditions, the THD value of the proposed inverter is found to be 33.58%.

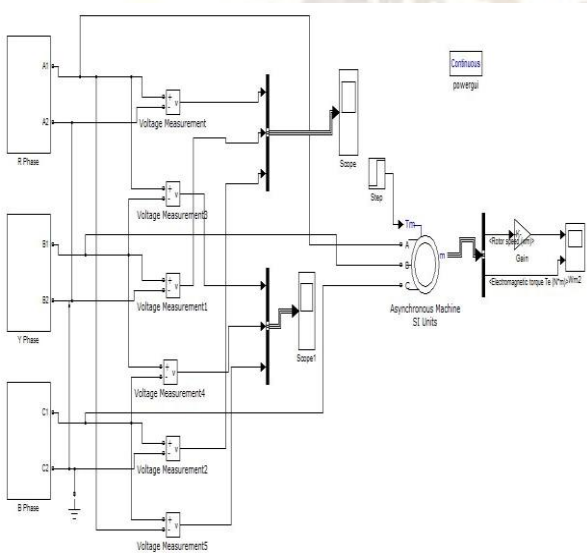


Figure 4. Simulation of the Modified Cascaded Multilevel Inverter

VII. CONCLUSION

From the above inferences, it is clear that the proposed multilevel inverter topology can be used for induction motor drive applications, which involves less number of switches, which in turn reduces the complexity of the system. As the conventional seven level inverter involves twelve switches, it increases the complexity of the circuit, increases switching losses and cost of the circuit is also increased. But in the proposed topology, the same seven levels is obtained with only seven switches, which reduces the harmonics, circuit complexity, reduces the cost and moreover it reduces the total harmonic distortion.

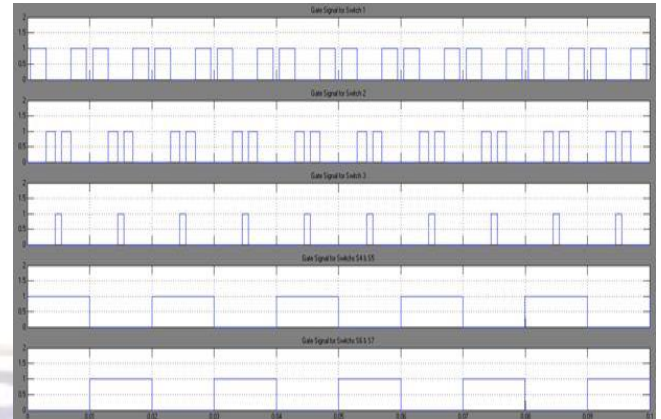


Figure 5. Switching Pulse Sequence of R-Phase

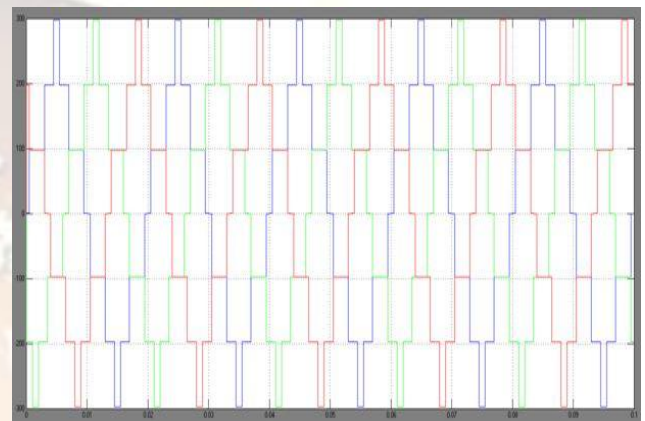


Figure 6(a) Output Voltage Waveform for Three Phase Line to ground

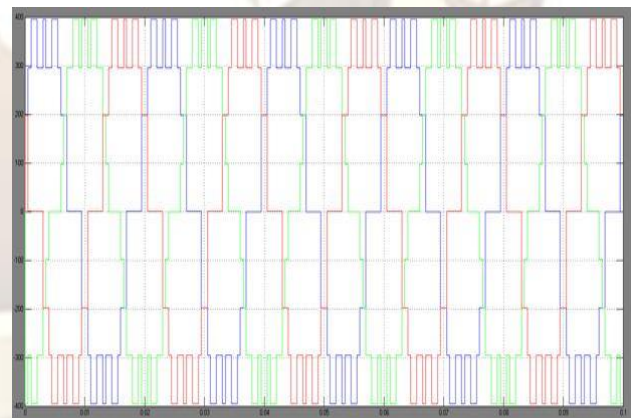


Figure 6(b) Output Voltage Waveform for Three Phase Line to Line

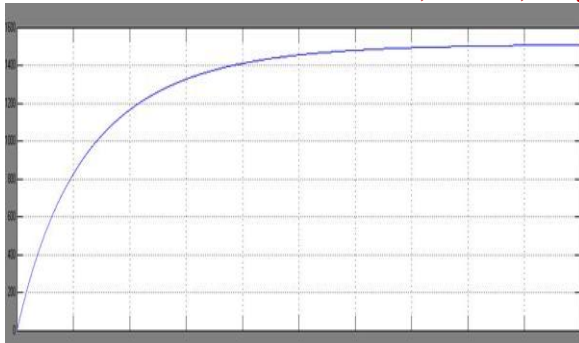


Figure 7 (a) Modified Cascaded Multilevel Inverter – Speed Curve

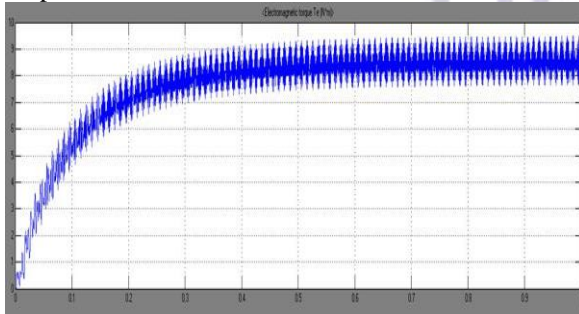


Figure 7 (b) Modified Cascaded Multilevel Inverter – Torque Curve

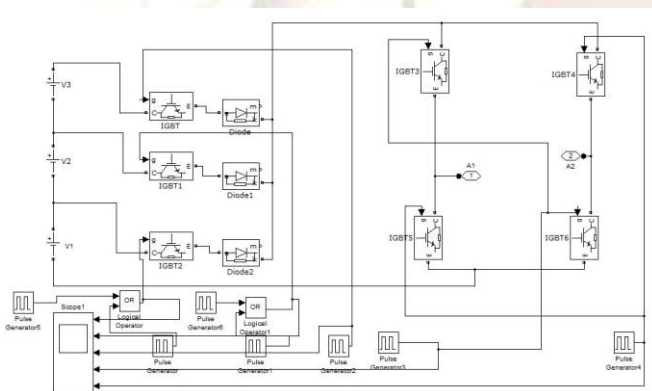


Figure 8. Detailed Model for Individual Phase

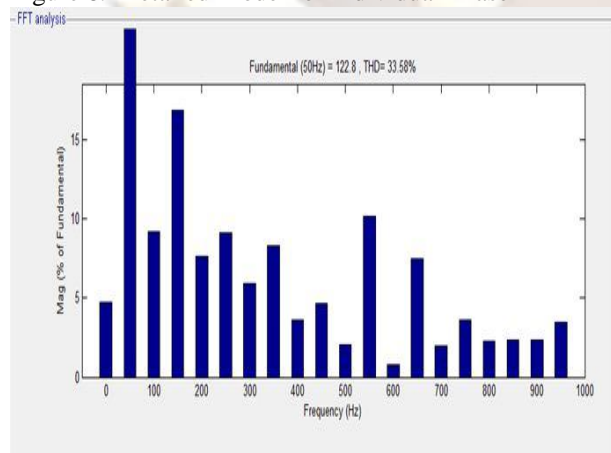


Figure 9 Modified Cascaded Multilevel Inverter – FFT Analysis.

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