Leakage Power Reduction in CMOS

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Abstract

The advantage of scaling devices is to achieve high performance, low power, large integration and low cost continues to be attractive to the semiconductor industries. However, increasing variability in the device characteristics, soft errors and device degradation in CMOS technologies pose major challenges in the future scaling. Variation in process, voltage and temperature cause uncertainty in the worst case critical path delays. Delay Margins or Voltage Margins are added to obtain fully functional chips, but results in high power consumption and/or performance loss.

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems. In VLSI systems, the clock system consumes anywhere between 20-50% of the total chip power with approximately 90% of the clocking power used to drive storage elements such as flip-flops. The significant power consumption of the clock system is mainly due to the 100% transition probability of the clock signal.

Keywords- CMOS, Leakage Power, Static Power, Threshold Voltage, Dynamic Power.

I. INTRODUCTION

The increasing speed and complexity of today's designs implies a significant increase in the power consumption of very large scale integration (VLSI). To meet this challenge, researchers have developed many different design techniques to reduce power. The complexity of today's ICs, with over 100 million transistors, clocked at over 1 GHz, means manual power optimization would be hopelessly slow and all too likely to contain errors. One of the key features that led to the success of complementary metal-oxide semiconductor, or CMOS technology was its intrinsic low-power consumption. Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies.

II. CMOS

CMOS stands for Complementary metal–oxide–semiconductor. It is a technology for constructing integrated circuits. It is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. The CMOS devices are best known for low power consumption. Another interesting feature of CMOS is its nice scaling properties, which has permitted a steady decrease in the feature size allowing for more and more complex systems on a single chip, working at higher clock frequencies. CMOS technology feature size and threshold voltage have been scaling down for decades for achieving high density and high performance. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power [17]. The sub-threshold leakage current of a MOS device can be modeled as follows [10,16]:

$$I_{leak} = I_0 e^{\frac{V_{GS}-V_T}{nV_{th}}}\left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)$$

Where $$I_0 = \mu_0 C_{ox}\frac{W}{L}V_{th}^2 e^{1.8}$$

This equation can be approximated in the equally well known form:

$$I_{leak} \cong \frac{I_0}{W_0}W10^{\frac{V_{GS}-V_T}{S}}$$

Where

$$S = nV_{th}\ln 10$$

Where μ_{eff} is the electron/hole mobility, C_{ox} is the gate capacitance per unit area, W and L are width and length of the channel respectively, V_t is the threshold voltage, n is the sub-threshold swing co-efficient, V_T is the thermal voltage, V_{gs} is the transistor gate to source voltage and V_{ds} is the drain to source voltage. Fig. 1 shows the subthreshold leakage trends with deep-submicron technologies [7, 18].

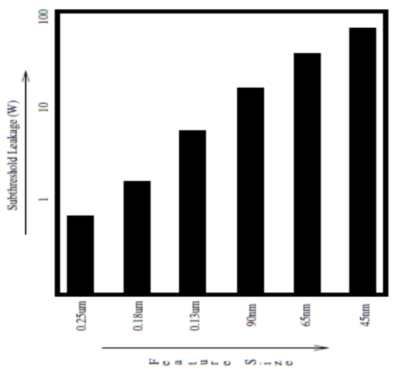

Fig. 1 Subthreshold leakage power trends

III. POWER DISSIPATION

The increasing use of portable and battery operated devices has raised the demand for low power devices. With higher speed and density of CMOS circuits, power dissipation has become a growing concern.

A. Dynamic Power Dissipation

Dynamic power dissipation occurs in the logic gates that are in the process of switching from one state to another. It is caused by the current flow from the charging and discharging of parasitic capacitances.

B. Static Power Dissipation

Static power dissipation is associated with inactive logic gates (i.e., not currently switching from one state to another). It is caused by leakage currents while the gates are idle; that is, no output transitions.

IV. LITERATURE REVIEW

Hiroshi Kawaguchi *et al.* implemented A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction. RCSFF is composed of a reduced swing clock driver and a special flip-flop which embodies the leak current cutoff mechanism. It can reduce the clock system power of a VLSI down to one-third compared to the conventional flip-flop through the reduced clock swing down to 1 V.

Chulwoo Kim *et al.* described A Low-Swing Clock Double-Edge Triggered Flip-Flop. This is developed to reduce power consumption significantly compared to conventional flip-flops. Power consumption in the clock tree is reduced because LSDFF uses a double-edge triggered operation as well as a low-swing clock. The power saving in flip-flop operation is estimated to be 28.6% to 49.6% with additional 78% power saving in the clock network.
Dan Ernst *et al.* implemented about circuit-level correction of timing errors for low-power operation using Razor FF. Here Dynamic voltage scaling is used which is one of the more effective and widely used methods for power-aware computing. .

Subhasish Mitra *et al.* described about Built-In Soft Error Resilience for Robust System Design. It is design technique for correcting soft errors in latches, flip-flops and combinational logic.

Yuji Kunitake *et al.* implemented about A Simple Flip-Flop Circuit for Typical-Case Designs for DSM. In this paper, canary logic is proposed that enables the typical-case design. and is easier to design than the previously proposed Razor logic by eliminating delayed clock. Simulations shows that the canary logic achieves average power reduction of 30%.

David Li *et al.* illustrated Design of a Novel High-Performance Reduced Clock-Swing Pre-Discharge Flip-Flop. These are very attractive in high-performance deep-pipelined systems since significant power reduction can be achieved with minimal performance degradation.

Touqeer Azam *et al.* concluded the robust low power design which provides robust low power circuit operation under different variations at a reduced performance/ power loss. Sensor based design methodology was presented that minimizes pessimistic margin, while providing reliable circuit operation.

Kavita Mehta *et al.* enumerates about Low Power Efficient D Flip Flop Circuit that explains low power, high speed design of D flip flop. In this various techniques to minimize sub threshold leakage power as well as the power consumption of the CMOS circuits was presented. It shows a design for D flip flop to increase the overall speed of the system as compared to other circuits to achieve low power consumption with minimum transistor count.

Uma Nirmal *et al.* enumerated A Low Power High Speed Adders using MTCMOS Technique. Addition is the most basic arithmetic operation and adder is the most fundamental arithmetic component of the processor. Several adders can be implemented in many ways such as carry look-ahead (CLA), carry-skip adder (CSA) and ripple carry adder (RCA) depending on the delay and power consumption requirements. MTCMOS is an effective circuit level technique that provides a high performance and low-power design by utilizing both low and high-threshold voltage transistors.

Yuji Kunitake *et al.* worked on the Possibilities to Miss Predicting Timing Errors in Canary Flip-flops. An alternative timing-error-predicting FF named canary FF and its critical issues has discussed in this paper. Simulations unveil that canary FF occasionally misses predicting timing errors.

M. Janaki Rani *et al*. analysed about leakage power reduction and analysis of CMOS sequential circuits. A significant portion of the total power consumption is mainly due to leakage power. It is important to reduce leakage power in portable systems. In this paper two techniques such as transistor stacking and self-adjustable voltage level circuit for reducing leakage power in sequential circuits are described. Simulation results show that the proposed pass transistor based D flip-flop using self-adjustable voltage level circuit has the least leakage power dissipation of 9.13nW.

V. PROPOSED WORK

In the proposed work for Leakage power reduction, Performance Analysis of various kinds of flip flops e.g. RCSFF, Gated D, Set D, J-K, MTCMOS type D Flip Flop will be done at different values of supply voltages, temperatures to find which will perform better.

VI. CONCLUSION

In low power applications area and power consumption by the device are the main technological aspects to prefer a design over the other contending designs. In this paper various literatures have studied and based on all the above comparisons among different techniques will be done to find which one is better.

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