

High Speed-Low Leakage-Multi Threshold 45 nm Floating Gated SRAM

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ABSTRACT

An asymmetrically six-transistor (6T) high speed low leakage multi V_{th} 45nm Floating Gated (FG) SRAM circuit is presented in this paper to suppress the power dissipation and leakage current. By using conventional external circuitry (decoder part, read-write circuitry part, voltage control switch part etc.), this technique is reduce up to 83.29% power dissipation and 290.5 times leakage current and also 2.52 times high speed in 45 nm technology. For minimizing power dissipation and leakage current, the function of multi V_{dd} and multi V_{th} concept are also included in that paper. Also the total read-write architecture block diagram is included in that paper.

Keywords – Floating Gate, Multi V_{dd} , Multi V_{th} , Read-Write Architecture, SRAM.

1. INTRODUCTION

Selecting of suitable component, not only there intended task but also external and internal operating condition as well as their operating limits (current, voltage and power) is still a big challenge in modern electronic circuit design. Similarly for a standard system-on-chip (SoC) or microprocessor, leakage current takes an important role in their memory elements which is mainly recognized as RAM and ROM [4]. Data mismatch, data loss, access time variation and so many other incidents occurs in the memory cell due to leakage current. To increase the speed of SoCs or microprocessors a huge amount of high speed cache memory (data cache, address cache and translation look-aside buffer) is required which is mainly constructed with SRAM cells. But for that the power supply, mutable data stability, leakage current, internal heat, reduce area come into the picture together, which become a primary challenge of SRAM cell designing.

The paper is organized as follows. Section 2 represents the basic of floating gated MOSFET. Conventional 6T SRAM circuit-operation is on Section 3. Proposed floating gated design and work function is on Section 4. Total circuit architecture and the resulting output on Section 5 and Section 6. The paper is concluded in Section 7.

2. FLOATING GATED MOSFET

A Floating gate MOS can be fabricated by standard MOS transistor and register-capacitor logic, so that resistive connection to its gate are not present. The electrically isolated secondary gates or inputs are implanted to the above floating gate (FG) are mainly capacitively connected to the floating gate which is completely surrounded by highly resistive material. So, in terms of its operation, the number of inputs act as floating inputs of the transistor [1].

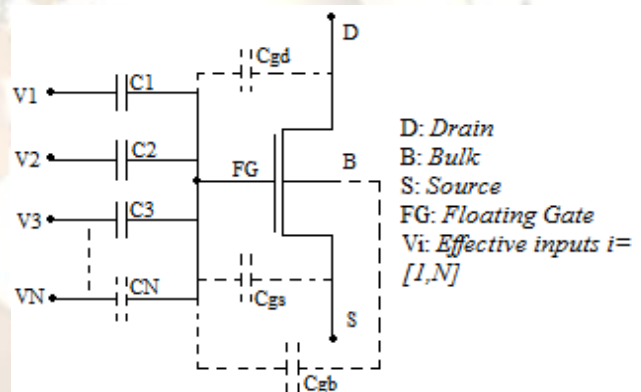


Figure 1. N-channel N-input FGMOS Transistor

3. CONVENTIONAL 6T SRAM

The conventional six transistor (6T) SRAM cell using multi V_{th} in 45 nm technology which is mainly characterized by the hold stability using cross couple inverters during the read-write operation, shown in Figure 2. The design of the data storage nodes which is directly connected with the bit-lines can be accessed through the pass transistors. Voltage deviation which is mainly associated with the cross coupled inverters and the pass transistors because of the leakage current, hamper the storage nodes.

Another important issue is the external noise, which is directly affect the read-access mechanism, which is so called known as destructive read of a standard 6T SRAM [5] and affect is read-write violation.

To maintain the data stability and high speed access the sizing (β ratio) of the cross coupled inverter transistors and the access transistors contain

a big role [6]. For maintaining the read and write stability the cross coupled transistors M_1 and M_3 (for read) and M_2 and M_4 (for write) must be stronger as compared to the access transistors M_5 and M_6 . But in case of the low leakage purpose in 45 nm technology the V_{th} of the M_5 and M_6 must be higher than the access transistors $M_1, M_2, M_3,$ and M_4 .

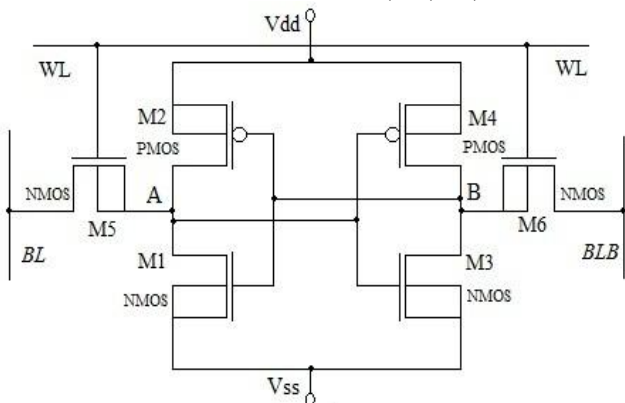


Figure 2. Conventional 6T SRAM cell (M_5 and M_6 High_ V_{th} and M_1, M_2, M_3, M_4 Normal V_{th})

Normally BL and BLB are precharged by V_{dd_Low} when the particular SRAM address is not selected. In both read-write operations the access transistors M_5 and M_6 are in saturation mode. For write '1', BL must be 1 and BLB must be 0, because of WL is high the transistor M_5 and M_6 are on and for that M_2 and M_3 are on and V_{dd} value is appeared into node A. For read operation, the stored value from node A goes to the BL and node B goes to the BLB and sense amplifier sense the value. In case of zero (0) the opposite phenomena will occur [2].

4. PROPOSED MULTI V_{TH} FLOATING GATED SRAM

In the proposed work of the paper there are two input NFGMOS and PFGMOS are implemented. The cross coupled inverters are replaced by PFGMOS and NFGMOS.

One of the inputs of both FG_MOSs is biased mode for tuning the MOS (V_{th}) (basically hear I use positive bias voltage for NFGMOS and same negative bias voltage for PFGMOS) and another input is used as operational input. The design of the proposed circuit is typically characterized by the ratio (β) of the size of the pull-down transistors to the access transistors.

Precharged case and the read-write operation are similar as the conventional 6T SRAM circuitry. For write zero (0) BL must be zero and BLB must be one which is controlled by the hole circuitry which is mention in the block diagram later on. For the high gate voltage (WL high) the access transistor are on and for that M_1 and M_4 are on and the node A value is grounded, so zero is stored on node A and node B stored the opposite one.

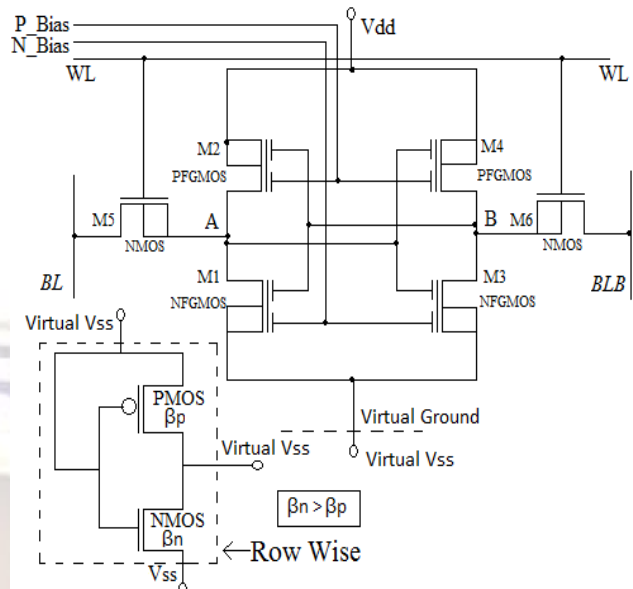


Figure 3. Six transistor (6T) Multi Vdd AND Multi Vth Floating Gated SRAM (M_5 and M_6 High_ V_{th} and M_1, M_2, M_3, M_4 Low_ V_{th} and M_7 Low V_{th} and M_8 High_ V_{th})

For read operation, the stored value from node A goes to the BL and node B goes to the BLB and sense amplifier sense the value. In case of one (1) the opposite phenomena will occur. Comparison of the both cases with the conventional 6T SRAM operation 83.29% power dissipation is reduced as well as speed is increased by 2.52 times for high current flow. The row wise virtual ground mechanism using inverting circuit ($\beta_n > \beta_p$) will also reduce the leakage current up to 290.5 times, it is because there are no option for grounding of the main circuit.

5. TOTAL CIRCUIT ARCHITECTURE

The total circuit apart from SRAM cell array there are sense amplifier and write driver which are work together as read-write circuitry, row decoder and column decoder both for address location, write enable and bit line voltage level switch are work together as multi V_{dd} [3] (V_{dd_High} and V_{dd_Low}).

For a particular SRAM which address is selected by the decoder section is used only V_{dd_High} and rest of SRAM array are controlled by V_{dd_Low} of power consumption of the whole architecture. Based on CD (column decoder) the circuit will precharged ($CD=1$) or enable for read-right operation ($CD=0$). When $CD=0$, the row decoder will activate and put high signal for desire SRAM row (word line) for operating particular SRAM (1Bit). At that time the by data in pin processor will store its desire data to the whole SRAM array.

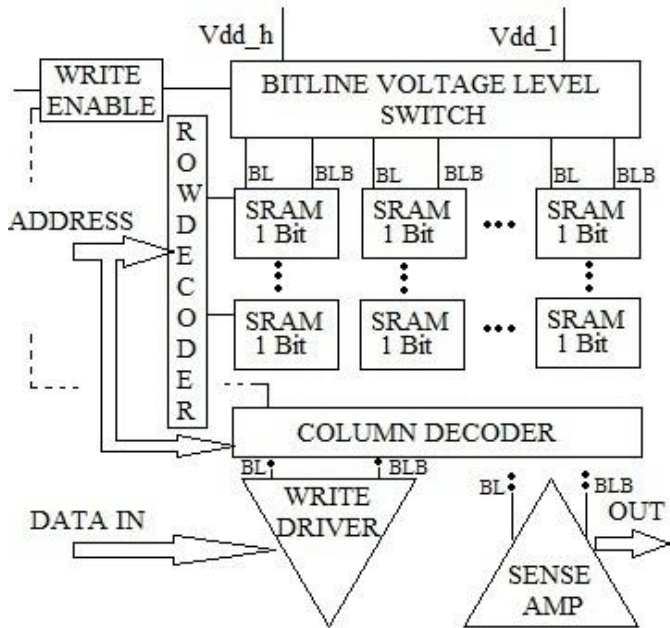


Figure 4. Block diagram representation of total circuit architecture

6. SIMULATION RESULTS

The simulation result of the total circuit using conventional 6T SRAM and 6T Floating Gate SRAM is shown in Figure 5 and Figure 6. It is clear from the output graph that the read and write operation is only done while particular address is selected by the microprocessor.

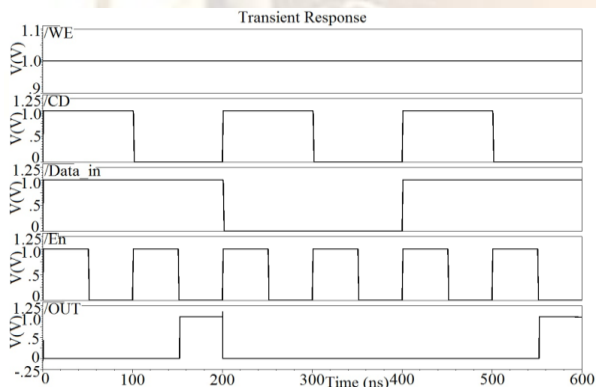


Figure 5. Total circuit output graph (conventional 6T SRAM) (Transient analysis time=0s – 600ns) (En: Enable, when '0' sense amp. will on and when '1' write driver will on and opposite case they are in off state, OUT represent the read write operation of 1 Bit conventional SRAM)

WE (Write enable) enable the total circuit. Based on CD (column decoder) the circuit will precharged (CD=1) or enable for read-right operation (CD=0).

When CD=0, the row decoder will activate and put high signal for desire SRAM row (word line) for operating particular SRAM (1Bit). In the both graph it is clearly visible that data in line is both 0 or 1 and accordingly write driver write it into the SRAM and

sense amplifier sense it, which is plotted on OUT line.

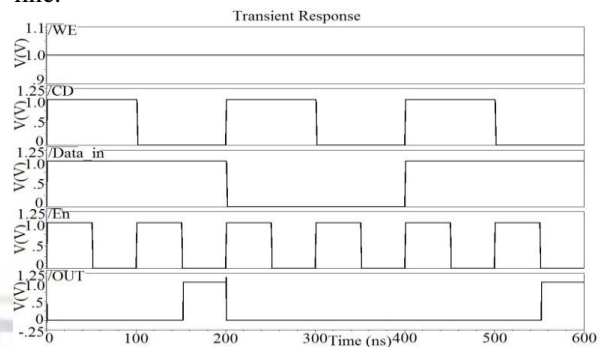


Figure 6. Total circuit output graph (6T Floating Gate SRAM)(Transient analysis time=0s – 600ns) (En: Enable, when '0' sense amp. will on and when '1' write driver will on and opposite case they are in off state, OUT represent the read write operation of 1 Bit conventional SRAM)

6.1 Power Dissipation

Apart from the SRAM cells the total circuit of conventional 6T SRAM and proposed SRAM are properly working at 980 mV.

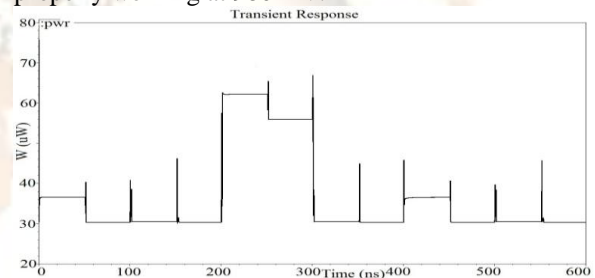


Figure 7. Graphical representation of power dissipation of conventional circuit (transient analysis time=0s – 600ns)

But the average power dissipation using multi V_{dd} and multi V_{th} is drastically reduce up to 83.29% using the proposed technique, where conventional SRAM work at minimum of 980 mV as well as proposed SRAM at 320 mV.

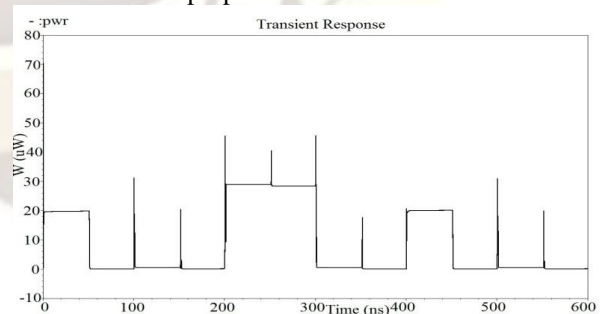


Figure 8. Graphical representation of power dissipation of proposed circuit (transient analysis time=0s – 600ns)

6.2 Read-Write Speed

SRAMs hold data that is frequently accessed by the processor. The faster the access, the faster the data transfer from SRAM to CPU. The

data fetching and writing speed is depending on read-write circuitry and SRAM array combined. As far our calculation from delay calculator we found proposed SRAM circuitry is 2.52 times faster than conventional SRAM circuitry.

6.3 Leakage current

Computer memory which does not require refresh operation is SRAM. But in case of hold data it has some leakage current which is very less compare to the other computer memory.

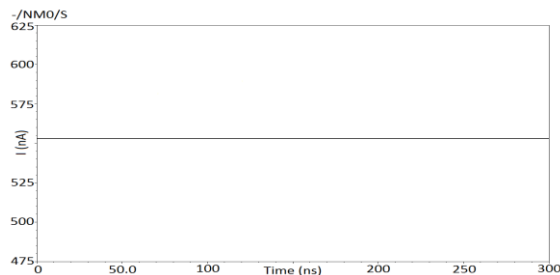


Figure 9. Graphical representation of leakage current of conventional circuit (transient analysis time=0s – 300ns)

The stability of a particular SRAM is inversely proportional of the leakage current. So the proposed SRAM is very much stable (290.5 times) compare to the conventional SRAM because of its low leakage current.

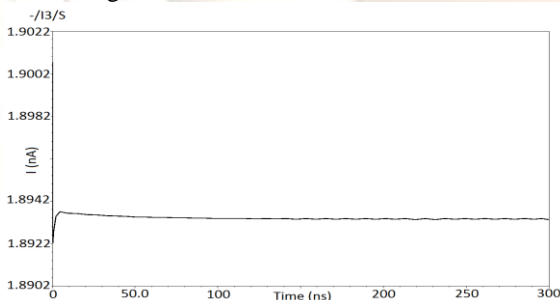


Figure 10. Graphical representation of leakage current of proposed circuit (transient analysis time=0s – 300ns)

Table 1. Performance Comparison of different SRAM circuits

Operation	1Bit Conventional 6T SRAM	1Bit Floating Gated 6T SRAM
Operating Voltage	980 mV	320mV
Total Circuit Operating Voltage	980 mV	980 mV
Total Circuit Avg. Power Dissipation	36.23E-6 W	6.055E-6 W
Read- write operation time	0.78 ns	0.31 ns
Leakage Current	550 nA	1.893 nA

7. CONCLUSION

High speed low leakage multi threshold 45nm floating gated SRAM which will reduce the active and standby mode power dissipation as well as enhancing the data stability and read-write mode as well as hold time leakage current and increasing the read-wright speed is proposed in this paper. Up to 83.29% power saving and 2.52 time faster speed and 290.5 time more stability are achieved with the proposed floating gated SRAM as compare to the conventional design. The above circuit design and simulation is on Cadence Virtuoso environment.

ACKNOWLEDGEMENT

First of all I would like to thank both of my guide G.L.Kumar Moganti and Dr. S.K.Mandal for guiding me throughout the research part.

I am also grateful to my friends Lopamudra Pattanayak, Abhinab Anand, Srijan Chattacharjee and Pratik Ganguly for all their helping hands during my days of research.

I am also thankful to all the staffs and employees of School of Electronics Engineering of KIIT University.

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