Rashmi Sharma, Anshuman Singh, Dr.V.K Pandey / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 3, Issue 2, March -April 2013, pp.1847-1851

Analysis and comparisons of Power Dissipation for Write operation in Low Power SRAM

Rashmi Sharma*, Anshuman SinghDr.V.K Pandey*****

*(Department of Electronics, N.I.E.T Greater Noida-201306, U.P)
** (Department of Electronics, N.I.E.T Greater Noida-201306, U.P)
*** (Department of Electronics, N.I.E.T Greater Noida-201306, U.P)

ABSTRACT

This paper presents the reduction in dynamic power dissipation during write operation.Todays microprocessor are very fast and require fast caches with low power dissipation. The result of 8T SRAM cell is comparing with conventional 6T SRAM and 7T SRAM on different frequency. The whole thesis circuit verification is done on Tanner tool. Schematic of the SRAM cell is designed on S-Edit and Net list Simulation done by using T-Spice and waveforms are analyzed through W-EDIT. The circuit is characterized by using the 130nm technology which is having q supply voltage of 1.5volt.The result are compared with conventional 6T SRAM, 7T SRAM and 8T SRAM cell. So this type of memory cell will be more useful in portable electronics and battery operated devices.

Keywords – Power Dissipation, CMOS, Threshold Voltage, 8T SRAM, 130nm.

1. INTRODUCTION

SRAM is mainly used for the cache memory in Microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to High speed and low power consumption. With the increased SRAM sizes, the leakage is becoming a growing concern [10]. Besides, the leakage current increases with technology scaling, hence, dc power minimization has become a priority and been addressed by innovative solutions [1], [3] Dynamic Dissipation is due to the Charging and discharging of load capacitances**.** CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched. In one complete cycle of CMOS logic, current flows from V_{DD} to the load capacitance to charge it and then flows from the charged load capacitance to ground during discharge. Therefore in one complete charge/discharge cycle, a total of $Q=C_LV_{DD}$ is thus transferred from V_{DD} to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage
Again to get the characteristic switching power dissipated by a CMOS device:

$$P = CV^2 f.$$

There are different techniques to reduce the Write Power Consumption like, Virtual grounding [2], Robust Fin-FET based SRAM design, Charge sharing Techniques [4], in this method a low-power write scheme by adopting charge sharing technique. By reducing the bit-lines voltage swing, the bit-lines dynamic power is reduced [9-5]. Divided Word line scheme [6], and hierarchical divided bit line approach for reducing active power in SRAM by reducing bit Capacitance [7]. All the scope paper is used extra circuitry for reducing the power consumption. This paper presents the comparison of power dissipation for write operation. In this paper the 8T SRAM cell which consumes lesser Power as compare to 6T SRAM and 7T SRAM cell on different frequency. The SRAM cell contains two extra tail transistors in the pull-down path of the respective inverter to avoid charging of the bit-lines. These two trail transistor are controlled by an extra signal write select (WS). During read or write mode at least one of the tail transistor must be turned OFF to disconnect the driving path of respective inverters.

2. CONVENTIONAL 6T SRAM CELL:

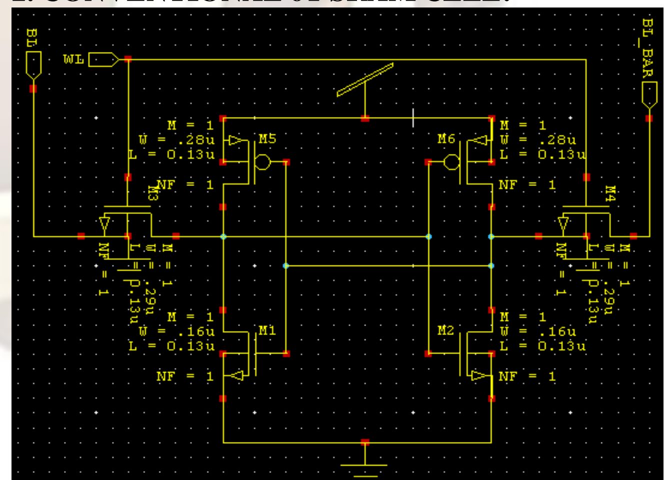

Fig2.1: 6T SRAM cell

Write mode:

Figure2.1 shows the write mode of conventional SRAM cell. Word line is used for enabling the access transistors M1 and M2 for write operation [8].The start of a write cycle begins by applying the

value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting Bit to 0 and Bit bar to 1. This is similar to applying a set pulse to a SR-latch, which causes the flip flop to change state. 1 is written by inverting the values of the bit lines. Word Lines is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily over ride the previous state of the cross-coupled 2 inverters. Careful sizing of the transistors in a SRAM cell is needed to ensure proper operation.

3. 7T SRAM CELL :

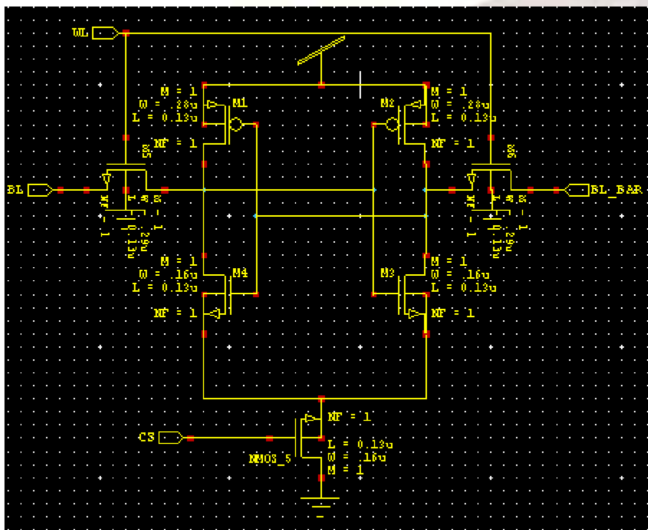

Fig3.1: 7T SRAM cell

Write Mode

In the write "1" mode, node B must be written to high value that is done by setting CS to 0 and asserting word lines signal and the data value is apply to the bit lines and possible case is writing the cell state from "1" to "1". Because both nodes B and CS are 0, no state transition arises in this case. Another possible case is. In this case, because access transistor N4 has much larger conductance than P2, it is easy to flip the cell state from "0" to "1" by discharging node B through N4. When the data is written
from zero to one corresponding path is shown in the fig3.2

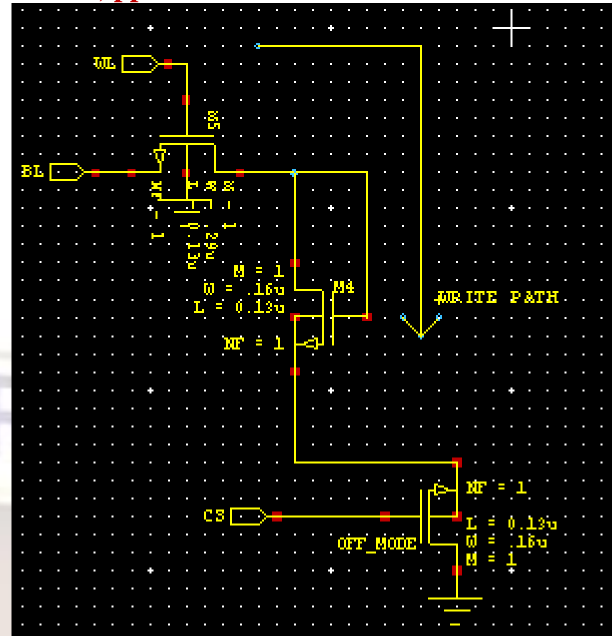

Fig3.2: The path in writing cell state from '0' to '1'.

Similarly the write "0" will be done in the low power SRAM cell the path of the circuit is shown in the fig3.3.

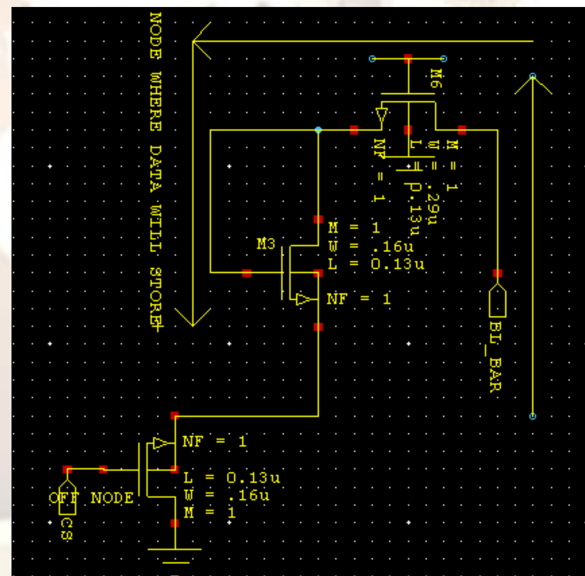

Fig 3.3: The path in writing cell state from'1' to '0'

4. 8T SRAM CELL

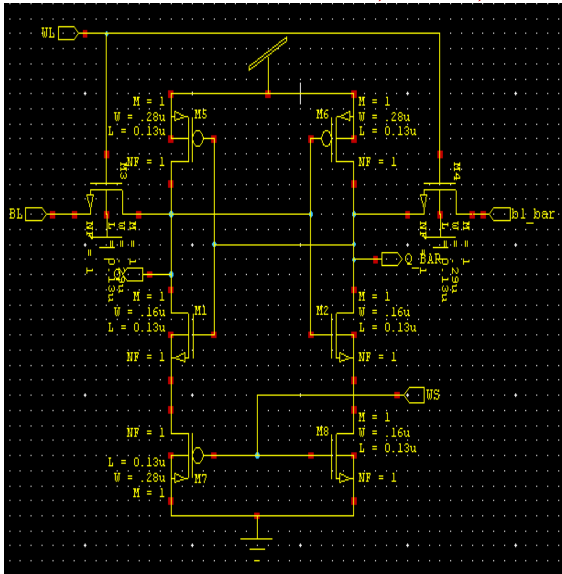

Fig4.1:8T SRAM

Write mode:

In dynamic logic circuits, the two bit-lines are recharged initially to power supply (VDD). When the write enable signal is asserted, the input data and its complement are placed on the BL and after that, asserting "1" on WL one can perform the write operation in the conventional SRAM cell. The bit-lines are the most power consuming Components in the conventional SRAM cell because of large power dissipation in driving the long bit-lines with larger capacitance. Since, write consumes considerable larger power due to the full voltage swing on the bit-lines,

Therefore, in the present paper we have given more emphasis on the write operation. We will consider two write operation in detail for our proposed SRAM cell. In our proposed cell, for write operation we will select Write Select as per Operation. Proposed cell mainly contains 8-transistors. We will consider two write modes:

1.) Write "1" mode. In write "1" mode, node B must be written to low that can be achieved by setting BL to "0" and asserting WL. Path for write "1" operation is shown in fig:
4.2.

The two possible cases are:

Case I: writing the cell state from 1 to 1. This is not possible because both node B and BL are at zero potential. Case II: writing the cell state from "0" to one (0 -1). In our proposed cell, it is easy to flip the cell state from 0 to 1 by setting WS is high before asserting WL.

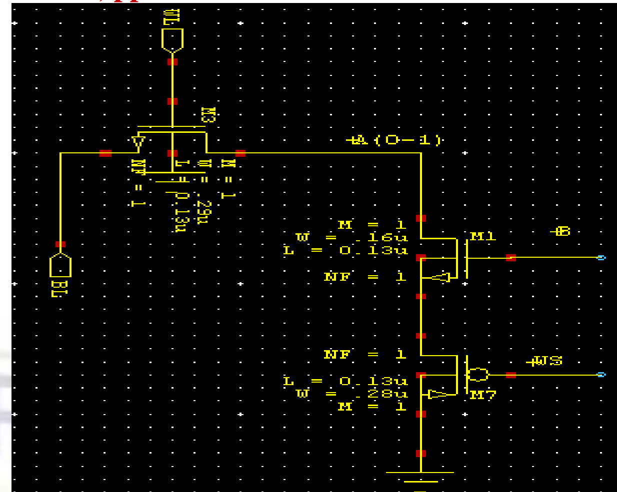

Fig4.2: Path for write "1"

2.) Write "0" mode. In write "0" mode, the node B must be written to high that is done by setting BL to VDD and asserting WL. Path for write "0" operation is shown in the fig. 4.3.

The two possible cases are:
Case I: Write pattern is 0 - 0, since node B is initially
high therefore this write pattern is not possible.
Case II: 1 - 0. This write pattern can be easily performed
in our proposed cell by setting WS is low, so that pull down
path through driver transistor M2 of inv-B is disconnected.
Now assert WL is high to perform the desired write pattern.

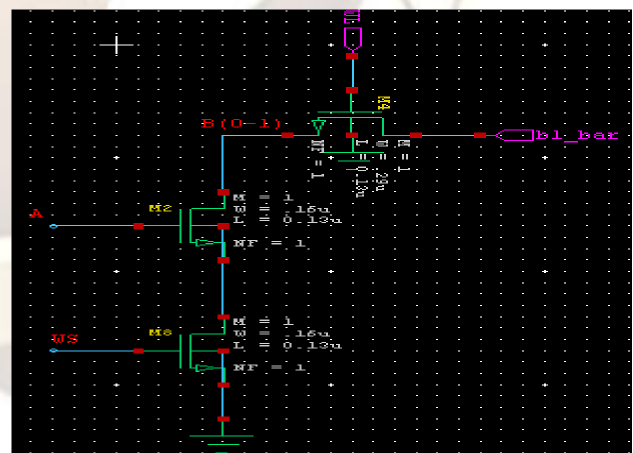

Fig4.3: path for write"0"

In our proposed circuit, the WS signal is used to ensure the correct operation and by selecting proper value of signal
WS before asserting WL, transition from 1 - 0 and 0 - 1 can
Be easily allowed. The two pull down transistor are used to reduce the Sub threshold current which is

flowing in the circuit when transistor is in Cut Off region. This leakage current is dependent on Threshold Voltage. As the threshold voltage decrease the Sub-threshold current increases. Because of drain induced barrier lowering (DIBL) in the MOSFET the threshold voltage decreases as the Drain voltage increases. This may be expressed as:

Where

$Vth' = Vth - ή\, vd$

$ή$=DIBL coefficient

Vth is threshold voltage and Vd is drain voltage

The use of two trail transistor is reducing the drain voltage which increases the threshold voltage. The increase in threshold voltage results in decreased sub-threshold current which reduces the power dissipation. This size configuration provides the proper driving voltage to transistor for ON and OFF condition.

5. RESULT AND DISCUSSION

To evaluate the dynamic power dissipation during the Write operation in CMOS SRAM cell for different frequency. This section provided the detail simulation analysis of Proposed SRAM cell. The schematic of SRAM cell is designed and implemented by using Tanner EDA for simulation. The proposed design has been simulated using 1.5V power supply at 130nm CMOS technology, for different frequencies. The dynamic power may be expressed as: $P=\alpha CV^2 f$.

Since most gates do not operate/switch at every clock cycle, they are often accompanied by a factor α, called the activity factor. A clock in a system has an activity factor α=1, since it rises and falls every cycle. Most data has an activity factor of 0.1. If correct load capacitance is estimated on a node together with its activity factor, the dynamic power dissipation at that node can be calculated effectively. So as the frequency increases the dynamic power dissipation also increases because the Dynamic power depends upon the operating frequency.

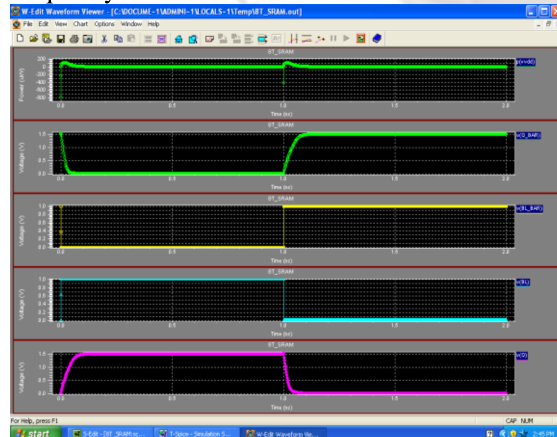

Figure5.1:8T SRAM cell for 500MHz.

The simulation results have been shown in fig-5.1, 5.2, and 5.3 for 500MHz, 1GHz and 2GHz frequencies respectively. It is clear from the figures, as the frequency increases the charging and discharging time is also increases which may cause the increase in power dissipation. But still 8T SRAM cell Dissipate less power in comparison to Conventional
SRAM cell and 7T SRAM cell.

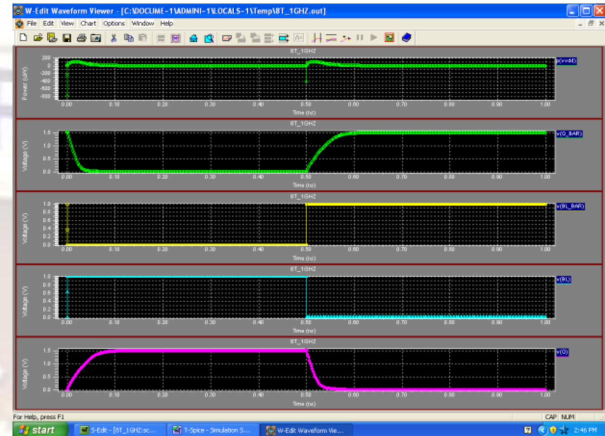

Figure5.2:8T SRAM cell for 1GHz

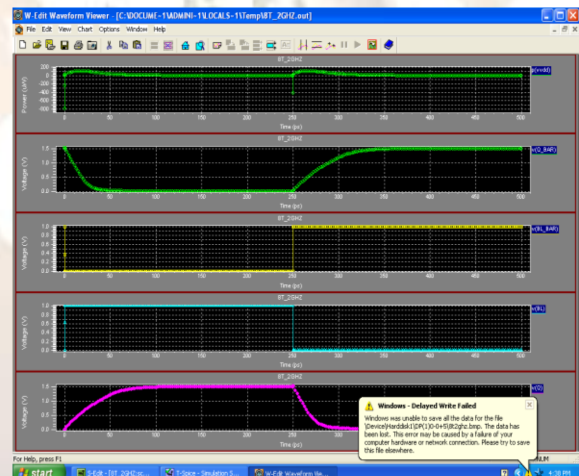

Figure5.3:8T SRAM cell for 2GHz.

Table1: Comparison Table of all SRAM Cells

Frequencies	Power Dissipation in 6T SRAM cell (μw)	Power Dissipation in 7T SRAM cell (μw)	Power Dissipation in 8T SRAM cell (μw)
500MHz	3.58	3.024	2.325
1GHz	6.75	5.52	4.72
2GHz	9.854	9.232	8.782

From the figure 5.2 it has been clear that for 1 GHz the charging time is less then discharging time. Similarly from the figure 5.3.

So due to increment in charging and discharging time with frequency the power dissipation will also

increase. In the conventional SRAM cell, one of the two bit lines must be discharged to low regardless of written value, therefore the power dissipation in both write "0" and "1" is more. In our 8T SRAM cell as shown in figure 4.1 we are preventing any single bit line from being discharged during write "0" as well as write "1" mode by proper selection of signal WS, which turn either M7 or M8 OFF. The comparison of conventional SRAM cell and proposed SRAM cell for Write operation on different frequencies, are given in Table I. Our 8T SRA cell dissipates lower dynamic power during the switching activity. In 8T SRAM cell the crosstalk voltage values are increased for bit lines, word line (WL) and for outputs in comparison to conventional SRAM cell but these
values can be controlled with the help of proper sizing of Width (W) and Length (L) of the transistor.

6. CONCLUSION AND FUTURE WORK

Most of the developed low-power SRAM techniques are used to reduce only read power. Since, in the SRAM cell, the write power is generally larger than read power. We have proposed an SRAM cell to reduce the power in write operation by introducing two tail Transistors in the pull-down path for reducing leakages. Due to these Stack transistors the power dissipation has reduced from 12 to 38 % in comparison to Conventional 6T SRAM cell. 8T SRAM provides power efficient solution at different frequencies. Although numbers of transistors are increased but relative power dissipation is reduced. In future work will be designed area efficient 4-K memory by using Proposed SRAM cell with the help of Layout Design Techniques. This proposed SRAM cell can be used to provide low power and low cost solution for portable devices like laptops, mobile phones etc.

REFERENCE

[1] Yung-Do Yang and Lee-Sup Kim, "A Low-Power SRAM Using Hierarchical Bit Line and Local Sense Amplifiers" IEEE Journal of solid state circuits, VOL. 40, NO. 6, JUNE 2005.

[2] "Segmented Virtual Ground Architecture for Low power Embedded SRAM" IEEE Transaction on Very Large Scale Integration (VLSI) system" , Vol.15, No.2 February 2007, Page.196-205.

[3] "Low Standby Power and Robust FinFET Based SRAM Design" IEEE Computer Society Annual Symposium on VLSI, Jan 2008 Page no. 185-190 Behzad Ebrahimi, Saeed Zeinolabedinzadeh, and Ali Afzali-Kusha.

[4] "Low Power SRAM Design Using Charge Sharing Technique" ,Gu Ming, Yang Jun, Xue Jun, National ASIC System Engineering Technology Research Center Southeast University, Page no-102- 105 IEEE-2005.

[5] Mai, K.W., Mori, T., Amrutur, B.S., Ho, R., Wilburn, B., Horowitz, M.A., Fukushi, I., Izawa, T. and Mitarai, S. (1998), "Low power SRAM design using half-swing pulsemode techniques", IEEE J. Solid-State Circuits, Vol. 33, pp. 1659-71.

[6] "A Low Power 256 KB SRAM Design", Basabi Bhaumik, Pravas Pradhan, G.S. Visweswaran, R. Varambally, Department of Electrical Engineering, IIT Delhi, Hauz Khas, New Delh in 2008.

[7] " Low Power SRAM Design using Hierarchical Divided Bit-Line Approach" , Ashish Karandikar, Keshab K. Parhi, Intel Corporation, Santa Clara, CA 95052, USA-2009.

[8] Vkita, M. et al. (1993), "A single-bit line cross-point cell activation (SCPA) architecture for ultra-low power SRAM's", IEEE J. Solid-State Circuits, Vol. 28, pp. 1114-8.

[9] CMOS VLSI Design By Neil H.E.Weste, David Harris, Ayan Banerjee, Pearson Education, Third Edition, Page 55-57.

[10] A. Tajalli and Y. Leblebici, "Leakage current reduction using subthreshold source-coupled logic," IEEE Trans. on Circ. And Syst.-II, vol.56, no.5, pp.347-351,May2009.