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An Area Efficient Reversible Multiplier Circuit Design By Using Low power Technique

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ABSTRACT

Power dissipation is one of the most important factors in the VLSI circuits design. By using reversible technique to reduce the power in the circuits. In this paper the reversible multiplier circuit design is also done by using low power technique called GDI and to compare the area and power of the multiplier in this technique with CMOS technique. In this paper a 4x4 reversible multiplier circuit is proposed with the design of two new reversible gates called ABC and GPS gates. The proposed multiplier was efficient to existing designs in termsof gate count, garbage inputs, and garbage outputs. The transistor level implementation of the proposed gates design by using Tanner tools.

Keywords – Reversible logic, garbage inputs, garbage outputs, gate count.

I. INTRODUCTION

Power dissipation is an important factor in VLSI design as modern logic circuits offer a great deal of computing power in a small footprint. The combinational logic circuits dissipate heat of KTln2 joules [1] for every bit of information erased during computation, where k = 1.3806505x10-23J/K is Boltzmann constant and T is the operating temperature in degrees at which the computation is carried out. Also, as Moore predicted that the number of transistors approximately doubles in every eighteen months and if this trend continues to hold, in the near future more and more energy will be lost due to the loss of information. Charles Bennett [2] showed that energy loss could be avoided or even eliminated if the computations are carried out in reversible logic and also proved that circuit built from reversible gates have zero power dissipation. Thus reversible logic appears to be promising in future low power design applications.
An efficient design in reversible logic should have the following features [3]: (a) use minimum number of reversible logic gates (b) should have less number of garbage outputs (c) less number of constant inputs and (d) minimization of quantum cost. Addition and multiplication operations are widely used arithmetic operations in many computations. High speed multiplier circuits are of particular interest in processor design.

Contribution: In this paper, we presented a reversible 4x4 multiplier with the design of new reversible gate called ABC Gate and GPS Gate. The proposed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, constant inputs and quantum cost, and this design can be generalized to construct reversible nxn multiplier

Organization: The paper is organized into the following sections. Section 2 is an overview of basic reversible gates. The background work is described in section 3. Section 4 is about new reversible gate and the proposed multiplier design, results and discussions of the proposed design is presented in section 5 and conclusions are contained in section 6.

II. BASIC REVERSIBLE GATES

Reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. A reversible circuit can be realized by using reversible gates only.

1. NOT Gate

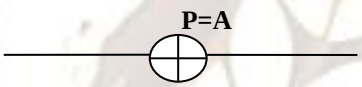


Fig 1: NOT gate

2. FEYNMAN Gate

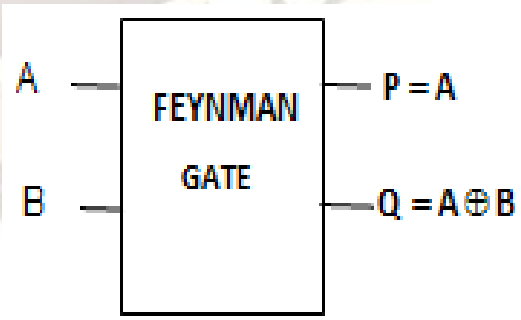


Fig 2: Feynman Gate

3 .FREDKIN GATE

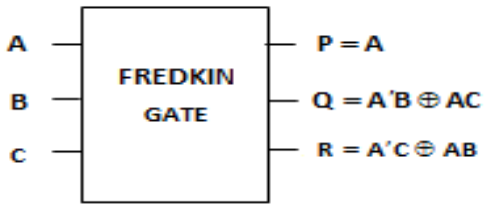


Fig 3: Fred kin Gate

4 .TOFFOLI GATE

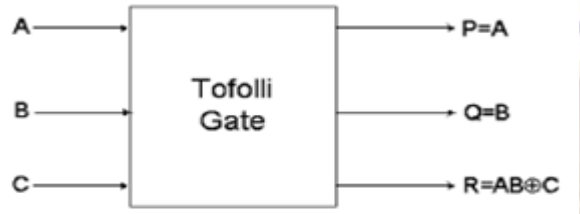


Fig 4:Toffole gate

5 PEERS GATE

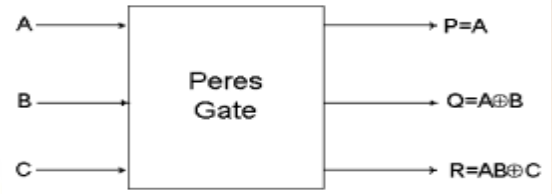


Fig 5: Peres Gate

6 .DOUBLE FEYNMAN GATE

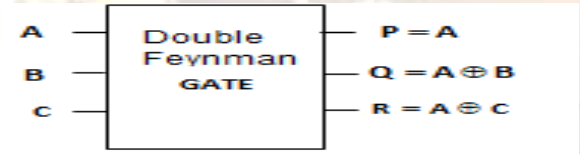


Fig 6: Double Feynman Gate

7 .TSG GATE

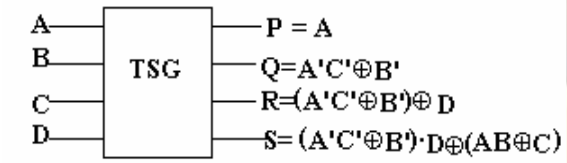


Fig 7: Reversible 4 X4 TSG Gate

III. GDI TECHINQUE

Gate-Diffusion-Input (GDI) method is based on the use of a simple cell as shown in figure .2. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences: 1) GDI cell contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). 2) Bulks of both NMOS and PMOS are connected to N or P respectively, so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS or SOI technologies .

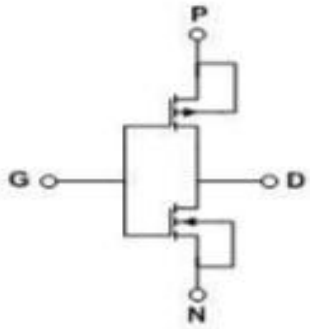


Fig 8:GDI Basic cell

Table I shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method.

Table I: Some logic functions that can be implemented with a single GDI cell

N	P	G	D
'0'	B	A	AB
B	'1'	A	A'+B
'1'	B	A	A+B
B	'0'	A	AB
C	B	A	A'B+AC
'0'	'1'	A	A'

IV. PROPOSED REVERSIBLE GATES

4.1(a) Proposed 3×3 Reversible ABC gate

The logic diagram of the proposed new Reversible ABC gate is as shown in the Fig. 9. The corresponding truth table is shown in Table 1. ABC Gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q= (A⊕B), R= A'C+B'C+ABC'.

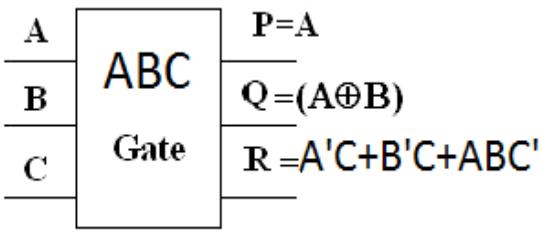


Fig 9: Proposed 3×3 reversible ABC gate

4.1(b) Implementation of ABC gate

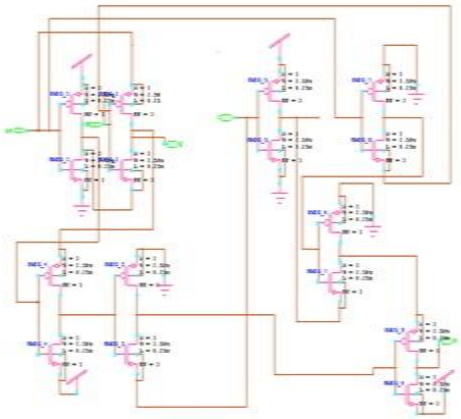


Fig 10: Transistor level implementation of ABC gate

4.2. Implementation of GPS gate

4.2(a) Proposed 4×4 Reversible GPS gate

The logic diagram of the proposed new Reversible GPS gate is as shown in the Fig. 11 The corresponding gate truth table is shown in Table 2. GPS Gate which is a 4*4 gate with inputs (A, B, C,D) and outputs P=B⊕C, Q=A, R= A⊕B⊕C⊕D, S=AB+BC+CA.

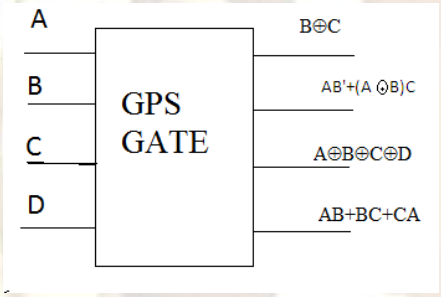


Fig 11: Proposed 3×3 Reversible GPS gate

4.2(b)Implementaion of GPS gate

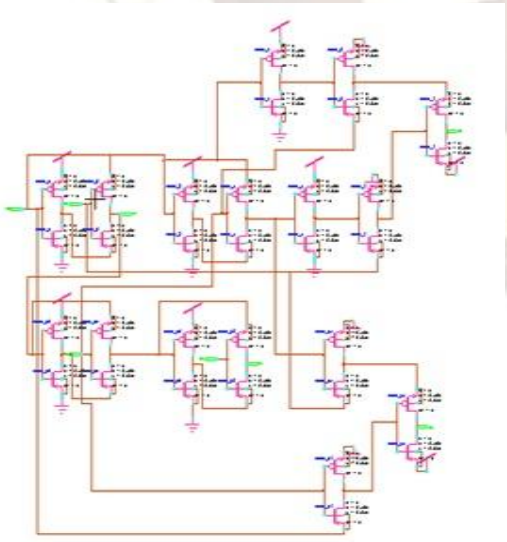
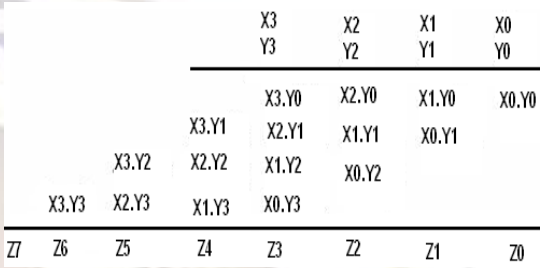


Fig 12: Transistor level implementation of GPS gate

V: PROPOSED REVERSIBLE MULTIPLIER DESIGN

A 4×4 Reversible multiplier has two parts..One is Partial Product term Generation (PPG) and other one is multi

Operand Addition circuit (MOA).The details of these two parts are following sections. The basic operation of 4×4 multiplier as shown in figure 13.It consist of sixteen partial products of the form Xi .Yi , where I vary between 0 and 3



F Fig 13: The basic operation of a 4×4 multiplier

5..1 Partial product term generation (PPG)

PPG circuit using Toffoli gate is as shown in figure 14.Here 16 Toffoli gates are used to generate sixteen Partial products as shown in figure 13.

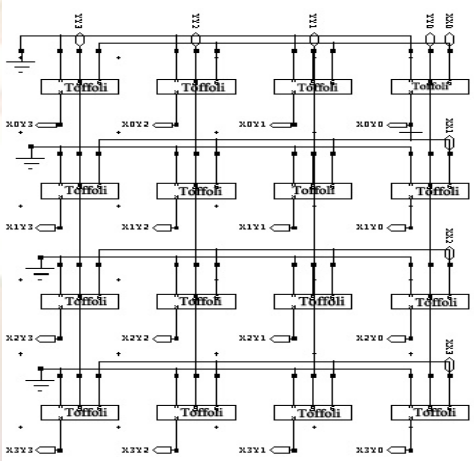


Fig 14: Partial product term generation circuit by using TG reversible gate

5.2 Multi Operand Addition circuit(MOA)

The addition of partial products using new proposed gates called ABC and GPS gates is as shown in figure 15.The basic cell for a such a multiplier is full adder using GPS gate with here inputs and one constant input, two garbage outputs and half adder using ABC gate with two inputs and one constant output, one garbage output. The proposed multiplier uses eight GPS gates and four ABC gates, Sixteen Toffolli gates for partial product terms generation.

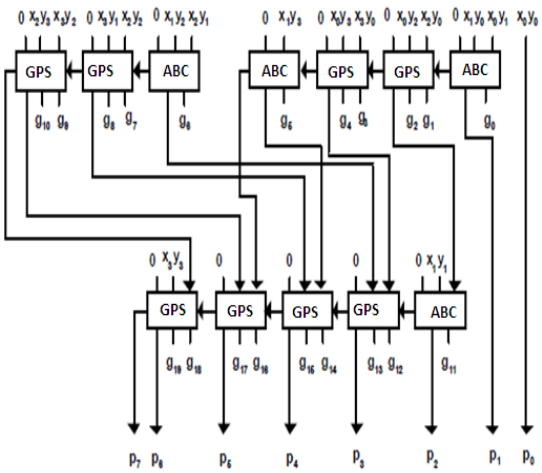


Fig15: Proposed 4×4 reversible multiplier

VI.RESULTS AND DISCUSSIONS

The simulation results of the multiplier as shown in figure 16 and figure 17.These two figures shows the voltage and power of the proposed reversible multiplier.

6.1 Simulation results of proposed Reversible multiplier

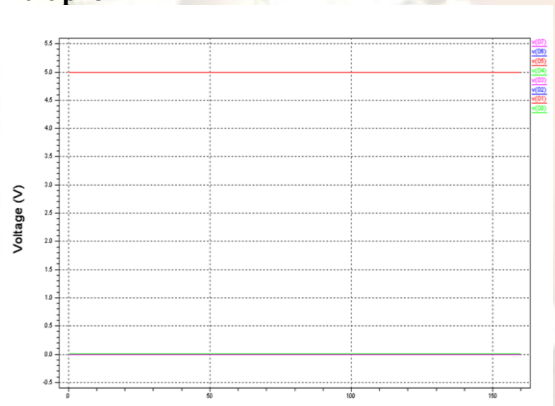


Fig: 16 Voltage wave form of proposed reversible Multiplier

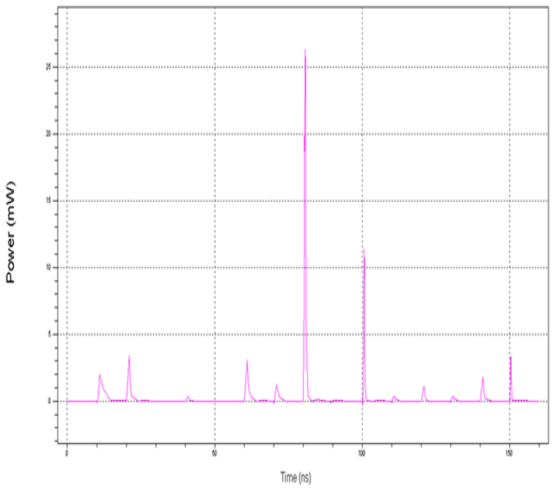


Fig 17: Output power waveform of proposed Reversible multiplier

6.2Comparison of CMOS and GDI techniques

In proposed reversible multiplier the output power is reduced up to 62.61% by using GDI technique when compared to CMOS and the transistor count is also reduced by using GDI technique when compared to CMOS. The transistor count reduced means the area of the circuit is reduced.

The comparison results as shown in table-2

TABLE-2 Comparison of CMOS and GDI

Parameter/ Technique	CMOS	GDI
Number of transistors	880	416
Power(µw)	115	43

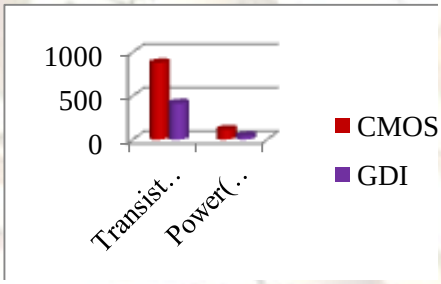


Fig 18: Comparison of CMOS and GDI techniques

6.3 Comparison of existing and proposed reversible multiplier circuits

Gate Count/Hardware Complexity: one of the major factors of a circuit is measured in terms of number of gates. It can be proved that the proposed circuit is better than the existing approaches in terms of hardware complexity. In [10], the total number of reversible gates required is 40, [11] requires 42, in [12] total number of gates required is 44 and in [13] number of gates required is32.Theproposed design requires 28 gates. Therefore, the proposed design is better than existing design approaches in terms gate count.

Garbage Inputs: Number of constant inputs is one of the main factors in designing a reversible logic circuit. The input is used as a control input by connecting to logic low or high to get function at the output is called garbage input. The proposed design require 16 garbage inputs, but the existing designs[10], [11] , [12] and[13] requires52 , 42,44 and 40 respectively. So it clearly shows that the proposed design is better than existing designs in terms of garbage inputs.

Garbage Outputs: the output of the reversible gate that is not used as a primary input or as input to the other gates is referred as garbage output. Optimizing garbage outputs is one of the other main constraints

in designing reversible logic logic circuit. The proposed reversible multiplier circuit produces 23 garbage outputs, but the design [10], [11],[12] and [13] produces 52, 49,52 and 40 respectively. Therefore, it is clear that proposed design is better that the existing designs in terms of number of garbage outputs.

Evaluation of the proposed reversible multiplier circuit:

The proposed reversible multiplier is more efficient compare to existing designs presented by [10], [11], [12] and [13].This can be comprehended easily with the comparison results as shown in table-3

TABLE-3 comparison of existing and proposed reversible multiplier circuit

Multiplier/ parameter	Gate count	Garbage inputs	Garbage outputs
[10]	40	52	52
[11]	42	42	49
[12]	44	44	52
[13]	32	40	40
proposed	28	16	23

Figure19 shows the difference between existing and proposed multiplier designs in terms of gate count, garbage inputs and garbage outputs. So it clearly shows the proposed reversible circuit is more efficient when compared to existing designs.

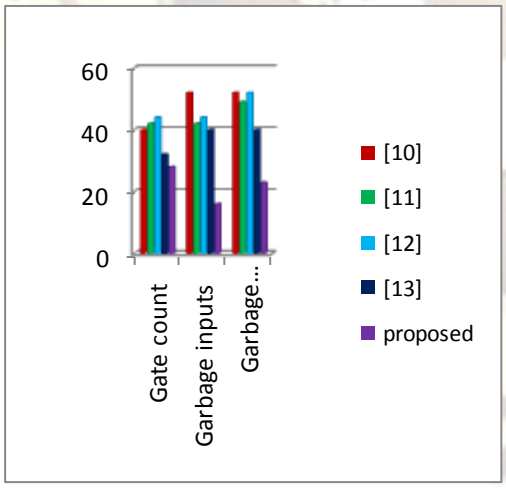


Fig 19 Comparison of existing and proposed reversible multiplier designs

VII CONCLUSIONS

In this paper the proposed 4×4 reversible multiplier is designed with two new proposed gates called ABC and GPS. These two gates are useful in design of multi operand circuit (MOA). The Toffolli gate(TG) is useful in partial product term generation circuit(PPG).The results clearly shows that the number of gates , number of garbage inputs and number of garbage outputs are less in proposed reversible multiplier circuit compared to existing design approaches. In this paper the proposed reversible multiplier designed by using GDI technique and compares the area and power of the multiplier with the CMOS technique. These results shows the GDI is the best low power technique when compare to CMOS technique.

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