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High-Power Applications CCM Boost Converter with Two Limb Topology Using Soft-Switching Techniques

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Abstract

This paper proposes a new double limb topology converter which doubles the input dc voltage suitable for high power applications. Switching losses is also considerably reduced by implementing soft switching techniques. The load current is shared by two branches and hence current stress across the switch is greatly reduced. The zero-voltage-transition (ZVT) pulse width modulation (PWM) converter achieves soft switching of the main switch and diode without increasing their voltage or current stresses.

Index Terms – Continuous Conduction mode (CCM), Zero Voltage switching (ZVS), Zero Current Switching (ZCS), Isolated

I. INTRODUCTION

Continuous-conduction-mode (CCM) boost converters have been widely used as the front-end converter for active input current shaping. In recent years, CCM boost converters are increasingly needed in high power applications such as hybrid electric vehicles and fuel cell power conversion systems. High power density and high efficiency are major concerns in high-power CCM boost converters. The hard-switched CCM boost converter suffers from severe diode reverse-recovery problem in high current high-power applications. That is when the main switch is turned on a shoot through of the output capacitor to ground due to the diode reverse recovery causes a large current spike through the diode and main switch. This not only incurs significant turn-off loss of the diode and turn-on loss of the main switch, but also causes severe electromagnetic interference (EMI) emission. Therefore, the hard-switched CCM boost converter is not capable to achieve high efficiency and high power density at high power level. Many soft-switching techniques on CCM boost converters have been proposed. The zero-voltage switched (ZVS) quasi resonant converter (QRC) and the ZVS quasi square-wave converter (QSW) technique offers ZVS turn-on of the main switch. However, both main switch and diode suffer from a high current stress and voltage stress resulting in significant conduction losses on the above two methods. Hence zero-voltage-transition (ZVT) pulse width modulation (PWM) converter achieves soft switching of the main switch and diode without increasing their voltage or current stresses, since ZVS is achieved by partial resonance of the shunt branch across the main switch. Furthermore, the reverse recovery-related problem is alleviated by controlling diode current decrease rate *di*/*dt* during its turn off. However, severe undesired resonance may occur in the shunt branch. Adding a rectifier and saturable inductor can mitigate the resonance, but this causes circuit complexity an d additional cost Due to soft switching technique the proposed converter has numerous advantages compared to that of conventional converter. The proposed converter has the following advantages:

1. Voltage and power conversion ratio is almost doubled compared to the conventional boost converter.
2. The load current is shared by two branches and hence current stress across the switch is greatly reduced.
3. ZVS turn-on of the main switches in CCM and ZCS turn-off of diodes.
4. Negligible diode reverse recovery due to ZCS turn-off of the diode
5. Significantly reduced components voltage ratings and energy volumes of most passive components.

II. PROPOSED CONVERTER

The proposed converter has two limb connected in parallel to increase the output power. This is achieved by two diode limb where the load current is combined together which will drive the load.

GENERAL ARCHITECTURE

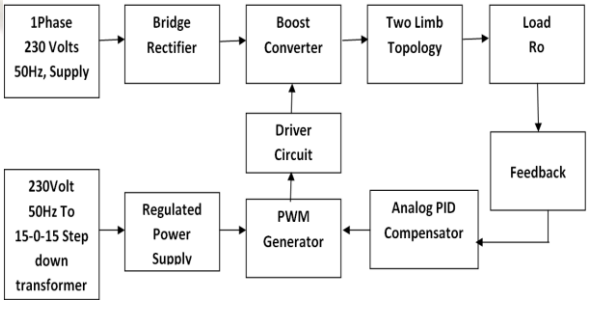

Fig.1. Architecture

ARCHITECTURE DESCRIPTION

Fig.1 shows the Architecture of the proposed converter. The single phase AC supply is converted into DC supply and applied to boost converter. Due to two limb topology the output power is greatly increased compared to that of conventional converter. The switch is controlled by means of PWM technique. Hence controlled DC voltage is applied to the DC Load.

III CIRCUIT DIAGRAM

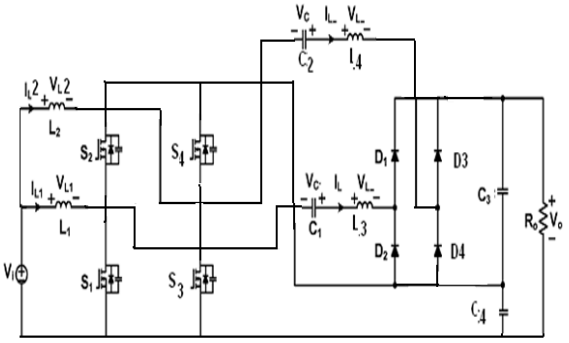

Fig.2. Circuit diagram

Fig.2. shows the Circuit diagram of proposed converter. The upper switch S2 and S4 in the proposed converter replaces the rectifier diode in the conventional boost converter. The switches S1, S3 and S2, S4 are operated asymmetrically to produce regulated output voltage. The auxiliary circuit consists of inductors L3, L4 and capacitors C1, C2 to produce high output voltage and to achieve ZVS of active switches in CCM technique.

A. OPERATING PRINCIPLE

The operation of proposed converter can be easily understood by five modes of operation.

Mode 1:

This mode begins when iL3 and iL4 decreases to zero and D2,D4 is turned on as shown in Fig. 3. During this mode, the lower switch S1 and S3 maintains ON state. Both input inductor current *iL*1,iL 2 and auxiliary inductor current *iL*3,iL4 flows through lower switch S1 and S2 respectively. The slope of these currents are given by

$$\frac{diL1}{dt} = \frac{Vi}{L1}$$
$$\frac{diL2}{dt} = \frac{Vi}{L2}$$

Similarly,

$$\frac{diL3}{dt} = \frac{Vc1 - Vc3}{L3}$$
$$\frac{diL4}{dt} = \frac{Vc2 - Vc3}{L4}$$

Mode 2:

This mode begins when S1, S3 is turned off and the body diode of S2, S4 is turned on. The gating signal for S2 & S4 is applied during this mode, and S2, S4 is turned on under ZVS conditions. Both iL1,iL3 and iL2, iL4 are decreasing with the slope determined by the following equations:

$$\frac{diL1}{dt} = \frac{Vi - Vc3}{L1}$$
$$\frac{diL2}{dt} = \frac{Vi - Vc3}{L2}$$

Similarly,

At the end of this mode, inductor current iL3,iL4 changes its direction of flow and D1,D3 starts to conduct. It should be noted that D2 and D4 is turned off under ZCS.

$$\frac{diL3}{dt} = \frac{Vc1}{L3}$$
$$\frac{diL4}{dt} = \frac{Vc2}{L4}$$

Mode 3:

During this mode iL1, iL2 keeps decreasing with the slope determined in Mode 2, and iL3, iL4 increases with slope.

$$\frac{diL3}{dt} = \frac{Vc1 - Vc4}{L3}$$
$$\frac{diL4}{dt} = \frac{Vc2 - Vc4}{L4}$$

At the end of this mode, switch current iS2, iS4 reverses its direction of flow and conducts the main channel of S2 and S4.

Mode 4:

During this mode, inductor current iL1, iL2 and iL3, iL4 keep flowing with the same slope determined in Mode 3.

Mode 5:

This mode begins when lower switches S2 and S4 are turned off and the body diode of S1and S3 is turned on. The gating signal for S1, S3 is applied during this mode, and S1 and S3 could be turned on under ZVS conditions. Inductor currents iL1, iL3 and iL2, iL4 start to increase and decrease, respectively, with the slope determined by the following equation. This state ends when the decreasing current iL3, iL4 reaches to 0V. This is the end of one complete cycle. Note that diode D1 and D3 is also turned off under ZCS.

$$\frac{diL1}{dt} = \frac{Vi}{L1} \qquad \frac{diL3}{dt} = \frac{Vc1 - Vc3 - Vc4}{L3}$$
$$\frac{diL2}{dt} = \frac{Vi}{L2} \qquad \frac{diL4}{dt} = \frac{Vc2 - Vc3 - Vc4}{L4}$$

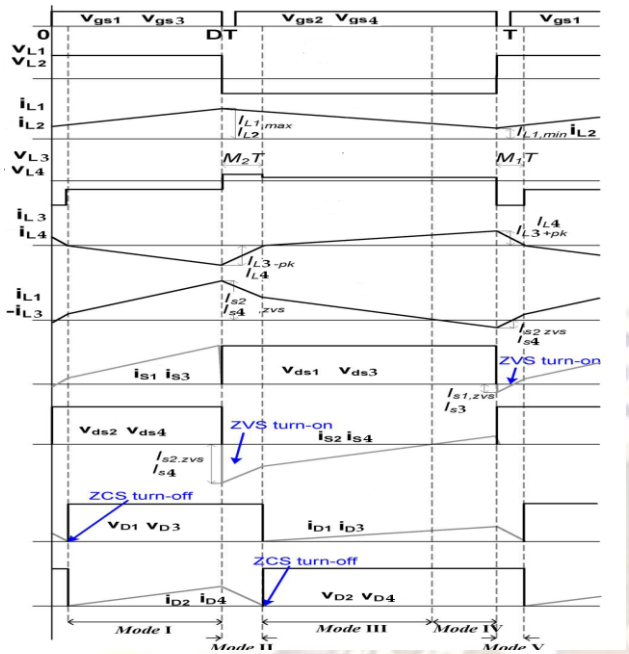

Fig.3. Key waveforms of the proposed converter

B. VOLTAGE CONVERSION RATIO

To obtain the voltage gain of the proposed converter, it is assumed that the voltage across *C*1, *C*2, and *C*3 are constant during the switching period of *TS*. The output voltage is given by

VO = VC2 + VC3

Where the effective duty Deff is defined

Deff = D +M1 −M2. $V_o = \frac{2}{1 - D_{\text{eff}}} V_i$

The output voltage can also be expressed

$$V_o = \frac{2}{1 - D} V_i - \Delta V$$

Where ΔV is the voltage drop caused by the duty loss (M2–M1). The voltage drop ΔV can be obtained by

$$\Delta V = \frac{2V_i(M_2 - M_1)}{(1 - D)(1 - D + M_2 - M_1)}.$$

According to volt-sec balance principle on L2, capacitor voltage VC1 can be obtained

VC1 = VC2 (1 − D − (M2 −M1) + DVC3

Where VC2 and VC3 can be expressed as

$$V_{C_3} = \frac{1}{1 - D} V_i$$

$$V_{C_2} = \frac{1}{1 - D} V_i - \Delta V.$$

In the steady state, the average output load current equals the average current of D1 and D2 since the average value of the current through L2 (C2) is zero. The following equations can be derived:

$$I_{D_1,\text{av}} = \frac{V_o}{R_o} = \frac{1}{2}(1 - D - (M_2 - M_1))I_{L_2,+\text{pk}}$$

$$I_{D_2,\text{av}} = \frac{V_o}{R_o} = \frac{1}{2}(D + M_2 - M_1)I_{L_2,-\text{pk}}$$

where IL2 ,+pk and IL2 ,−pk are positive and negative peak values of the inductor current IL2 , and are given by

$$I_{L_2,+\text{pk}} = \frac{(V_{C_1} - V_{C_2} - V_{C_3})M_1 T_S}{L_2}$$

$$I_{L_2,-\text{pk}} = \frac{V_{C_1} M_2 T_S}{L_2}.$$

Diode current ID2, and ID4, which is a negative portion of current IL3 and IL4, becomes incremental current in switch S1 and S3, resulting in increased conduction loss. At the same time, diode current ID1, ID3, which is a positive portion of current IL3 and IL4, becomes decremental current in switch S2 and S4, resulting in decreased conduction loss.

Also, current IL3 and IL4 increases the ZVS currents for both lower switch, IS1 and IS3 ZVS, and upper switch, IS2 and IS4 ZVS, resulting in reduced switching losses. The peak values IL3, IL4 −pk and IL3, IL4 +pk can be adjusted by the inductance L3 AND L4 . Therefore, the magnitude of current IL3 and IL4 should be properly designed considering this tradeoff relation. Duty loss *(M2−M1)* can be reduced by choosing smaller inductance of *L*3 and L4, but this reduces ZVS range of main switch S1 and S3. Therefore, inductance *L*3 and L4 should be properly chosen, considering a tradeoff of switching loss and voltage gain.

We know that power in DC is nothing but product of current and voltage.

Po = Vo *Io

Hence Power is almost increased compared to basic converter.

C. ZVS CHARACTERISTIC FOR MAIN SWITCH

ZVS of the upper and lower switches depends on the difference of the filter inductor current and auxiliary inductor current. The ZVS current for lower switch IS1 and IS4, ZVS is the positive peak of iL1 –iL3 when the upper switch is turned off and can be expressed as

$$I_{S_1,\mathrm{ZVS}} = I_{L_2,+\mathrm{pk}} - I_{L_1,\min}$$
$$= \frac{(V_{C_1} - V_{C_2} - V_{C_3})M_1 T_s}{L_2} - \left(\frac{V_o^2}{V_i R_o} + \frac{DV_i}{2L_1 f_s}\right).$$

The ZVS current for upper switch IS2 and IS4, ZVS is the negative peak of iL1 –IL3 when the lower switch is turned off and can be expressed as

$$I_{S_2,\mathrm{ZVS}} = |I_{L_2,-\mathrm{pk}}| + I_{L_1,\max}$$
$$= \frac{V_{C_1} M_2 T_s}{L_2} + \left(\frac{V_o^2}{V_i R_o} + \frac{DV_i}{2L_1 f_s}\right).$$

To ensure the ZVS turn-on of upper switch S2 and S4, the following condition should be satisfied

$$\frac{1}{2}(L_1 I_{L_1,\max}^2 + L_2 I_{L_2,-\mathrm{pk}}^2) > \frac{1}{2}(C_{os1} + C_{os2})\left(\frac{V_i}{1-D}\right)^2$$

Where Cos1 and Cos2 are the output capacitances of lower switch S1, S3 and upper switch S2, S4 respectively. In fact, the condition of can be easily satisfied, and ZVS of upper switch S2 can be achieved over the whole load range. To ensure the ZVS turn-on of lower switch S1 and S3,

$$\frac{1}{2}(L_2 I_{L_2,+\mathrm{pk}}^2 - L_1 I_{L_1,\min}^2) > \frac{1}{2}(C_{os1} + C_{os2})\left(\frac{V_i}{1-D}\right)^2.$$

the following condition should be satisfied.

D. COMPARISON OF COMPONENT RATINGS

In order to perform a comparison of the proposed converter to the conventional ZVT converter in terms of the component rating, the converters have been simulated according to the following specifications:

1) Po = 1.1kW
2) Vi = 80 V
1) Po = 1.1kW
2) Vi = 80 V
3) Vo = 350 V
4) ΔIi = 10%
5) ΔVo = 3%
6) Fs=15 kHz

The component ratings of the proposed converter and the ZVT converter calculated according to the design specification. Because of the proposed connection of the auxiliary circuit, the voltage ratings of all components of the proposed converter are much smaller compared to those of the ZVT converter that are the same as the output voltage. Therefore, the switch and diode utilizations of the proposed converter are greatly improved.

SIMULATION CIRCUIT

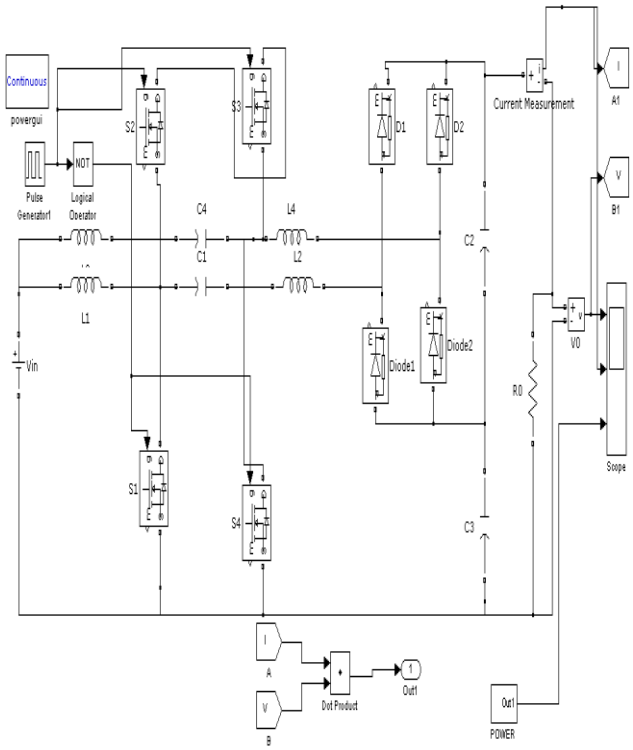

Fig:4 Simulation circuit

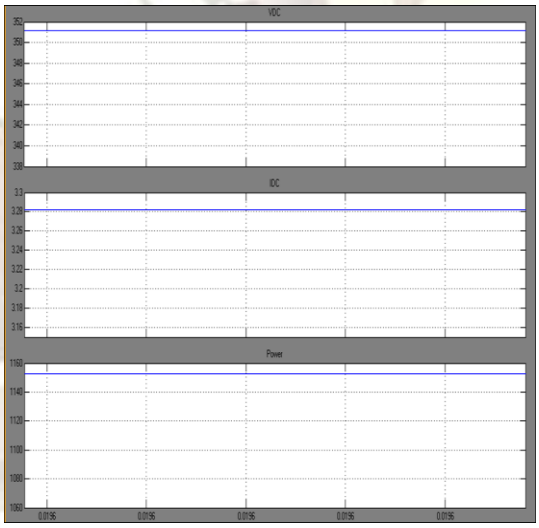

Fig: 5 Outputs: 1.voltage 2. Current 3.power

IV. CONCLUSION

In this paper, a new double limb topology boost converter suitable for high power application has been proposed. In this converter the Voltage and power conversion ratio is almost doubled compared to the conventional boost converter. The load current is shared by two branches and hence current stress across the switch is greatly reduced.

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