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# Design Of 3 bit synchronous Counter using DLDFF

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## ABSTRACT

**Flip flops are the fundamental building blocks for all sequential circuits. Data transition look ahead D flip flop consumes less power than the conventional D Flip flop. The power consumption of CMOS LSI's is a very important issue these days. Here we propose a modified data transition D flip flop which consumes less power than existing data transition D flip flop. The total power reduction of proposed data transition D flip flop is 18.37% when compared with existing data transition D flip flop. We design a 3 bit synchronous counter which consumes less power than existing data transition look ahead D flip flop and D flip flop.**

**Keywords -** DLDFF, Low power, Synchronous counter, Switching activity.

## I. INTRODUCTION

The power consumption of CMOS LSI's is a very important issue these days. For instance, the demand for portable devices is currently increasing, and LSI's for these device require low power because they run on batteries. Therefore, much work is focused on low-power designs for LSI's. Switching power is reduced in the combinational logic between flip flops. D-Flip- flop and latches are a fundamental buildings block of digital electronics system used in computer, communication and many other types of system. Flip –flop and latches are used as data storage elements .such data storage can be used for storage of state, and such a circuit is described as sequential logic. Flip-flops are the fundamental buildings blocks for all sequential circuits. Flip-flops, have their content change only either at rising or falling edge of the enable signal. But after the rising or falling edge of enable signal, the flip-flop's content remain constant even if the input changes.[2]

In synchronous systems, flip-flop are the starting and ending points of signal delay paths, which decide the maximum speed of system. Typically the consume a large amount of power because they are clocked at the system operating [1] frequency. Here the DLDFF is coming under low power internal clock gating flip flop, Low power flip flop using internal clock gating is that new technique of flip flop family uses an internal predictive circuit for turning off the internal clock when the input and stored data are equal. The internal clock gating technique is appropriate for flip flops with low switching rate in the input data.

Flip flop usually find application in counters and shift registers. A counter is essentially a register that goes through a predetermined sequence of binary states .A register that goes through a prescribed sequence of states upon the application of input pulses is called a counter. The input pulses may be clock pulses, or they may originate from some external source and may occur at a fixed interval of time or at random. The sequence of states may follow the binary number sequence or any other sequence of states. An n-bit binary counter consists of n flip-flops and can count in binary from 0 through $2^n$-1..

Counter are available in two categories: asynchronous and synchronous counters. In an asynchronous counter, a flip flop output transition serves as a source for triggering other flip flop. In other words, the clock input of some or all flip flops are triggered, not by the common clock pulses, but rather by the transition that occurs in other flip-flops outputs In synchronous counter, the clock inputs of all flip flops receive the common clock. Here in this design we proposed a data transition look ahead flip flop which consumes less power and less area than the existing DLDFF. Then a 3 bit synchronous counter is going to design with both existing and proposed flip flop. The proposed and conventional designs are simulated and analysed in Hspice at (130 This paper is organized as follows: Section II Low power flip flop with internal clock gating . Section III describes about the synchronous counters. Section IV summarizes the results and comparisons. Section V concludes the paper.

## II.LOW POWER FLIP FLOP WITH INTERNAL CLOCK GATING

Low power flip flop using internal clock gating is that new technique of flip flop family uses an internal predictive circuit for turning off the internal clock when the input and stored data are equal. The internal clock gating technique is appropriate for flip flops with low switching rate in the input data. Here this transmission gate master slave flip flop, the part of clock energy of flip flop is consumed by the internal clock buffer to control the transmission gates. If the input of the flip flop is identical to its output, the switching of its clock signal can be suppressed to conserve power. Here

clock signal always flows into the Dflip flop irrespective of whether the input changes or not.

One type of internal clock gating flip flop is the Data transition look ahead flip flop is DL-Dff ,in this flip flop the gating function is derived within the flip flop without any external control signal, the external clock signal of the flip flop still switches. But, the clock signal flowing into the flip flop is deactivated when there are no data transition.[3].

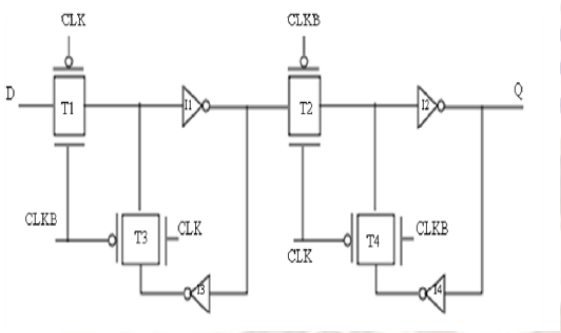


Fig :1: Transmission gate master-slave flip flop.

when compared to the ordinary flip flop this type of internal clock gating flip flop stops the unwanted switching activities in the clock signals and it save power consumption.

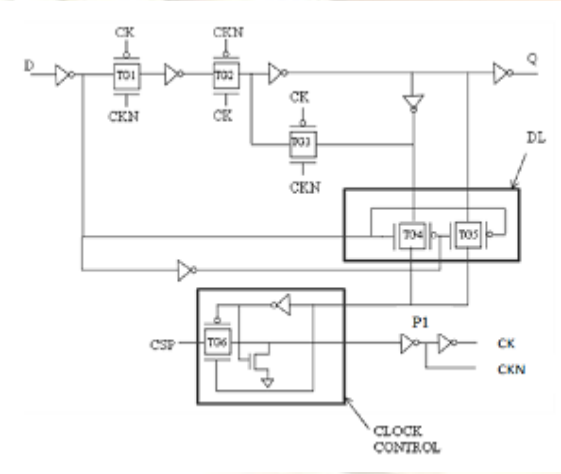


Fig: 2: Existing data transition look ahead flip-flop

The basic concept is that the clock signal is deactivated when there are no data transitions. Therefore, a DL-DFF consumes less power when compared with other ordinary flip flops. In Fig. 2 is a circuit diagram of a DL-DFF. The sub nano second pulse generator is used as a local clock driver. A DL-DFFhas three main features. First, the data-transition look-ahead(DL) circuit compares the input data with the hold data. Second, the clock control circuit cuts off the clock when the input and hold data are the same. And third, the dynamic circuit can be used as a master latch because data are held in the master latch for less than a nanosecond. The dynamic circuit also helps to further reduce the power consumption. The DL-DFF requires seven

more transistors than the convention alone. However, small transistors can be used as the additional ones because they drive only internal nodes of the DL-DFF.

The proposed Data transition look ahead flip flop , here in existing data transition look ahead flip flop the transmission gate is replaced by the NMOS pass transistor, because in transmission gate no threshold loss but in pass transistor threshold loss will be there ,but pass transistor is followed by inverter means it will produce exact logic without any threshold loss. In order to reduce power and less area we replaced the transmission gate in to pass transistor. When compare to the existing DLDFF the proposed DLDFF consumes less power and less area.

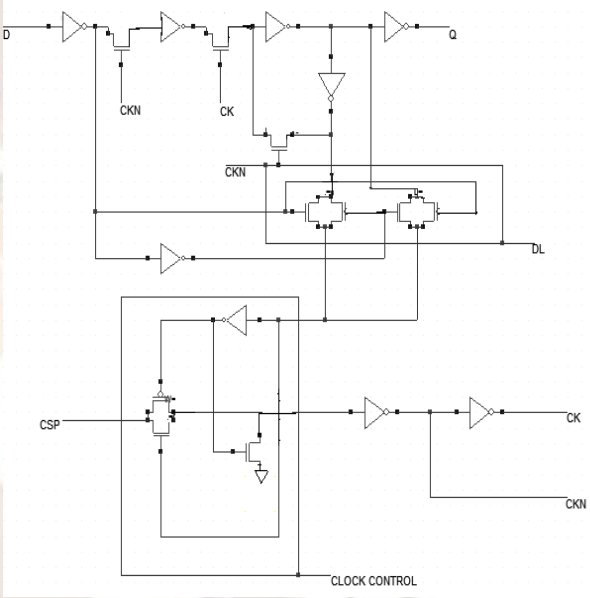


Fig 3 Proposed data transition look ahead flip flop.

***Operation:*** Data transition look ahead D flip flop. The transmission gates TG4 and TG5 (DL) do the data transition look ahead. It compares the hold data at the output with the respective input data and enables the flip flop to write the data, accordingly. The DL block act as an XNOR gate. For example, when D = Q = 1, the clock is inactive and transmission of data is not required. But, when D = 1, Q = 0, the clock is enabled and data gets transmitted. **T**he Clock control block consists of the transmission gate TG6 followed by an NMOS transistor. The clock control signal depends on the DL's output .The input to the clock control is given by the external clock CSP and divides into CK and CKN. since pass transistor has not having exact output level, but it is followed by an inverter it will make exact logic level in the output level, so the operation of the flip flop doesn't change and further one advantage is that power is also reduced by using

pass transistor. . When an input datum D is the same as the hold datum Q the DL circuit makes P1 low.

This turns the transmission gate in the clock control circuit off. as a result, CK and CKN do not transit. CK and CKN transit only when D and Q are different when D changes to a value different from q,P1 first change to high. Next, when CKI rises, CK also rises and Q change.then,P1 change back to low because D and Q are the same again. This immediately makes CK low.

## III. COUNTER DESIGN

A counter is a circuit that produces a set of unique output combinations corresponding to the number of applied input pulses. The number of unique outputs of a counter is known as its mod number or modulus. High-frequency operations require that all the FFs of a synchronous counter be triggered at the same time to prevent errors. We use a Synchronous counter for this type of operation. The synchronous counter is similar to a ripple counter with two exceptions: The clock pulses are applied to each FF, and additional gates are added to ensure that the FFs toggle in the proper sequence. The advantage of synchronous counter over asynchronous counter is that, Since all inputs are synchronized with a common clock, no interrupts can occur in the middle of a state transition in synchronous counters, all flip-flops change simultaneously and in asynchronous counters, the propagation delay of the flip-flops add up to produce the overall delay.

3 bit synchronous counter having a common clock to all the flip flop Generally counter bits are evaluated at every clock cycle and captured by associated flip flops at every triggering edge of the clock. because the switching activity of counter bits in a binary counter is decreased by half as the significance of each bit increase, this type of operation apparently causes a lot of redundant transition, particularly for counter bits having higher significance. Here in this synchronous counter both conventional D flip flop and data transition look ahead D flip flop were used to generate the binary sequence from “000” to “111” because it will count up to seven bit for every clock signal. But the clock signal flows continuously in the D flip flop independent of the data transition, the increase in the load capacitance results in increase in the power consumption relatively more in D flip flop compare to the data transition look ahead D flip flop. And this Data transition look ahead D flip flop used to minimize the overall power consumption of counters by attempting to eliminate redundant transition in flip flops.The design procedure for synchronous counters is same as that Sequential circuits. Synchronous counter have a regular pattern and can be constructed with complementing flip flops and gates.

So here in this work synchronous counter is more suitable for this type of flip flop because the

flip flops of synchronous counter are monitored by a global clock. Since asynchronous counter uses the clock signal only to the first stage of flip flop and the preceding stage uses the output of the previous stages of the clock stages. so the data transition look ahead flip flop cannot be efficiently implemented in asynchronous counter. The design procedure for synchronous counters is same as that Sequential circuit. Synchronous counter have a regular pattern and can be constructed with complementing flip flops and gates.

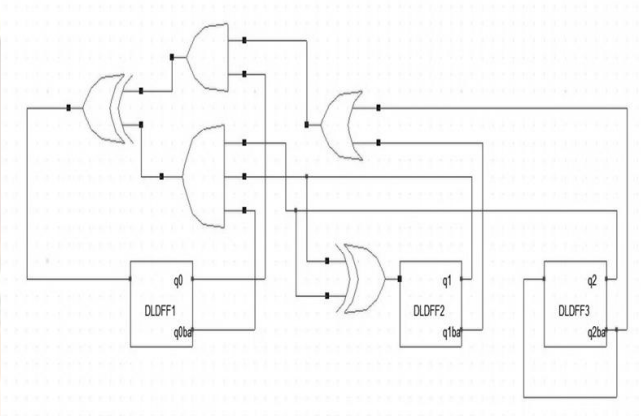


Fig: 4: 3 bit synchronous counter using existing DLDFF

Table1: Counting sequence of 3 bit synchronous counter

| Clock cycle | $Q_0$ | $Q_1$ | $Q_2$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |

The counters are designed by the proposed data transition look ahead flip flop which consumes low power and less area, than the existing counters using data transition look ahead flip flop. Generally synchronous counter bits are evaluated at every clock cycle and captured by associated flip flops at every triggering edge of the clock. Because the switching activity of counter bits in a binary counter is decreased by half as the significance of each bit

increase, this type of operation apparently causes a lot of redundant transition, particularly for counter

bits having higher significance. This 3 bit synchronous counter used to generate the binary sequence from "000" to "111" because it will count up to seven bit for every clock signal. The design procedure is same as that of existing counters using conventional data transition look ahead flip flop.

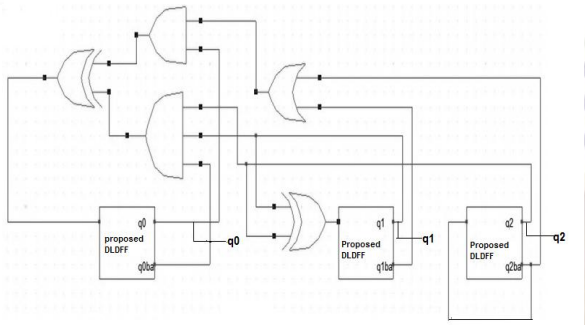


**Fig: 5: 3 bit synchronous counter using proposed DLDFF**

## IV. RESULTS AND COMPARISON

The simulation is done by HSPICE and the output waveform for the existing counter and proposed counter is given below.

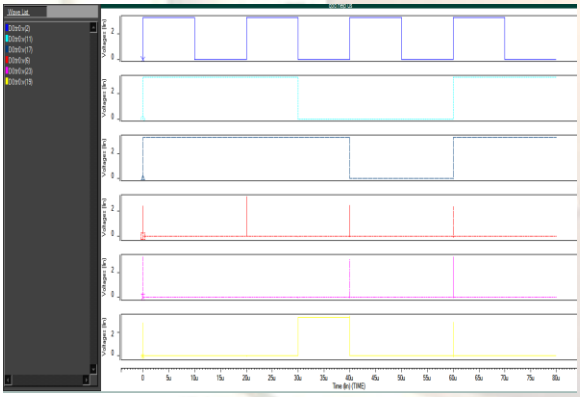

Fig.6. Output waveform of existing DLDFF.

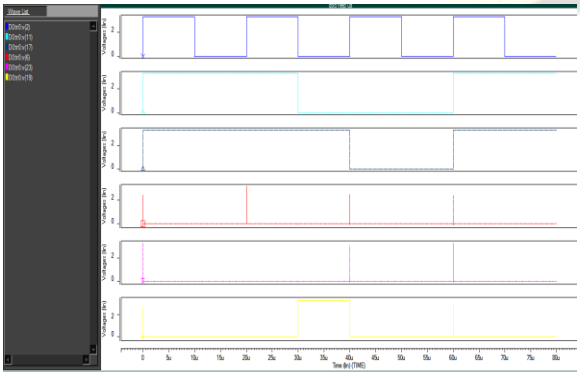

Fig.7. Output waveform of proposed DLDFF .

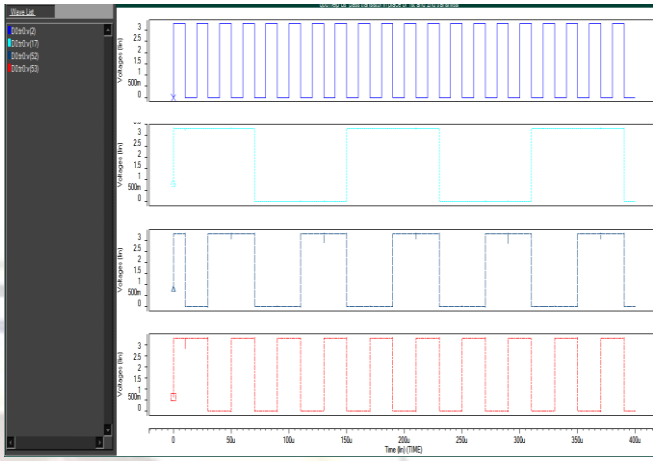

Fig.8. Output waveform of existing 3 bit synchronous counter.

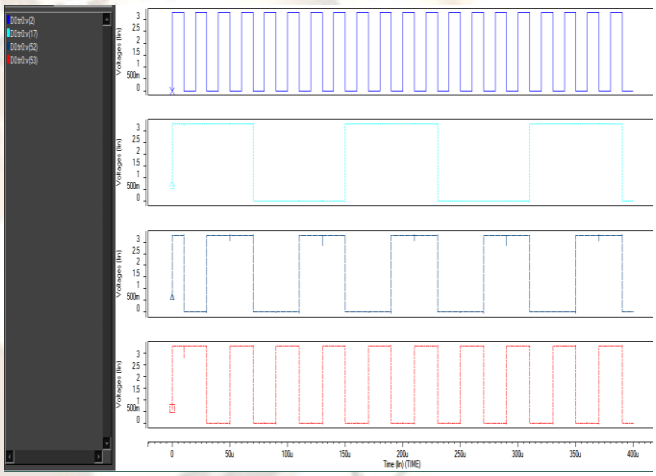

Fig.9. Output waveform of proposed 3 bit synchronous counter.

The power comparison is made between these flip flops and counters .the proposed flip flop and counter which consumes low power when compared with conventional flip flop and counter.

Table.2 Power and transistor comparisons of flip flops

| Flip flop | No of transistors | Power consumption(uw) |
|---|---|---|
| Existing DLDFF | 50 | 2.814E-07 |

| | | |
|---|---|---|
| Proposed DLDFF | 46 | 2.297E-07 |

Table.3. Power and transistor comparisons of counters

| Counters | Power consumption(uw) |
|---|---|
| Existing 3 bit synchronous counter | 9.014E-07 |
| Proposed 3 bit synchronous counter | 8.961E-07 |

## V. CONCLUSION

In this paper we have proposed Data transition look ahead DFF using which the 3 bit synchronous counter has been designed and simulated in 130nm CMOS technology with HSPICE tool. From the comparison table it is clear that the proposed design has less power consumption in terms of power.

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