Rajeev Kumar, Mandeep Singh Saini / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 3, May-Jun 2012, pp. 174- 178 Design of 64 bit Integer Multiplier for Low Power Consumption

Rajeev Kumar¹, Mandeep Singh Saini²

¹Assistant Professor, Deptt of ECE IITT College, Pojewal, Punjab ²Assistant Professor, Deptt of ECE, IITT College ,Pojewal, Punjab

Introduction

In mathematical calculations multiplication is an important operation. Multiplication is done using Multiplier. In scientific calculations large bit width are required. In the previous architectures 32 bit multipliers are designed using Hardware Description Languages. So as the bit width increases to perform long calculations, the requirement of hardware should be more. In the hardware each gate consumes power. So in this particular multiplier our aim is to reduce the power consumption of the multiplier chip. Here we present the design of a 64 bit Integer Multiplier that generates 128 bit output. This multiplier is designed using Verilog HDL.

Experimental Work

All the specifications are written first. Then they are converted in RTL using Verilog HDL.It contains two 64 bit inputs namely a and b and c is the 128 bit output. Here clk is the clock input which is taken as negative edge for fast triggering.

Here cs is the chip select signal. If cs is high then chip is disabled and no multiplication is done .On the other hand if cs signal is low then multiplication is done. Functionality is verified using simulation on Active HDL 7.2.



Architecture Design for 64 bit Multiplier

After simulation is over the gate level netlist is generated using Xilinx ISE 9.2i. After synthesis the design is technology specific. Finally all the necessary parameters obtained from the synthesis are given in the table.

Experimental Results Simulation Result



Device Utilization Report

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Devic	e utilization s	ummary:						
Selec	ted Device : 2s	200fg45	6-6					
Numb	er of Slices:			21	83	out of	2352	92%
Numb	er of 4 input L	UTs:		43	48	out of	4704	92%
Numb	er of IOs:			2	58			
Numb	er of bonded IO	Bs:		2	58	out of	284	90%
I	OB Flip Flops:			1	92			
Numb	er of GCLKs:				1	out of	4	25%
		2	Delav I	2enor	t	-		
Tim:	ing Summary:		belay I	серот	·		1996 - C	
k								
Spee	ed Grade: -6							
1	Minimum perio	d: No	path :	found				
1	Minimum input	; arriv	val tin	me be	foi	re cloc	k: 26.2	244ns
1	Maximum outpu	it requ	lired	time	aft	ter clo	ck: 12	.381ns
1	Maximum combi	nation	nal par	th de	la	y: No p	ath fou	ind
Tim	ing Detail:							
	ing Decail.							
A11	values displ	layed i	in nan	oseco	nds	s (ns)		
		-						
	Data Path: Mtrien	c to c<99	>					
		-	Gate	Net				
	Cell.in-Nout	fanout	Delay	Delay	Log	rical Name	(Net Name)	
1.4		Lanout		летаў	шоў	ICal Name	(Net Name)	
	FD 1:C->Q	1	1,085	1.035	Mtr	ien c (Mtri	ien c)	
	BUF: I->0	65	0.549	4,905	Mtr	ien c 1 (Mt	rien c 1)	
	OBUFT:T->0		4.807		c 9	OBUFT (CK) >	
	Total		12.381ns	(6.441	ns l	.ogic, 5.940)ns route)	
				(52.0%	100	ric. 48.0% 1	route)	1

CPU : 49.67 / 49.97 s | Elapsed : 49.00 / 50.00 s



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Technology Schematic



Power Report

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Design:		alu.ncd				
Preferences	:	alu.pcf				
Part:		2s200fg456-6				
Data version	n:	PRELIMINARY, v1.0,	07-31-	-02		

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		7
Vccint 2.50V:	0	0
Vcco33 3.30V:	2	7
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vcco33 3.30V:	2	7
Thermal summary:		
Estimated junction temperature: Ambient temp: 25C		25C
Case temp: 250		

Theta J-A range: 27 - 22C/W

Post Layout Simulation Report

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Component Spartan-II

********	*********	********	**********	*******	*******	****
Component]	Spartan2					
Manufacturer]	Xilinx Ind	s.				
Package]						
For Package T	ype fg456					
variable	typ	min	max			
pkg	161.00m	117.00m	205.00m			
pkg	4.1500nH	1.9000nH	6.4000nH			
pkg	1.1500pF	0.7000pF	1.6000pF			
-						

Chip Floor Plan: SPARTAN2 FPGA



Chip Design

Xilinx FPGA Editor - aluncd

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Rajeev Kumar, Mandeep Singh Saini / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 3, May-Jun 2012, pp. 174- 178 Experimental Results & Discussion

	Experimental Results & Discussio
Gate Delay	12.381ns
Net Delay	6.441ns
Clock Fanout	161
Power Consumption	7mW
Gate Count	56,644
Additional JTAG Gate Count	12,384
Setup Time	26.244ns
Hold Time	12.381ns
Technology	0.18um CMOS
Bonded IO	258
. 01	ILPA

Finally the synthesis is done on SPARTAN2 FPGA using package 2s200fg456 with speed grade -6. This chip provides the low power consumption that is the prime requirement of today technology. In future the multiplier can be designed for high speed with minimum hardware.

Comparison									
Parameters	SPARTAN2	SPARTAN2e							
Gate Delay	12.381ns	26.851ns							
Net Delay	6.441ns	18.151ns							
Clock Fanout	161	161							
Power Consumption	7mW	34mW							
Gate Count	56,644	56,644							
Additional JTAG Gate	12,384	12,384							
Count	15- 66	Cable							
Setup Time	26.244ns	26.851ns							
Hold Time	12.381ns	11.330ns							
Bonded IO	258 257								

So from the above table it is clear that the delay (gate delay & net delay) as well as the power consumption is less in SPARTAN 2 FPGA.

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