Design of Low-Leakage CNTFET SRAM Cell at 32nm Technology using Forced Stack Technique

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ABSTRACT

As silicon semiconductor device feature size scales down to the nanometer range, planar bulk CMOS design and fabrication encounter significant challenges nowadays. Carbon Nanotube Field Effect Transistor (CNTFET) has been introduced for high stability, high performance and low power SRAM cell design as an alternative material. Technology scaling demands a decrease in both V_{DD} and V_T to sustain historical delay reduction, while restraining active power dissipation. Scaling of V_T however leads to substantial increase in the sub-threshold leakage power and is expected to become a considerable constituent of the total dissipated power. It has been observed that the stacking of two off devices has smaller leakage current than one off device. This paper proposes a SRAM cell circuit based on CNTFET that uses Forced Stack Technique to reduce leakage power. This circuit is simulated using HSPICE with Stanford CNFET model at 32nm. The simulated results shows that this proposed Forced Stack CNTFET SRAM cell reduces a leakage-power by 38.6% compared to conventional 6T CNTFET SRAM cell with minimal Area and delay trade off.
Keywords - **SRAM Cell, CNTFET, Leakage-Power, HSPICE, Forced Stack**

I. INTRODUCTION

The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Thinner gate oxides have led to an increase in gate leakage current. Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption. In 65 nm and below technologies, leakage accounts for 30-40% of processor power.

According to the International Technology Roadmap for Semiconductors (ITRS) [1], leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink.

According to Moore's law, the dimensions of individual devices in an integrated circuit have been decreased by a factor of approximately two every two years. This scaling down of devices has been the driving force in technological advances since late 20th century. However, as noted by ITRS 2009 edition, further scaling down has faced serious limits related to fabrication technology and device performances as the critical dimension shrunk down to sub-22 nm range [1]. The limits involve electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping [2]. Carbon nanotubes (CNT) are very promising in respect of overcoming the serious limits faced by the Si CMOS Technology, because of their exceptional structural, electronic, and optical properties [2]. In particular, they exhibit ballistic transport over length scales of several hundred nanometers. Nanotube devices can be integrated with existing silicon-based structures. A CNTFET refers to a FET that uses CNT as the channel instead of bulk silicon in the traditional MOSFET structure.

SRAM, which is one of the main building blocks in digital circuits, occupies about 90% of the area of a SoC in 2013 [1]. SRAM is also one of the important sources of static power consumption. Therefore, it is important to design new low power SRAM using novel devices like CNTFETs.

Recently, Authors [3-8] proposed a new SRAM cell design using CNFETs. While there are several circuit-level solutions to reduce leakage in processors [9-12], this paper proposes a novel approach for reducing leakage power in CNTFET based SRAM Cell with minimum possible area and delay trade off..

II. THE CARBON NANOTUBE FET

A CNT is a tube made entirely of Carbon with a diameter of about a nanometer ($1/1,000,000,000$th of a meter). A CNT is a rolled tube of Carbon atoms in a honeycomb arrangement. CNTFET is a three-terminal device consisting of a semiconducting nanotube bringing two contacts (source and drain), and acting as a carrier channel, which is turned on or off electrically via the third contact (gate). Presently, there are

several types of CNTFETs have been fabricated, but CNTFET geometries may be grouped in two major categories: planar and coaxial CNTFET, whether planar or coaxial, relies on simple principles, while being governed by additional phenomena such as 1D density of states (DOS), ballistic transport, and phonon scattering [13].

Planar CNTFETs as shown in Fig. 1(a) constitute the majority of devices fabricated to date, mostly due to their relative simplicity and moderate compatibility with existing manufacturing technologies. The coaxial geometry as shown in Fig. 1(b) maximizes the capacitive coupling between the gate electrode and the nanotube surface, thereby inducing more channel charge at a given bias than other geometries. This improved coupling is desirable in mitigating the short-channel effects that plague technologies like CMOS as they downside device features. Parameters such as pitch, channel length (Lch), gate width (Wgate), and number of tubes will affect the performance of CNFET. The threshold voltage of CNFET is determined by the CNT diameter [14].
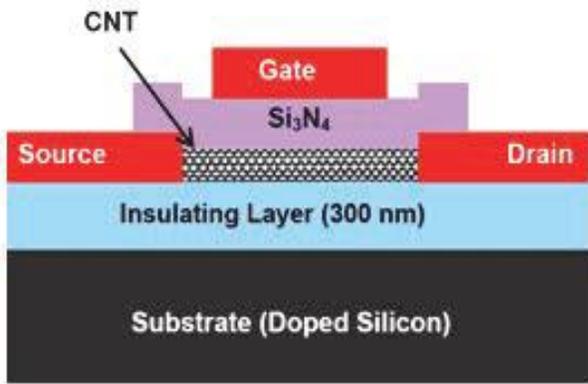
(a)
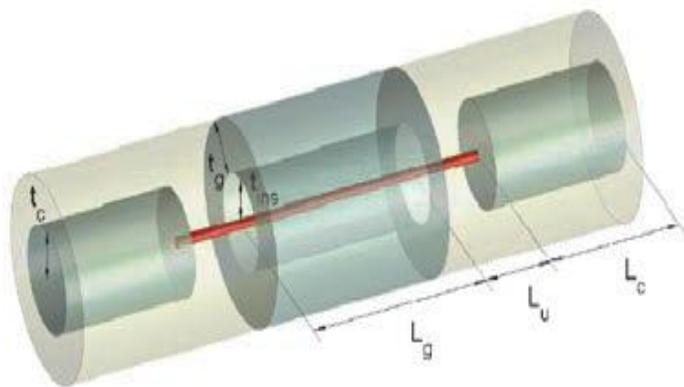
(b)

Fig. 1: Structures of CNTFETs: (a) planar (b) coaxial

Carbon nanomaterials have been identified as potential candidates to replace silicon in high-speed, low-power device channels. Channel length of CNTFETs can be reduced to 5nm, before tunneling at room temperature results in unacceptable leakage currents. The sizing of a CNTFET is equivalent to adjusting the number of tubes.

III.   FORCED STACK BAICS

Stacking transistor can reduce sub-threshold leakage [9]. So it is called stacked effect. Where two or more stacked transistor is turned off together, the result can reduce the leakage power. The effect of stacking on reducing leakage can be understood from the Fig. 2.
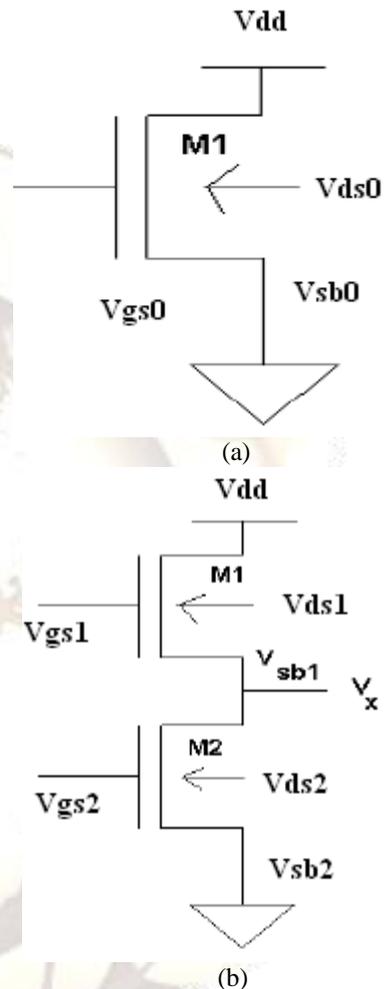

(a)

(b)

Fig. 2: (a) Single Transistor
(b) Forced Stack Transistor

If the input is '0', then both transistor M1 and M2 are turned off. Here Vx is the intermediate node voltage between M1 and M2. Transistor M2 has its internal resistance. Due to this resistance Vx is greater than the ground potential. This positive Vx results in a negative gate-source (Vgs) for the M1 transistor and the negative source-base voltage (Vsb) for M1. Here M1 also has a reduced drain-source voltage (Vds), which lower the drain induced barrier lowering (DIBL) effect. These three effects together reduced the the leakage power. The Figure 3 also illustrates the concept of Stacking effect.
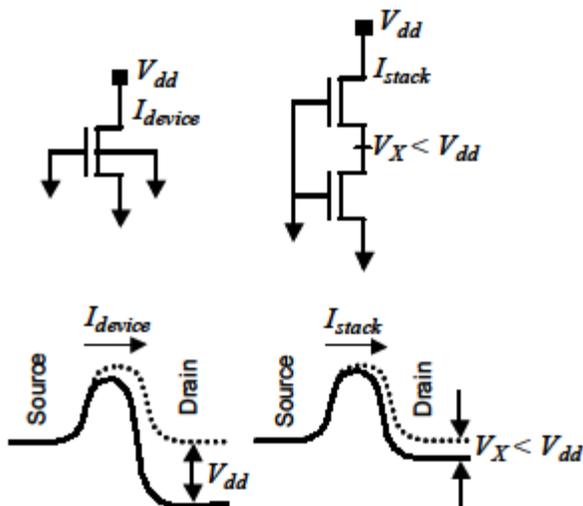
Fig. 3: Leakage current difference between a single OFF device and a stack of two OFF devices.

IV. THE PROPOSED FORCED STACK CNTFET SRAM CELL

Fig. 4 shows a SRAM Cell based on CNTFETs using Forced Stack Technique to reduce leakage power. Two pairs of Stack transistors (M1, M4 and M5, M8) are used in the SRAM cell. One in each pair is activated during idle mode based upon the value of the bit stored in the cell. This disconnects the OFF transistors from supply while retaining supply to the ON transistors. The effect of stacking the transistor results in the reduction of subthreshold leakage current when two or more transistors are turned off together. In the Conventional 6T CNTFET SRAM Cell there are only 6 transistors. But here in case of forced stack CNTFET SRAM Cell two extra pull up transistors (M4 and M8) and two extra pull down transistors (M1 and M5) are added in addition to original 6 transistors. M2, M3, M5, M7, M9 and M10 are original six transistors. All inputs share the same input in the forced stack circuit. This forced stack technique is a state saving technique. That means when the circuit is in OFF mode it saves the current state. The main drawback of this forced stack inverter is that it can not use the high Vth transistor. Because if it use the high Vth transistor than there is a dramatic increase of delay. This delay increase is 5X larger than the conventional CMOS.

In CNTFETs the number of tubes used for each transistor decides their size. In this design 1 tube is used in all the stack transistors (M1, M4, M5 and M8), 2 tubes are used in two pull-up transistors M3, M7 and two access transistors M9 and M10. 3 tubes are used in two pull-down transistors M2 and M6.
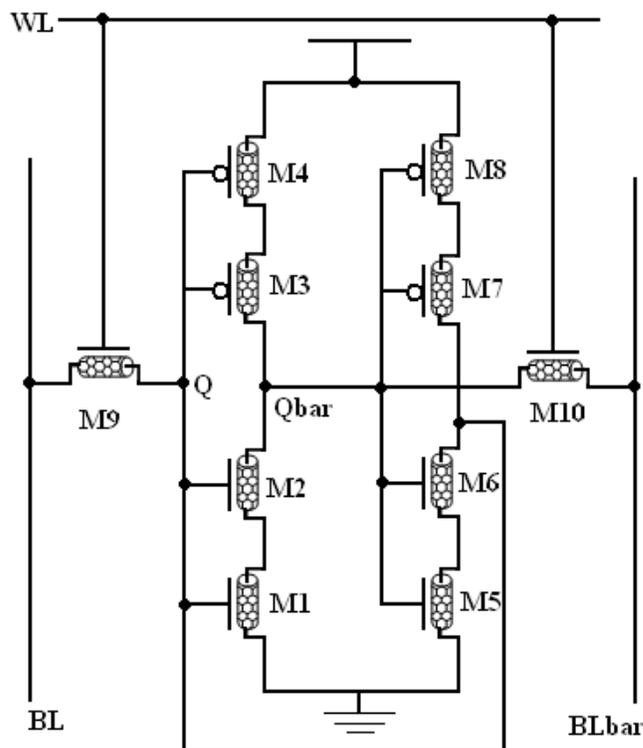

Fig. 4: The Proposed Forced Stack CNTFET SRAM Cell

V.   SIMULATION RESULTS

The proposed SRAM cell based on CNTFETs is designed and simulated using the Synopsis HSPICE. Simulations performed with Stanford CNTFET model at 32nm feature size with supply voltage V_{DD} of 0.9V [15].

The following technology parameters are used for simulation of 6T and 7T SRAM cells using CNTFET Technology [16]:

- Physical channel length (L_channel) = 32.0nm.
- The length of doped CNT source/drain extension region (L_sd) = 32.0nm.
- Fermi level of the doped S/D tube (Efo) = 0.6 eV.
- The thickness of high-k top gate dielectric material (Tox) = 4.0nm.
- Chirality of tube (m,n) = (19,0).
- CNT Pitch = 10nm.
- Flatband voltage for n-CNTFET and p-CNTFET (Vfbn and Vfbp) = 0.0eV and 0.0eV.
- The mean free path in intrinsic CNT (Lceff) = 200.0nm.
- The mean free path in p+/n+ doped CNT = 15.0nm.
- The work function of Source/Drain metal contact = 4.6eV.
- CNT work function = 4.5eV.

The HSPICE Cscope is used for displaying and measuring simulation parameters. From these measurements it is conformed that the leakage currents through off transistors of CNTFET SRAM Cell with Forced stack Transistors are very

small compared to CNTFET SRAM cell without forced stack Transistors. Leakage currents flowing through OFF transistors of CNTFET SRAM cell with and without Forced Stack Transistors are compared and summarized in Table I and Table II when Q=1 and Q=0 respectively. The total Power dissipated in CNTFET SRAM cell without and with Forced Stack Transistors are 72.4185nW and 66.3803nW respectively.

TABLE I.   LEKAGE CURRENT THROUGH OFF TRANSISTORS IF Q=1

Sl. No.	Leakage Currents (A)	6T CNTFET SRAM Cell Without Forced Stack Transistors	6T CNTFET SRAM Cell With Forced Stack Transistors
1	I (M3, M4)	1.767e-06	1.130e-08
2	I(M5, M6)	7.133e-07	2.365e-08
3	I(M10)	6.789e-06	3.168e-07
4	Total Leakage	7.843e-06	3.292e-07

TABLE II.   LEKAGE CURRENT THROUGH OFF TRANSISTORS IF Q=0

Sl. No.	Leakage Currents (A)	6T CNTFET SRAM Cell Without Forced Stack Transistors	6T CNTFET SRAM Cell With Forced Stack Transistors
1	I (M1, M2)	1.767e-06	1.117e-08
2	I(M7, M8)	7.133e-07	2.350e-08
3	I(M9)	6.829e-06	2.758e-07
4	Total Leakage	7.883e-06	2.882e-07

VI. CONCLUSION

Carbon nanotube electronics remains a very promising route to solve future down-scaling problems of conventional silicon technology. In this paper a CNTFET SRAM cell using Forced Stack technique is designed and simulated using HSPICE with Stanford CNFET Model at 32nm Technology for Low-Leakage power. The results shows that this proposed Forced Stack CNTFET SRAM cell reduces a leakage-power to the significant effect compared to conventional 6T CNTFET SRAM cell with minimal area and delay trade off. This circuit is very promising for low-leakage power CNTFET Memory designs.

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