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An Approach to Avoid Existing Overrun Error Problem in Universal Synchronous Asynchronous Receiver Transmitter (USART) Receiver Section by Using Queue and CPU Latency

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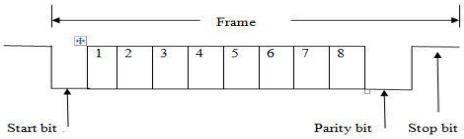
Abstract
USART is a device which is used in serial communication. In parallel communication number of line between transmitter and receiver depends on number of bits to be transmitted, to transmit one byte 8 lines are required between transmitter and receiver which increase the cost. However due to overlapping between lines cross talk will occur, to overcome this problem in communication USART is used. USART is a device which is capable to convert parallel to serial at the transmitter end and serial to parallel at the receiver end. However USART suffer from overrun error, parity error and framing error problem. In this paper we are proposing a method which stores the data in a queue and this queue is implemented using dynamic memory allocation to avoid overrun error in USART.

I. INTRODUCTION

Most of the microprocessor based systems are designed for parallel data transfer, because that is the fastest way to do it. In parallel communication number of lines required to transfer data depends upon number of bits to be transferred i.e. to transfer 1 byte of data 8 lines are required from transmitter to receiver, however to transfer data over long distance parallel data transmission requires too many wires which is expensive and its difficult to maintain. If two line overlap on each other then it leads to cross talk i.e overlapping of information on the adjacent channel . Where as, in serial communication data can be transferred over a long distance between two systems as it reduces distortion of signals. Therefore, data to be sent for long distances is converted from parallel form to serial form so that it can be sent on a single wire [1]. Serial data received from long distance is converted to parallel form so that it can easily be transferred on the microcomputer buses.

Serial data can be sent synchronously or asynchronously using a device called USART (universal synchronous asynchronous receiver transmitter). It has built in baud rate generator and it allows full duplex transmission and reception. In asynchronous communication there is different clock between transmitter and receiver to make synchronization between transmitter and receiver we make use of start bit and stop bit. In asynchronous data transfer, data is transmitted in terms of characters. The combination of start bit, character and stop bit is known as frame. Different systems uses different stop bits such as 1, 1.5 and 2 depending upon the speed of the receiver. The start and stop bit carry no information, but are required because of asynchronous nature of data [3]. Here start bit is used to indicate the receiver about the beginning of the frame which is always logic high where as stop bits are used to indicate the end of the frame which is always logic low.



II. Existing method to send and receive character in USART

USART consist of two buffer registers such as transmitter SBUF and receiver SBUF. Data is stored in transmitter SBUF register and parity bit is stored in TB8 of SCON resister and then data is transmitted and then Transmitter interrupt (TI) is set in SCON, its programmer or user responsibility to clear TI to transmit next character. To know how many characters have been sent a counter can be used. The transmitter will stay low until another character is ready to be read. Receiver will recognize valid start bit and then receiver discard start bit and data is store in receiver SBUF register and parity bit is store in RB8 and then Receiver Interrupt (RI) is set in SCON to indicate data is received, its programmer or user responsibility to clear RI to receiver next character.

III. CASE STUDY

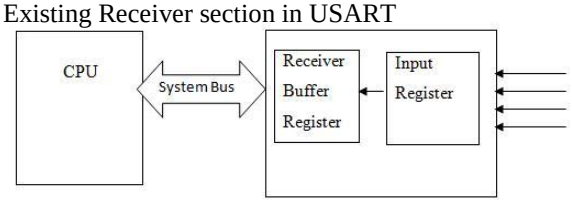
By the assessment of several research papers and related work many authors had tried to over come this overrun error by different phenomenon and have suggested a few methods. CPU should be run at a maximum possible speed, to speed up the execution of USART interrupt. We can prevent the overrun error created due to interrupt latencies by reducing the baud rate of USART. We can overcome this error by keeping the USART ISR (Interrupt service routine) efficient and as short as possible i.e. the time taken to execute ISR must be less than the time taken to receive next data byte. By keeping this in view the author made an attempt to over come this overrun error by using queue. Queue is implemented using dynamic memory allocation to avoid overrun error in USART.

IV. USART - OVERRUN ERROR

In USART the receiver section consist of two register that is input register and receiver buffer register. Input register receives data in serial form and convert it in parallel form and output is stored in receiver buffer. CPU is supposed to read this character before next character is received, but if CPU fails to read the character then next received character replaces the previous one and when CPU attempts to read character it reads second character instead of reading first character this is called over run error.

V. An approach to avoid overrun problem in USART

Existing Receiver section in USART



a. queue method to avoid overrun error

In this paper author made an attempt to propose a method to overcome overrun error problem in USART, which intend improve the overall efficiency in serial communication and more reliable data reception and the receiver end. The figure shown below illustrates modification to conventional USART receiver section. Input register store serial data and convert it in to parallel and then this parallel data is stored in queue , then the queue register generates a control signal i.e. Receiver buffer register Empty (RE) to check whether Receiver buffer register is empty. If Receiver buffer register is empty then its generate acknowledge (REA) to inform that it is empty and ready to accept data, then queue send data in to receiver buffer register [1].

If receiver buffer register is full i.e. CPU did not read data from receiver buffer register and mean while new data comes then input register converts it into parallel and then data is store in queue. Here queue memory is allocation dynamically by using malloc function. Syntax for dynamic memory allocation is malloc (sizeof(char a)) .

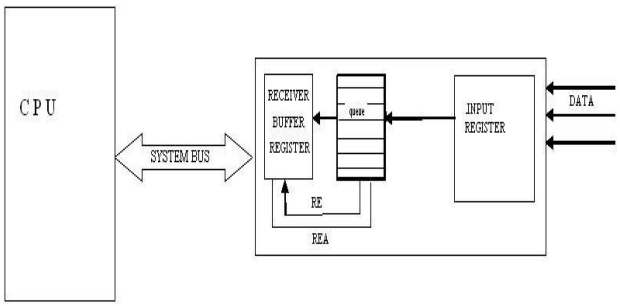
Char *cptr; // creating char pointer

Cptr= (*cptr) malloc(sizeof(cptr)); // allotting dynamic memory to char pointer with type casting

***cptr // dereferencing a char pointer**

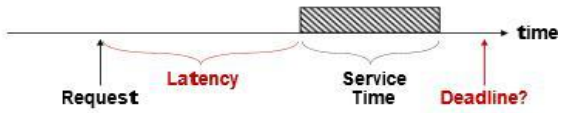
Now queue check whether receiver buffer is empty, if receiver buffer register is full queue does not get any acknowledge, then new data is stored in queue in FIFI method rather than over writing it in receiver buffer register. Now when CPU attempt to read data it reads data from receiver buffer register. After CPU read the data from receiver buffer register, it generates REA signal to accept new data which is stored in queue in FIFO manner.

Proposed Receiver section in USART using Queue



b. CPU latency to avoid overrun error: There are different data transfer mechanisms in which CPU provides service to its peripherals i.e DMA data transfer, Interrupt driven data transfer, polling data transfer and stored program data transfer. In polling method the processor continuously check the devices to know whether it requesting its service or not. It is an inefficient method as processor time is wasted unnecessary for checking the request rather then providing service. In contrast an interrupt is nothing but disturbance to CPU which causes Microprocessor to work with requested task and later return to its previous task. Interrupt Latency is defined as the time difference between receiving interrupt request from interrupt source and service provided to it. Throughput and interrupt latency have inverse relation that is throughput of the microprocessor increases by reducing interrupt latency. In this paper

author made an attempt to avoid overrun error using interrupt latency [4]. If CPU gives high priority to USART interrupt i.e CPU reduces USART interrupt latency time. Therefore CPU reads character faster from receiver buffer register before the new character arrives.



VII. CONCLUSION

In this paper author proposed two different methods that Queue and CPU latency to avoid overrun error in Universal Synchronous Asynchronous Receiver Transmitter (USART), by using this technique we can improve the efficiency of received data.

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