

Review of Viterbi Decoder for Trellis Coded Modulation System

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ABSTRACT

The Viterbi algorithm is commonly used in a wide range of communications and data storage applications. It is used for decoding convolutional codes, in baseband detection for wireless systems, and also for detection of recorded data in magnetic disk drives. The requirements for the Viterbi decoder or Viterbi detector, which is a processor that implements the Viterbi algorithm, depend on the applications where they are used. This results in very wide range of required data throughputs and power or area requirements. Viterbi detectors are used in cellular telephones with low data rates, of the order below 1Mb/s but with very low energy dissipation requirement. They are used for trellis code demodulation in telephone line modems, where the throughput is in the range of tens of kb/s, with restrictive limits in power dissipation and the area/cost of the chip. On the opposite end, very high speed Viterbi detectors are used in magnetic disk drive read channels, with throughputs over 600Mb/s. But at these high speeds, area and power are still limited.

Keywords – TCM, decoding algorithm, TB method, RE Method, HRE Method.

I. INTRODUCTION

The task which a designer faces in a digital communication system is of providing a cost effective facility for transmitting information from one end of the system at a rate and a level of reliability and quality that are acceptable to the user at the other end. Convolutional encoding with Viterbi decoding is a technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by additive white Gaussian noise (AWGN). Viterbi decoding was developed by Andrew J. Viterbi in 1967. Since then, other researchers have expanded on his work by finding good convolutional codes, exploring the performance limits of the technique, and varying decoder design parameters to optimize the implementation of the technique in hardware and software. The Viterbi decoding algorithm is also used in decoding trellis-coded modulation technique which is used as an effective coding technique for band limited channels as in telephone line modems to squeeze high ratios of bits-per-second in 3kHz band-width analog telephone lines. For years, convolutional coding with Viterbi decoding has been the predominant Forward error, correction (FEC) technique used in space communications, particularly in geostationary satellite communication networks, such as VSAT (very small aperture terminal). In the following sections the coder used in this communication will be

described as well as the Viterbi decoding technique.

The Viterbi Algorithm, an application of dynamic programming, is widely used for estimation and detection problems in digital communications and signal processing. It is used to detect signals in communications channels with memory, and to decode sequential error control codes that are used to enhance the performance of digital communication systems. Though various platforms can be used for realizing Viterbi Decoder including Field Programmable Gate Array (FPGAs), Complex Programmable Logic Devices (CPLDs) or Digital Signal Processing (DSP) chips but here benefit of using an FPGA to Implement Viterbi Decoding Algorithm has been described. FPGAs are a technology that gives the designer flexibility of a programmable solution, the performance of a custom solution and lowering overall cost. The advantages of the FPGA approach to DSP Implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC. The FPGA also adds design flexibility and adaptability with optimal device utilization conserving both boarspace and system power that is often not the case with DSP chips.

The problem of survival memory management of a Viterbi Decoder (VD) was solved by introducing a

pointer implementation for the register exchange (RE) method, where a pointer is assigned to each row of memory in the SMU. The content of the pointer which points to one row of memory is altered to point to another row of memory, instead of copying the contents of the first row to the second.

II. TWO IMPORTANT BLOCK OF VITERBI DECODING SYSTEM

A structure and short overview of the basic Viterbi decoding system is illustrated in Fig. 1. This figure shows three basic elements of the Viterbi decoding communication system: convolutional encoder, communication channel and Viterbi decoder.

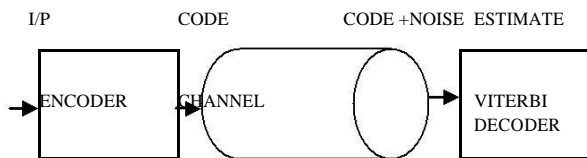


Fig 1: Basic Viterbi Decoding System

2.1 Convolutional Encoder

Convolutional encoder consists of linear shift register and XOR gates; and is generally characterized in (n, k, m+1) format, where: n represents the number of outputs of the encoder; k is the number of inputs of the encoder, m is the number of memory elements (Flip-Flops) and m+1 represents the constraint length. The rate of this encoder can be represented as k/n. The Figure2 shows the convolutional encoder structure CC (4,3,6) . It consists of 6 (m=6) shift register stages and four modulo-3 adders (n= 4) giving the outputs of the encoder. The rate of the code is $r = 3/4$.

TABLE I
ENCODER SPECIFICATION

Parameter	Parameter	Value
Input Length	k	3
Output Length	n	4
Coding Rate	k/n	3/4
Memory register count	m	6
Constrain Length	K	7

The outputs Z0, Z1, Z2 and Z3 of the adders are governed by the following generator polynomials general Equation. We denote by g_i the K-element generator polynomial for parity bit p_i . We can then write $p_i[n]$ as follows:

$k-1$

$$p_i [n] = \left(\sum_{j=0}^{k-1} g_i [j] x [n-j] \right)$$

The form of the above equation is a convolution of g and x (modulo 2)—hence the term

—convolutional code. The number of generator polynomials is equal to the number of generated parity bits, r, in each sliding window. The rate of the code is 1/r if the encoder slides the window one bit at a time.

The polynomials give code its unique error protection quality.

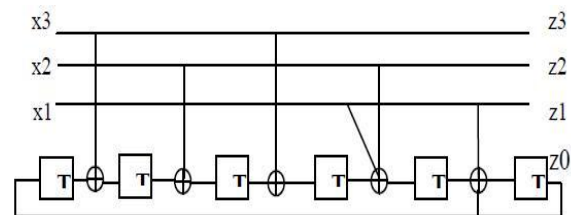


Fig 2: Convolutional Encoder for rate 3/4

2.2 Viterbi Decoder

The Viterbi decoding algorithm is a decoding process for Convolutional codes. This algorithm is based on maximum likelihood algorithm. Received signal quantized in many levels. If the levels are two then it is hard decision. If the levels are many then it is Soft decision. Soft decision is better in error performance but has higher complexity [4]. When the received signal is sampled and quantized into two levels, either zero or one, the hard decision decoding will be used. In such decoding, the path through the trellis diagram is determined using hamming distance measure. Where the trellis represents the extension of the state diagram with the time. The hamming distance is defined as a number of bits that are different between the observed symbol at the decoder and the sent symbol from the encoder [4]. The length of the trellis is equal to the length of the input sequence, which consists of the information bits followed by the reset sequence. The reset sequence forces the trellis into the initial state, so the trace back can be started at the initial state. Figure (3) shows the simplified Viterbi decoder block diagram.

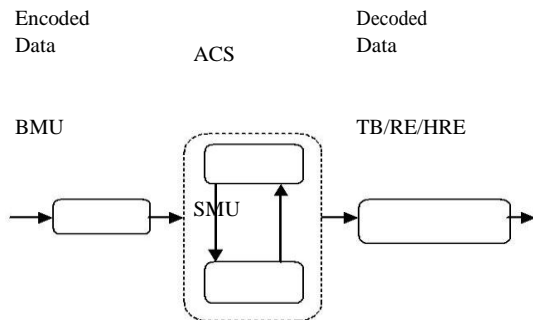


Fig. 3: Simplified Viterbi Decoder Block Diagram

2.3 Viterbi Decoder System

The basic units of Viterbi decoder are branch metric unit, add compare and select unit and survivor memory management unit.

2.3.1 Branch Metric Unit

The first unit is called branch metric unit (BMU). Here the received data symbols are compared to the ideal outputs of the encoder from the transmitter and branch metric is calculated. BMU is transition metric unit and its function is to generate corresponding merit of skip branch according to the input code sequence. The generated sequence merit is delivered to ACS unit, completing the process as bit calculation. Then BMs are fed into the add compare-select unit. Hamming distance or the Euclidean distance is used for branch metric computation.

2.3.2 Path Metric Unit

The second unit, called path metric computation unit, calculates the path metrics of a stage by adding the branch metrics, associated with a received symbol, to the path metrics from the previous stage of the trellis.

2.3.3 Survivor Memory Management Unit

The final unit is the trace-back process or register exchange method, where the survivor path and the output data are identified. The trace-back (TB) and the register exchange (RE) methods are the two major techniques used for the path history management in the chip designs of Viterbi decoders. The TB method takes up less area but requires more time as compared to RE method because it needs to search or trace the survivor path back sequentially. Also, extra hardware is required to reverse the decoded bits.

2.3.4 TraceBack Method & Register Exchange

Method

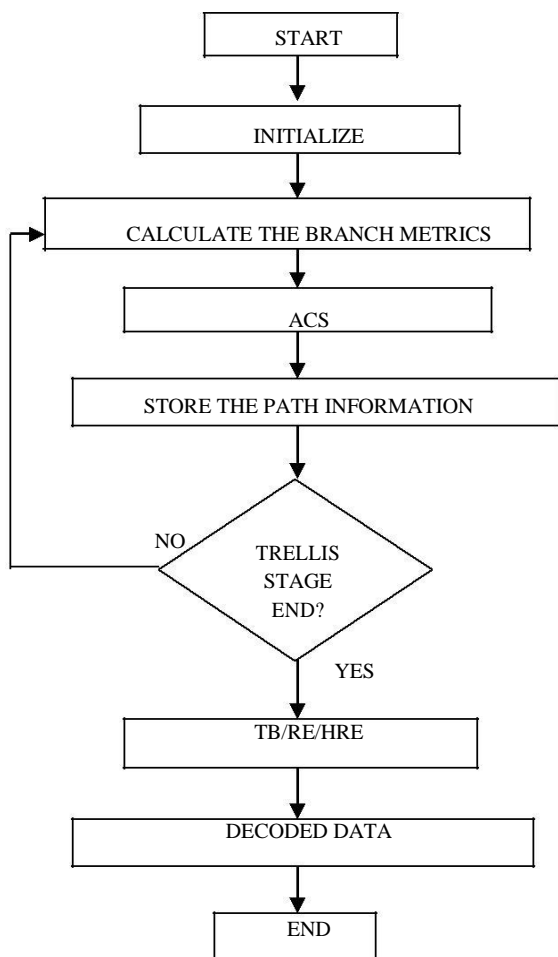
In the TB method, the storage can be implemented as RAM and is called the path memory. Comparisons in the ACS unit and not the actual survivors are stored. After at least L branches have been processed, the trellis connections are recalled in the reverse order and the path is traced back through the trellis diagram. The TB method extracts the decoded bits, beginning from the state with the minimum PM. Beginning at this state and tracing backward in time by following the survivor path, which originally contributed to the current PM, a unique path is identified. While tracing back through the trellis, the decoded output sequence, corresponding to the traced branches, is generated in the reverse order. Trace back architecture has a limited memory bandwidth in nature, and thus limits the decoding speed.

The register exchange (RE) method is the simplest conceptually and a commonly used technique. Because of the large power consumption and large area required in VLSI implementations of the RE method, the trace back method (TB) method is the preferred method in the design of large constraint length, high performance Viterbi decoders[3]. In the register exchange, a register assigned to each state contains information bits for the survivor path from the initial state to the current state.

2.4 Viterbi Decoder Algorithm Design Flow

The algorithm can be broken down into the following three steps:

- i) Weigh the trellis; that is, calculate the branch metrics.
- ii) Recursively computes the shortest paths to time n, in terms of the shortest paths to time n-1. In this step, decisions are used to recursively update the survivor path of the signal. This is known as add-compare select (ACS) recursion.
- iii) Recursively finds the shortest path leading to each trellis state using the decisions from Step 2. The shortest path is called the survivor path for that state and the process is referred to as survivor path decode. Finally, if all survivor paths are traced back in time, they merge into a unique path, which is the most likely signal path.



III. LITERATURE REVIEW

An exhaustive literature review has been carried out related to the titled work to find out the current research. Abstracts of some of the most relevant research works are reported in the following paragraph

3.1 High-Speed Low-Power Viterbi Decoder Design for TCM Decoders Jinjin He, Huaping Liu, Zhongfeng Wang, Xinming Huang, andkai Zhang iee transactions on very large scale integration (vlsi) systems, vol. 20, no. 4, April 2012.

Author has proposed a high-speed low-power VD design for TCM systems. The precomputation architecture that incorporates T –algorithm efficiently reduces the power consumption of vds without reducing the decoding speeds appreciably. Authors have also analyzed the precomputation algorithm, where the optimal precomputation steps are calculated and this algorithm is suitable for TCM systems which always employ high-rate convolutional codes. Both the ACSU and SMU are modified to correctly decode the signal. ASIC synthesis and power estimation results show that, compared with the full-trellis VD without a low-

power scheme, the precomputation VD could reduce the power consumption by 70% with only 11% reduction of the maximum decoding speed.

3.2 Yang min,|| Design optimization of FPGA based Viterbi decoder||, IEEE international conference, April- 2011 ISSN: 978-1-4244-8036Vol.1, Issue.1, pp- 4129 - 4131.

Yang min [2] proposed a novel Viterbi decoder in part parallel structure. The core part of the decoder-Add - Compare - Select Unit, is improved by means of pipeline. BMC (Branch Metric Computation) is improved through linear transform. TB (Trace Back).

3.3 FPGA Based Efficient Implementation of Viterbi Decoder Anubhuti Khare, Manish Saxena, Jagdish Patel, International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-1,

Issue 1, October 2011.

In this paper author presented an implementation of the Viterbi Decoder with constraint length of 3 and code rate of 1/2, The proposed solution has proven to be particularly efficient in terms of the required FPGA implementation resources so as Chip Silicon Area, Decoding Time and Power Consumption. Author have developed Viterbi Decoder on Spartan 3A FPGA by utilizing both method and Synthesis result shows that Traceback method is more efficient in term of Chip Area Utilization so as will be Power Consumption in comparison with Register Exchanged Method.

3.4 Fpga Implementation of Soft Output Viterbi Algorithm Using Memoryless Hybrid Register Exchange Method R .D. Kadam and S. L. Haridas International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.3, September 2011.

In this paper author show that The MLVD using HREM is a memoryless implementation of the VA, and successfully decodes the continuous data encoded by a convolutional encoder. The latency is only 2 data bits. The new implementation is realized by applying the pointer concept to the HREM implementation, and by using trellis truncation for every bit encoded. It is found that the new proposed decoding technique requires lesser hardware as compared to REM, HREM and memoryless REM techniques. So the memoryless hybrid register exchange approach can be used in place of traceback, register exchange for decoding of data.

3.5 —FPGA Implementation of Viterbi Decoder|| Hema.S, Suresh Babu.V, Ramesh P Hema.S. Proceedings of the 6th WSEAS Int. Conf. on Electronics, Hardware, Wireless and Optical Communications, Corfu Island, Greece, February 16-19, 2007.

Presented a field programmable gate array implementation of Viterbi Decoder with a constraint length of 11 and a code rate of 1/3. It shows that the larger the constraint length used in a Convolutional encoding process, the more powerful the code produced. A Viterbi algorithm based on the strongly connected trellis decoding of binary a convolutional code has been presented.

3.6 || Design and Tradeoff Analysis of an Area Efficient Viterbi Decoder|| IEEE international conference, march- 2007, ISSN: 0-7803-9429-1 Vol.1, Issue.1, pp-1.

Saleem, examined the Viterbi decoder is widely used in digital communication systems. It performs the maximum-likelihood decoding of Convolutional codes received from a noisy channel Depending on the application (terrestrial, satellite, digital modems, digital cellular telephone applications and others) a Viterbi decoder must be designed to meet specific requirements such as small area, high speed or maximum efficiency. They also present a novel architecture for area efficient Viterbi decoder, which can be used for low bit rate applications. The design schedules all computations on less number of ACS processing elements as compared to parallel implementation assuming that a lot of clock cycles are available for decoding.

3.7 —Good trellises for IC implementation of Viterbi decoders for linear block codes|| Moorthy, H.T IEEE Trans. Communication, vol.45, pp. 50-67, 1997.

Moorthy, investigates trellis structures of linear block codes for the integrated circuit (IC) implementation of Viterbi decoders capable of achieving high decoding speed while satisfying a constraint on the structural complexity of the trellis in terms of the maximum number of states at any particular depth. Only uniform section alizations of the code trellis diagram are considered. An upper bound on the number of parallel and structurally identical (or isomorphic) sub trellises in a proper trellis for a code without exceeding the maximum state complexity of the minimal trellis of the code is first derived

3.8 —A Dynamically Reconfigurable Adaptive Viterbi Decoder||, Sriram Swaminathan, Russell Tessier, Dennis Goeckel, and Wayne Burleson

Wayne Burleson, FPGA'02, February 24-26, 2002.

Sriram Swaminathan, describes the analysis and implementations of a reduced complexity decode approach, the adaptive Viterbi algorithm (AVA). Their AVA design is implemented in reconfigurable hardware to take full advantage of algorithm parallelism and specialization. Run-time dynamic reconfiguration is used in response to changing channel noise conditions to achieve improved decoder performance.

3.9 “Design and Implementation of Viterbi Decoder Using FPGAs”, B.Pandita Published in the Proceedings of the 12th International Conference on VLSI Design.

B. Pandita, describes the design and implementation of Viterbi decoder using FPGAs. In this paper we explore an FPGA based implementation methodology for rapid prototyping designs. We use high level synthesis to achieve this. One of the main blocks of a CDMA modem used during forward-link demodulation is a Viterbi decoder.

IV. CONCLUSIONS

Viterbi Algorithm is widely used for the elimination of the potential noise in a data stream. Encoding is such that the Viterbi Decoder can remove potential noise in the incoming stream by decoding it. The characteristics of the decoder are its effectiveness in noise elimination, speed of decoding and cost (hardware utilization). This review concludes that the results of the present study are of great importance in the viterbi decoder which is one of the challenging tasks in communication system. Effectiveness in noise elimination, speed of decoding and cost achieved in all these research work is satisfactory however by using and integrating some other techniques this can be improved.

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