

## "FPGA Based Implementation of AES Encryption and Decryption with Verilog HDL"

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### Abstract

Security is the most important part in data communication system, where more randomization in secret keys increases the security as well as complexity of the cryptography algorithms. As a result in recent dates these algorithms are compensating with enormous memory spaces and large execution time on hardware platform. Field programmable gate arrays (FPGAs), provide one of the major alternative in hardware platform scenario due to its reconfiguration nature, low price and marketing speed. In this a hardware implementation of the AES128 encryption and decryption algorithm is proposed. The AES cryptography algorithm can be used to encrypt/decrypt blocks of 128 bits and is capable of using cipher keys of 128 bits wide (AES128). A unique feature of the proposed pipelined design is that the round keys, which are consumed during different iterations of encryption, are generated in parallel with the encryption process. This lowers the delay associated with each round of encryption and reduces the overall encryption delay of a plaintext block. This will lead to an increase in the message encryption throughput. This method will experimentally simulate using Xilinx software with Verilog Hardware Description Language and hardware implementation on FPGA.

**Keywords:** AES cryptography, FPGA, pipelined design, throughput, Xilinx.

### I. INTRODUCTION

AES is short for Advanced Encryption Standard and is a United States encryption standard defined in Federal Information Processing Standard (FIPS) 192, published in November 2001. It was ratified as a federal standard in May 2002. AES supersedes Data Encryption Standard (DES). The DES algorithm broken because of short keys (56-bit key). AES can be implemented both on hardware and software.

AES is a symmetric encryption algorithm processing data in block of 128 bits. Under the influence of a key, a 128-bit block is encrypted by transforming it in a unique way into a new block of the same size. AES is symmetric since the same key is used for encryption and the reverse transformation, decryption. The only secret necessary to keep for security is the key. In this project new AES algorithm with encryption and decryption was realized in Verilog Hardware Description Language. The 128-bit plaintext and 128-bit key, as well as the 128-bit output data were all divided into four 32-bit consecutive units respectively controlled by the clock. The pipelining technology was utilized in the intermediate nine round transformations so that the new algorithm achieved a balance between speed and chip area.

AES-128 may be configured to use different key-lengths, the standard defines 3 lengths and the resulting algorithms are named AES-128, AES-192 and AES-256 respectively to indicate the length in

bits of the key. In this project AES-128 encryption and decryption with 128-bit key is considered [1-4]. Each additional bit in the key effectively doubles the strength of the algorithm, when defined as the time necessary for an attacker to stage a brute force attack, i.e. an exhaustive search of all possible key combinations in order to find the right one. AES can resist various currently known attacks. Hardware security solution based on highly optimized programmable FPGA provides the parallel processing capabilities and can achieve the required performance benchmarks. The current Area Optimized algorithm of AES are mainly based on the realization of S-box mode and the minimizing of the internal registers which could save the area of IP core significantly [1-5].

The rest of the paper is organized as follows. Section 2, describes existing model, 3, describes proposed improved AES Encryption Algorithm with pipeline technology during round transformation, Section 4, describes proposed decryption, Section 5 describes comparison. Finally concluded the paper in section 6.

### II. EXISTING MODEL

AES is a specification for the encryption of electronic data. It has been adopted by the U.S government and is now used worldwide. The algorithm described by AES is a symmetric-key algorithm, meaning the same key is used for both encrypting and decrypting the data.

AES is based on a design principle known as a substitution-permutation network. It is fast in both software and hardware.[6] Unlike its predecessor, DES, AES does not use a Feistel network.

AES has a fixed block size of 128 bits and a key size of 128, 192, or 256 bits, whereas Rijndael can be specified with block and key sizes in any multiple of 32 bits, with a minimum of 128 bits. The block size has a maximum of 256 bits, but the keysize has no theoretical maximum.

AES operates on a 4x4 column-major order matrix of bytes, termed the state (versions of Rijndael with a larger block size have additional columns in the state). Most AES calculations are done in a special finite field.

The AES cipher is specified as a number of repetitions of transformation rounds that convert the input plaintext into the final output of ciphertext. Each round consists of several processing steps, including one that depends on the encryption key. A set of reverse rounds are applied to transform ciphertext back into the original plaintext using the same encryption key.

The algorithm is composed of three main parts: Cipher, Inverse Cipher and Key Expansion. Cipher converts data, commonly known as plaintext, to an unintelligible form called cipher. Key Expansion generates a key schedule that is used in the Cipher and the Inverse Cipher procedure. Cipher and Inverse Cipher are composed of specific number of rounds (Table 1). For the AES algorithm, the number of rounds to be performed during the execution of the algorithm is dependent on the key length [1]. AES operates on a 4x4 array of bytes (referred to as "state").

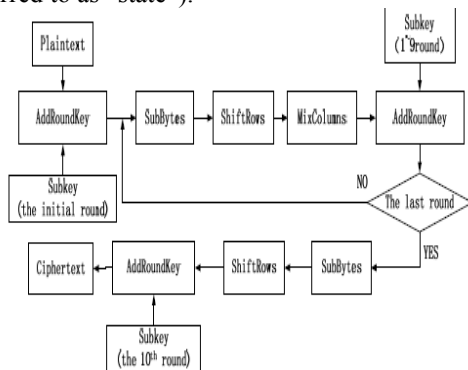


Fig1: Rijndael Algorithm

The algorithm consists of four different simple operations.

These operations are:

- Sub Bytes
- Shift Rows
- Mix Columns
- Add Round Key.

- Sub Bytes a non-linear substitution step where each byte is replaced with another according to a lookup table.
- Shift Rows—a transposition step where each row of the state is shifted cyclically a certain number of steps.
- Mix Columns—a mixing operation which operates on the columns of the state, combining the four bytes in each column.
- Add Round Key: Bit wise XOR operation

TABLE: 1. Features of AES for Different Key Lengths.

	Block size Nb	words	Key length Nk
<b>AES- 128_bits Key</b>	<b>4</b>	<b>4</b>	<b>10</b>
<b>AES-192_bits key</b>	<b>4</b>	<b>6</b>	<b>12</b>
<b>AES-256_bits key</b>	<b>4</b>	<b>8</b>	<b>14</b>

### III. The Design Of Improved AES Algorithm

The proposed architecture is designed to get maximum speed and lesser area by mapping all the four Logical functions of AES to LUTs, ROMs and Block RAMs. The proposed architecture has three parts

1. Key Generation Module
2. Encryption Module
3. Decryption Module.

The AES encryption and decryption core unit contains key generation module as a common unit. This module gives necessary key expansion for both encryption and decryption functions. Fig.2 presents the block diagram of AES Rijndael encryption and decryption with Key Generation Module as a common unit. The key generation module consists of key register of 128 bits, S-Box and XOR gates for bitwise XOR operation.

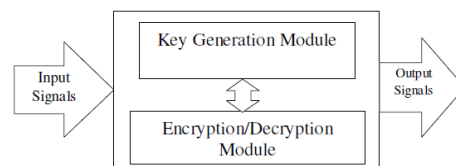


Fig 3.1: AES Encryption and Decryption Unit Block Diagram

It is designed to produce round keys on each positive edge of the clock, when it is enabled. However in the proposed work, the key generation

architecture does not require any hardware for shift operation and the port mapping between key register and S-Box is done according to the required shift. Hence the proposed work offers the advantage in area. Also in the proposed work the bits are rearranged on data path from register to S-Box and the round constant required for each rounds are stored in ROM and retrieved on each clock. Fig.3 represents proposed architecture of key generation unit.

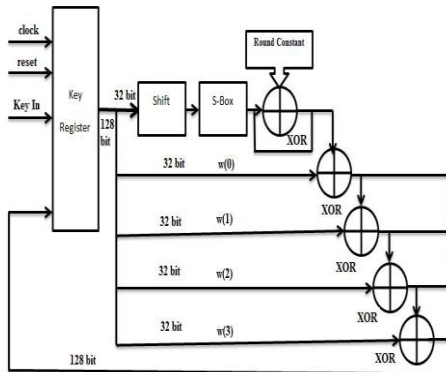


Fig. 3.2. Architecture of Key Generation Module.

### 3.1 Encryption:

The encryption module takes 128 bit text to be encrypted and receives round key from key generation module to do each round of encryption. Fig.4 presents the proposed encryption module.

Start, stop\_mix, terminate are control signal produced by the control unit. The “done” signal is provided to indicate that encryption is done. Architecture is as shown in Fig.5.

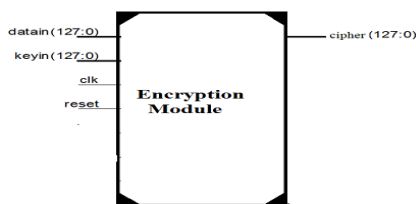


Fig 3.3 Encryption Module

In the proposed work for reducing the hardware of entire architecture, the control unit of encryption module is not designed separately. The control unit of key generation module which is a 4-bit counter is designed to control the entire functioning of encryption module. The sharing of control unit by both encryption and round key generation gives unique advantage of reduction in hardware as compared to other implementations.

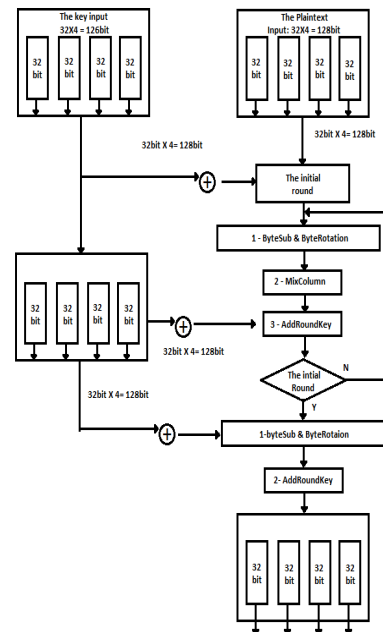


Fig. 3.4: Proposed architecture of encryption module

The functions of various parts of the structure shown above are described as follow:

- The initial round of encryption:  
The four packets of consecutive 32-bit plaintext (128 bits) have been put into the corresponding registers. Meanwhile, another four packets of consecutive 32-bit initial key (128 bits) have been put into other registers by the control of the enable clock signal. Furthermore, this module should combine the plaintext and initial key by using the XOR operators.

- Round Transformation in the intermediate steps:  
A round transformation mainly realizes the function of Sub Bytes and Mix Columns with 32-bit columns. Four packets of round transformation are processed independently. Then the results of Mix Columns and the 32-bit keys sourced from Key expansion are combined by using XOR operators. Here, the round transformation is a module with 64 input ports (32-bit plaintext+32-bit key) and 32 output ports.

The function of Sub Byte is realized by Look-Up Table (LUT). It means that the operation is completed by the Find and Replace after all replacement units are stored in a memory (256x8bit = 1024 bit).

The implementation of Mix Column is mainly based on the mathematical analysis in the Galois field GF(28). Only the multiplication module and the 32-bit XOR module of each processing unit(one column) are needed to design, because the elements of the multiplication and addition in Galois

field are commutative and associative. Then the function of Mix Column can be achieved.

In the proposed work, the S-Box is implemented by a LUT having 8 bit address (256 addresses) and a data width of 8 bit. This implementation gives higher throughput for the design by significantly decreasing delay in data path. As a result the proposed design takes lesser number of slices when compared with other combinational technique proposed.

Fig.6.is a block diagram for the introduction of pipelining technology used in the round transformation.

In the process of pipelining, the 128-bit data is divided into four consecutive 32-bit packets that take round transformation independently. The operation of the above four groups of data can be realized in pipelining technology. In brief, it can be described as follow: store the unprocessed data in the 128-bit register, and control the clock for re-starting the 128-bit register to read the new data when the four groups' operations have been overcome. Thus the 128-bit round-operating unit has been transformed into four 32-bit round-operating elements. The internal pipelining processing should be implemented during the whole nine intermediate Round Transformations of the four packets before achieving the 128-bit ciphertext.

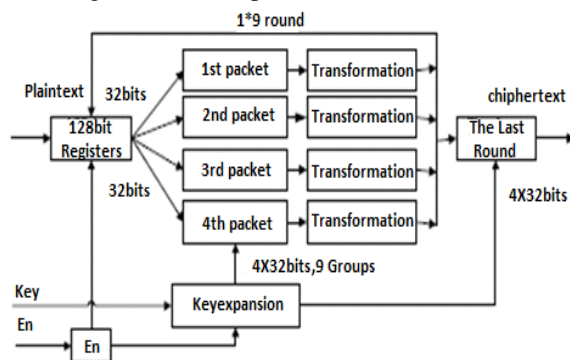


Fig.3.5. The round processing with pipeline technology

- The process of the last round

The final round is a 128-bit processor. After nine rounds of operations included Shift rows, Sub Byte and Mix columns, the 128-bit intermediate encrypted data will be used in XOR operation with the final expanded key(4\*32bit), which is provided by the key expansion module. The output of final round in the processor is the desired 128-bit cipher text. Similarly, the cipher text is divided into four packets of 32-bit data by an external enable signal.

- Key expansion and Key extraction

This module is implemented basically the same with the traditional way as another part of the AES

encryption algorithm. The only difference lies on the mode of data transmission. The initial key and expanded keys are divided into four 32-bit data before being extracted.

#### IV. Decryption

In this Decryption algorithm which includes : Inverse bytes substitution (InvSubBytes), the Inverse row shifts (InvShiftRows), Inverse column mixing (InvMixColumns),and the round key adding (AddRoundKey). Exclusive-OR operation is an inverse of itself, so there is no need for specific InvAddRoundKey transformation the same AddRoundKey operation is used for both encryption and decryption rounds .In the proposed work the Mix Column encryption hardware uses two of such ROM for Galois multiplication of '2' and '3' and for performing 4-Input XOR operation in Mix Column operation, the proposed design use 16 x 1 ROM with the result that Mix Column operation offers higher speed and uses minimum number of slices in the hardware (FPGA).

The decryption unit also uses same design approach for the entire architecture and decrypt the given cipher back to original text. Inverse S-Box architecture uses the same design of S-Box. Entry of LUT is changed according to Inverse Sub Byte transformation. Mix Column operation is implemented using 256X8 ROM. Four such ROMs are designed for the Galois multiplication of 9, 11, 13 and 14. 4-Input XOR operation is designed by 16x1 ROM. Architecture of Decryption module is same as encryption module with all complimentary functions of encryption. Decryption unit contains an extra register for storing Round Keys. Storing key is important since first round decryption use tenth round key and second round use ninth round key and so on.

#### V. Simulation Result

In our test case we have taken 16 byte data by the key board

Input = [36 46 e6 a8 88 5a 30 8c 28 31 98 a2 e0 37 07 34].

Cipher Key= [2b 7e 15 16 28 ae d2 a6 ab f7 15 88 09 cf 4f 3c].

Then after ten rounds of the AES the cipher text will appear as

Cipher text= [27 37 c1 82 83 29 a4 f1 43 93 9c 5e a6 b0 7c e1]

as shown in Fig. 5.1. For decryption we use cipher text as input and use the same cipher key for decryption algorithm and find

original data= [36 46 e6 a8 88 5a 30 8c 28 31 98 a2 e0 37 07 34] ( Fig. 5.2) .

This decrypted data is sent to the PC through an RS232 port and been verified using the hyper terminal interface .



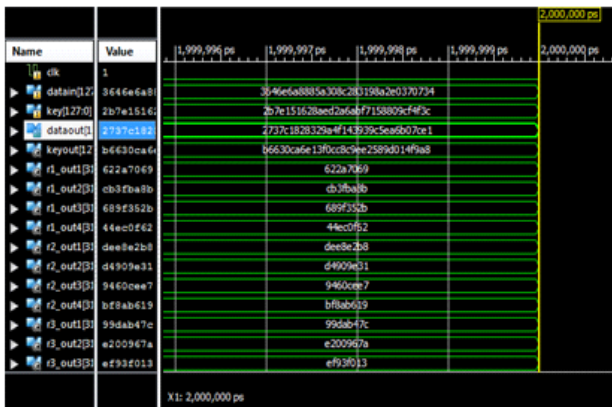


Fig.5.1 Simulation of AES encryption

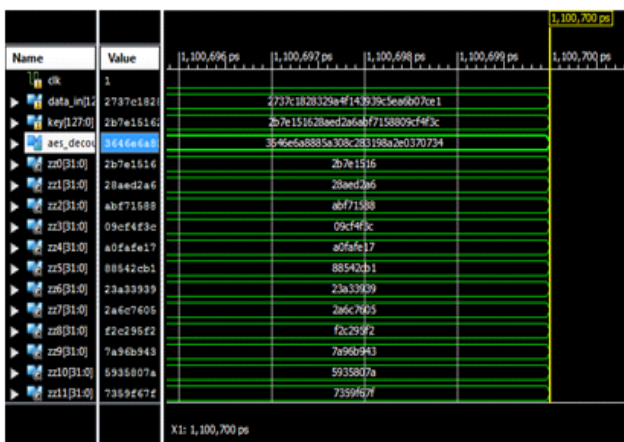


Fig5.2.Simulation of AES decryption

## VI. CONCLUSION

The aim of this proposed design is to perform a real time data communication exhibiting a significant level of security and providing a faster processing time where necessary. The bit length of the input, key used in our experiment is 128 bit and the result is obtained successfully. After being coded with Verilog Hardware Description Language, successfully get the result, the design with the pipelining technology and special data transmission mode can optimize the chip area effectively. Meanwhile, this design will reduce power consumption to some extent, for the power consumption is directly related to the chip area. Therefore the AES algorithm encryption and decryption device will implemente in this method can meet some practical applications. As the S-box is implemented by look-up-table in this design, the chip area and power can still be optimized.

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