RESEARCH ARTICLE

OPEN ACCESS

"Efficient Noc Architecture with CDMA Switch"

Prajakta Arunpant Kherde*, Prof. Sunil R. Gupta**

*Dept. of Electronics Engineering, J. D. College of Engineering, Nagpur prajaktagahukar@gmail.com **Dept. of Electronics Engineering, J. D. College of Engineering, Nagpur

Abstract

The Network-on-Chip (NoC) concept has been proposed to replace conventional bus-based system architectures. It will create scalable and flexible future SoC designs. A 2D-mesh topology is one of the most frequently mentioned topologies for a NoC design due to its natural layout mapping onto SoC. However, the 2D-mesh topology has a hot-spot problem at the center of the network and presents difficulties in multicasting. In this research work, it is proposed to use mesh-star hybrid NoC. It will remove problem of conventional 2D mesh topology. A novel multicastable CDMA switch is used for multicasting. The proposed switch connects 4 PEs and 4 links. The switches can unicast and multicast packets between the PEs which are directly connected to it. Also, the switch can unicast and multicast packet from other conventional 2D-mesh switches into group. This will remove the hot spot problem and increase network efficiency. Warmhole switching is proposed to reduce switch complexities. This approach leads to reduced traffic at the center of the network and better performance with multicasting

Keywords: CDMA, 2D mesh, NoC, PE's, SoC.

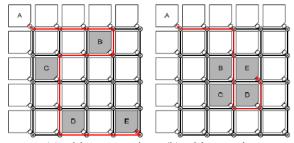
I. Introduction

As ITRS reported, gate delay is decreasing as technology scales, but global wire delay is increasing exponentially[1]. Network-on-Chip (NoC) concepts have emerged to resolve the limitations of conventionnal bus-based systems in terms of scalability and high throughput requirements[2]. Recently, many researchers have proposed a variety of NoC structures to reduce wire delay. In NoCs processing elements (PEs) such as CPU, DSP, I/Os, ASICS and memories are interconnected by switches based on specific topologies and communicate by routing packets[3].

By using NoC, disadvantage of bus is removed and also provide multicasting in a natural way[4]. The 2D-mesh topology is one of the most frequently considered NoC topologies because of its direct mapping and layout onto a chip. However, applying multicasting concepts to a 2D-mesh network poses challenges[5]. Researchers have proposed multicasting methods for a 2D-mesh network but with the primary focus being the avoidance of deadlock[6]. Code Division Multiple Access (CDMA)-based NoC techniques have been introduced, but the conventional CDMA switch does not support multicasting and cannot be directly connected to a 2D mesh network[7]. Due to its good performance and small buffering requirement, wormhole switching is being considered as a main network flow control mechanism for on-chip networks. Wormhole switching for NoCs is challenging from NoC application design and switch complexity reduction[8]. The conventional 2D Mesh

topology has problem of hot spot at the centre of the network and presents difficulties in multicasting. To remove these problems, mesh star hybrid NoC is used in NoCs, conventionally meshed switches are used. These switches causes contention and increases hop count. To remove this problem, CDMA switch is used. In NoC using CDMA switch, problem of hot spot and contention is removed. Also, hop count to farthest PE is reduced [9].

II. Conventional Multicasting Concept



(a) without grouping (b) with grouping figure 1: example of basic multicasting on a 2d-mesh noc.

Fig. 1 (a) shows a 5x5 2D-mesh network. Assume that PE A has a packet to be delivered to PEs B, C, D and E. Without the support of multicasting, PE A must unicast the same packet to each destination four times. This series unicasting of the same packet will increase both network traffic and the chances of contention. A basic multicasting method shown in Fig. 1 (a) is for PE A to first transmit a packet to PE B, then to PE C, then to PE D

and finally to PE E. Compared to series unicasting, this method will reduce network traffic. However, the packet still has a long distance to travel from the source PE to the final destination PE. Another, problem is that the packet is not delivered to all destinations at the same time. If the packet is real-time data and requires time-sensitive processing, then these different arrival times could pose a significant difficulty at the system level.

Fig. 1 (b) illustrates that PEs B, C, D and E are placed closer together at the center of the network and PE A is multicasting a packet to the group of PEs. We can reduce the total multicasting hop count by placing the multicasting destinations closer. Therefore, if frequent multicasting to a group is required, then place the PEs in the group closer to each other. If we place the frequently communicating group at the center of the network, then their frequent communication would increase the chances for contention because the traffic load at the center of an ordinary mesh network is much higher than average. If we place the group at the corner of the 2D-mesh network, then we would reduce this problem. However, in that case the hop count to the farthest PE will increase.

It is proposed to use novel CDMA switch and efficient mesh-star hybrid architecture for NoCs[9].

III. Proposed Architecture

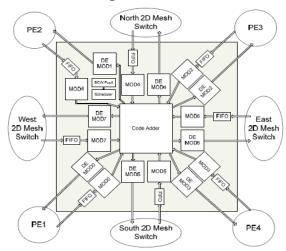


figure 2: block diagram of the proposed switch

Fig. 2 shows the block diagram of the proposed switch. Eight modulator and demodulator sets are connected through the code adder. Four modulators and demodulators are connected to each other through conventional 2D-mesh switches. The other four modulators and demodulators are connected to four PEs. A packet can be delivered to one PE or to multiple PEs which are connected to this switch. Any PEs which are directly linked by this

switch can unicast or multicast a packet to each other. Binary Walsh codes are used for this switch

3.1 Packet Format

47	76		3 2 1	C)
DATA		X	Y	R	DLD

Figure 3: packet format for the network

Packet format used in this research work is shown in fig. 3. In this packet, bits 0 and 1 are DLD field, bit 2 is request bit. Bit 3 to 6 are destination X and Y address and bit 7 to 47 are data bits.

3.2 Routing

In the proposed switch, XY routing algorithm is used, where X and Y represents the X-address and Y-address respectively. Each switch in the network has its own X-address and Y-address. If X and Y address of packet match with those of switch, then packet is sent to that PE which is connected to the switch. SX and SY represents source X and source Y address, DX and DY represents destination X and destination Y address, CX and CY represents current X and current Y address respectively.

e.g If data is to be sent from PE(0,0) to PE(3,3), then routing is performed in following manner as shown in table 1.

TABLE 1: ROUTING DIRECTION

SX, SY	DX, DY	CX, CY
0,0	3,3	0,0
0,0	3,3	1,0
0,0	3,3	2,0
0,0	3,3	3,0
0,0	3,3	3,1
0,0	3,3	3,2
0,0	3,3	3,3

In shown in the above table, packet first goes from 0,0 to 1,0, then to 2,0 and then to 3,0. In this manner packet address is first checked in x direction and then in y direction.

In the proposed CDMA switch, there are four processing elements and four convential mux switches. Addresses of these PEs and switches are as shown in the table 2.

TABLE 2: PEs AND SWITCHES ADDRESSES

PE/Switch	Address
PE1	0000
PE2	0001
PE3	0010
PE4	0011
West	0100
East	0101
North	0110
South	0111

3.3 Modulation and Demodulation:

Analogue modulation is used in the proposed system. In the process of modulation, first the data is multiplied by 3 and then divided by 2. In the process of demodulation, reverse process is followed. Data is first multiplied by 2 and then divided by 3, to recover the original data.

IV. Mesh Star Hybrid Noc:

Fig. 4 illustrates a multicasting example in the mesh-star hybrid NoC. We placed the CDMA switch inside of the dashed circle. Four PEs, B, C, D and E, are directly connected by the switch. Also, four conventional 2D-mesh switches are linked through the switch. One benefit of this architecture is that links are not utilized when PEs that are directly connected to the switch are communicating with each other, freeing them up for other traffic. This can lessen the hot spot problem at the center of the network. Another benefit is that it can reduce the multicasting hop count. Comparing Fig. 1 (b) and Fig. 4, we can see that the PEs in gray are at the same positions. However, the PEs in Fig. 4 have a reduced multicasting hop count, which increases network efficiency. Also, the multicasting data is delivered at the same time at the destinations, which is important in real-time or time-sensitive applications.

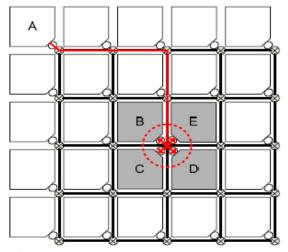


figure 4: 5x5 2d mesh-star hybrid noc

V. Results

5.1 Comparison Results

TABLE 3: COMPARISON BETWEEN 2D-MESH AND HYBRID NOC

		1	
	2D	2d	%
	Mesh	Mesh	Improv
		Star	ed
		Hybrid	
Min hop in group	2	1	50
Max hop in group	3	1	67
Min hop to the most	7	5	29
far PE from the group			
Min total hop for	5	2	60
multicasting from the			
most close PE which			
is located out of the			
group			
Min total hop for	8	5	38
multicasting from the			
most far PE which is			
located out of the			
group			
Occupy link during the	Yes	No	-
communication within			
group			
Multicasting data	No	Yes	-
arrive at the same time			
to the group			

Table 3 compares Fig. 1 (b) with Fig. 4. As can be seen from the table, we can minimize the hop count and reduce network traffic by using the proposed switch. Here we use only one CDMA switch; however, if it is required, we can include several CDMA switches in an NoC. Also, we can increase or decrease the number of PEs which are directly connected to the switch based on the requirements of an application.

5.2 Synthesis Results.

Table 4. Synthesis Results.

- 110 - 2		
Combinational area	9577.50 μm ²	
Non combinational area	3192.50 μm ²	
Total cell area	12770 μm ²	
Delay	2.946 ns	

A UMC 0.09 μm CMOS technology high-speed ASIC library was used for logic synthesis. The synthesis results for our proposed switch are presented in Table 4.

VI. Conclusion

In this paper, we have presented a novel multicastable CDMA-based switch and associated hybrid NoC based on the 2D-mesh and star topologies. The proposed switch connects 4 PEs and 4 links. The switch can unicast and multicast data between the PEs which are directly connected to it. Also, the switch can unicast and multicast packets from other conventional 2D-mesh switches into the group. This approach can mitigate the hot spot

problem of the network and increase network efficiency. As this novel switch requires less cell area and also delay is minimized, the efficiency of the network is highly improved.

References

- [1] http://www.itrs.net/
- [2] M. D. Osso, G. Biccari, L. Giovannini, D. Bertozzi and L. Benini, "Xpipes: a latency insensitve parameterized network-on-chip architecture for multi-processor SoCs" IEEE ICCD, pp.536-539, 2003.
- [3] K. Goossens, J. Dielissen and A. Radulescu, "Æthereal network on chip: Concepts, architectures and implementation," IEEE Design Test Comput., pp.414-421, 2005.
- [4] T. Bjerregaard and J. Sparso, "A router architecture for connection oriented service guarantees in the MANGO clockless network-onchip." In Proceedings of the Design, Automation and Test in Europe Conference, vol. 2, pp. 1226–1231, 2005.
- [5] S. Vangal and J. Howard, et al., "An 80-Tile 1.28 TFLOPS Network-on-Chip in 65nm CMOS," ISSCC, pp 98-99, 2007.
- [6] X. Lin, P. K. McKinley, and L. M. Ni, "Deadlock-free multicast wormhole routing in 2-D mesh multicomputers," IEEE Trans. on Parallel and Distributed Systems, vol. 5, no. 8, pp. 793–804, 1994.
- [7] D. Kim, M. Kim and G.E. Sobelman, "CDMA-Based Network-on-Chip Architecture" IEEE APCCAS, pp. 137-140, 2004
- [8] Zhonghai Lu, "Using Wormhole Switching for Networks on Chip: Feasibility Analysis and Microarchitecture Adaptation" Stockholm 2005, Thesis submitted to the Royal Institute of Technology in partial fulfillment of the requirements for the degree of Licentiate of Technology.
- [9] W. Lee and G. E. Sobelman, "Mesh-star hybrid noc architecture with cdma switch," in *IEEE Proc. of International Symposium on Circuits and Systems*, 2009, pp. 1349–1352.
- [10] Daewook Kim, Manho Kim and Gerald E. Sobelman, "CDMA Based Network On Chip Architecture" in *IEEE Asia Pacific Conference on Circuits and Systems, pp.* 137–140, 2004.
- [11] Daewook Kim, Manho Kim and Gerald E. Sobelman, "Design of high performance scalable CDMA router for on-Chip Switched Network" in *ISSOC*, 2005, pp. 32–35.

- [12] Ankur Agarwal, Florida Atlantic University, Boca Raton, Cyril Iskander, Hi-Tek Multisystems, Canada, Ravi Shankar, Florida Atlantic University, Boca Raton, "Survey of Network on Chip (NoC) Architectures & Contributions" in the journal of Engineering Computing and Architecture ISSN 1934-7197 Volume 3, Issue 1, 2009.
- [13] Jun Ho Bahn, Seung Eun Lee and Nader Bagherzadeh, "On Design and Application Mapping of a Network-On-Chip (NoC) Architecture" in *Parallel Processing Letters*. 01/2008; 18:239-255.
- [14] Xin Wang, Jari Nurmi "An On-Chip CDMA Communication Network" in *Proceedings International Symposium on System-on-Chip*; 12/2005.
- [15] Manho Kim, Daewook Kim and Gerald E. Sobelman, "Adaptive Scheduling for CDMA-Based Networks-on-Chip" in *IEEE-NEWCAS Conference, The 3rd International*; 07/2005.
- [16] Ik-Jae Chun, Tae-Moon Roh, and Bo-Gwan Kim, "Binary-Truncated CDMA-Based On-Chip Network" in *IEEE International Symposium on Circuits and Systems(ISCAS)*, pp. 397-400, 2007
- [17] Daewook Kim, Manho Kim and Gerald E. Sobelman, "FPGA- based CDMA Switch for Networks on-Chip" in 13th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2005), 17-20 April 2005, Napa, CA, USA, Proceedings; 01/2005.
- [18] Xin Wang, Tapani Ahonen, and Jari Nurmi 'Applying CDMA Technique to Network-on-Chip" in *IEEE transactions on very large scale integration (VLSI) systems, Vol. 15, NO. 10, October 2007.*
- [19] Jun Ho Bahn, Seung Eun Lee and Nader Bagherzadeh "Design Of Router for Network on Chip" in *International Journal on High Performance System Architecture*, Vol. 1, No.2, 2007.
- [20] Israel Cidon and Idit Keidar, "Zooming in on Network-on-Chip Architectures" in Technion Department of Electrical Engineering, Tech. Rep. CCIT 565, Dec. 2005.
- [21] Kun-Lin Tsai, Feipei Lai, Chien-Yu Pan, Di-Sheng Xiao, Hsiang-Jen Tan and Hung-Chang Lee, "Design of Low latency on-chip communication based on hybrid NoC Architecture" 978-1-4244-6805-8/10 ©2010 IEEE