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Nios II Based System for the Playing of Wave Files on Cyclone II FPGA.

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Abstract –
The motivation behind this study is the impact made on today's social media by music players, which include features like portability, size and equalizer functionality for the best possible sound output quality. The objective of this study is to develop a system that reads the wave files present on the Secure Data (SD) card, adjust the equalizer settings incorporated on it, and play them on the speaker with the best possible quality sound output. This can be done with the help of the SD card slot provided on the DE2 board, and its implementation on the board using Altera's SoPC (System-on-a-Programmable-Chip) Builder in the Altera Quartus 9.1 environment. Nios II is a 32-bit soft-core embedded processor architecture designed specifically for the Altera family of FPGAs. Programming of the Nios II processor will be done using the Nios II 9.1 IDE tool.
Index Terms – Embedded processor, Nios II embedded design, SoPC builder, and system on a programmable chip builder.

I. INTRODUCTION

Indicative of the popularity of being able to read wave files on SD (secure data) cards, there is no shortage of entries in the literature, on blogs and discussion boards, and postings of schematics. In this study, though, the authors address design advancements of the DE2_SD audio board in accordance with conceptual design methods [1-3] offering extended user control with features such as pause, reset and start, and with the implementation of switches an equalizer. The objective of this study is to develop a system that reads the wave files present on the SD card and plays them on the speaker with the best possible quality sound output.

1.1. SOPC BUILDER

A new technology has emerged that enables designers to utilize a large Field Programmable Gate Arrays (FPGA) that contains both memory and logic elements, along with a processor core to implement a computer and custom hardware for system-on-a-chip (SOC) applications. This approach has been termed as system-on-a-programmable chip (SOPC). SOPC Builder is a powerful system development tool which enables one to define and generate a complete system-on-a-programmable-chip (SOPC) in much less time than using traditional, manual integration methods. The designing technology of SOPC is the products of the modern computer-aided design technology, the EDA technology and the great development of large scale integrated circuit technology. SOPC technology is a completed electronic system, including the embedded processor system, the port system and the hardware acceleration or co-processors systems, the DSP systems, digital communication systems, the storage and general digital circuit system. It is embedded in a single FPGA to achieve the design of the circuit. SOPC Builder automates the task of integrating hardware components [4]. It reduces the task of manually writing HDL modules to wire the components of the system. Once the system components are specified in a Graphical user Interface (GUI), the SOPC Builder automatically generates the interconnect logic [5].Sensor network research began, like many of today's technological advances, with the military in such applications as battle-field surveillance and enemy tracking. After the technology proved itself, it quickly spread to civilian applications such as data centers, industrial settings and environmental observation and forecasting. However, due to non-standard communications protocols and electrical properties, sensor networks tend to be expensive, in spite of their broad use for Internet Protocol (IP) and platforms such as Hyper Text Transfer Protocol (HTTP), Simple Mail Transfer Protocol (SMTP) and Simple Network Management Protocol (SNMP) [6].

1.2. SOPC COMPONENT

A SOPC Builder component is a hardware design block available within SOPC Builder that can be instantiated in an SOPC Builder system. These are the following types of components in an SOPC Builder system:

1. Components that include their associated logic inside the SOPC Builder system.
2. Components that interface to logic outside the SOPC Builder system [10].

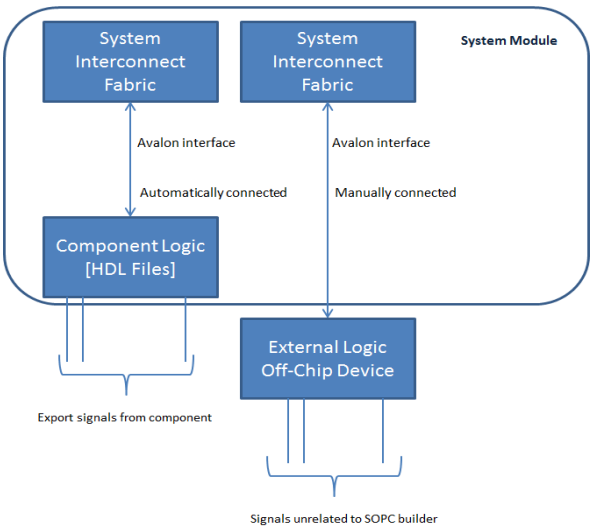

Figure 1: SoPC Components

1.3. NIOS II PROCESSOR

The Nios II processor is a configurable soft-core processor that allows features to be added or removed on a system-by-system basis to meet performance requirements. Users can configure the Nios II processor and add peripherals to meet their specifications, and then program the system into an Altera FPGA. On this single Altera chip or Nios II processor core the user can implement both peripherals and memory (both on- and off-chip). Such a system is similar to a microcontroller or computer on a chip having a CPU.

1.4. DESIGN FLOW

While there are CAD tools available commercially, which are available to the user for either their HDL or schematic design entry methods, manufacturers of FPGAs such as Altera (Quartus II) and Xilinx (ISE) provide such tools through their own software packages. These tools actually help step the designer through the process as follows:

- Package your component for SoPC Builder using the Component Editor.
- Simulate at the unit-level, possibly incorporating Avalon BFMs (Bus Functional Models) to verify the system.
- Complete the SoPC Builder design by adding other components, specifying interrupts, clocks, resets, and addresses.
- Generate the SoPC Builder system.
- Perform system-level simulation.
- Constrain and compile the design.
- Download the design to an Altera device.
- Test the design on the hardware.

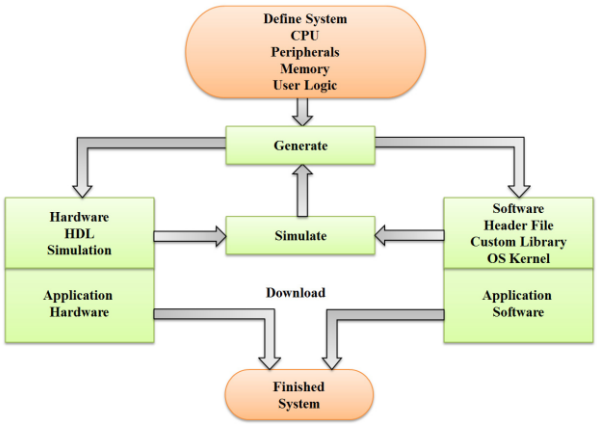

Figure 2: SoPC Design Flow

1.5. AVALON SWITCH INTERCONNECT

The system interconnect fabric is the collection of interconnect and logic resources that connects Avalon- MM master and slaves on components in a system. SOPC Builder generates the system interconnect fabric to match the needs of the components in a system.

System interconnects fabric for memory-mapped interfaces support the following:

1. Any number of master and slave components. The master-to-slave relationship can be one-to-one, one-to-many, many-to-one, or many-to-many.
2. On-chip components.
3. Interfaces to off-chip devices.
4. Master and slaves of different data widths.
5. Components operating in different clock domains.
6. Components using multiple Avalon-MM ports [5].

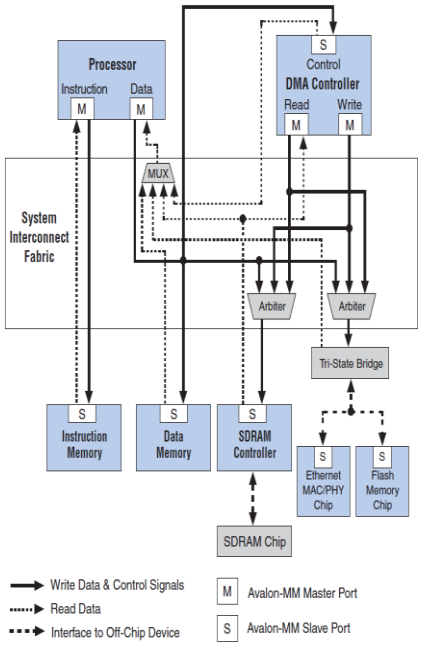

Figure 3: System interconnect fabric

1.6. AUTOMATED SYSTEM GENERATION

SOPC Builder system integration tools automatically perform the process of configuration of the processor features; hence the hardware of the design is produced that is used to program an Altera device. The graphical use interfaces (GUI) help in structuring of Nios II systems with multiple peripherals and memory interfaces (Fig. 4). After system generation, you can download the design onto a board, and debug the software executing on the board.

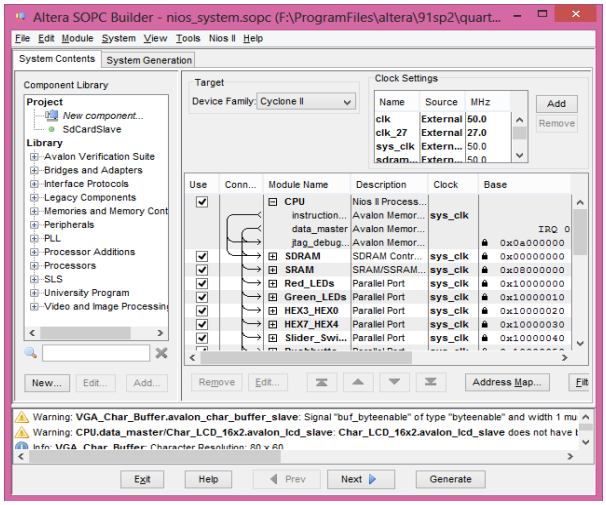

Fig. 4: SOPC Builder

II. NIOS II PROCESSOR

This 32-bit soft-core processor architecture was developed by Altera Corporation. The older Nios was introduced in 2001 and was industry's first viable commercial processor created specifically for embedded system design in FPGAs. Nios II can be embedded directly into FPGAs, which allowed for performance of more than 200DMIPS, and users can select more than 60 IP cores [7]. It also allows designers to include the available IP (Intellectual Property) modules during the design phase, which saves a lot of time [8]. The soft-core nature of the Nios II processors let designers integrate custom logic into the arithmetic logic unit (ALU) (Figure 5). The Avalon Switch Fabric (ASF) is one of the key features that differentiate the cyclone FPGA from other vendors' FPGA products. ASF is a high-bandwidth interconnects structure that offers greater flexibility than a shared bus. The switched interconnect structure of the ASF connects the master and slave ports. Nios II implements the function of the control and interpolation algorithm and the communication between the computer and the FPGA [9].

	Nios II Family: Cyclone II	Performance at 50 MHz	Logic Usage	Memory Usage
Nios II/e	**RISC** **32-bit**	Up to 5 DMIPS	600-700 LEs	Two M4Ks (or equiv.)
Nios II/s	RISC 32-bit **Instruction Cache** **Branch Prediction** **Hardware Multiply** **Hardware Divide**	Up to 25 DMIPS	1200-1400 Les	Two M4Ks + cache
Nios II/f	RISC 32-bit Instruction Cache Branch Prediction Hardware Multiply Hardware Divide **Barrel Shifter** **Data Cache** **Dynamic Branch Prediction**	Up to 51 DMIPS	1400-1800 LEs	Three M4Ks + cache

Figure 5: Nios II core configuration

1) Nios II/f Core (Fast)

The Nios II/f core is a high-performance device with limited core size. Limiting the core size is the tradeoff for the faster execution times. If neither a memory management unit (MMU) nor a memory protection unit (MPU) is included, the Nios II/f ends up being about 25% larger than the Nios II/s core. The Nios II/f is designed to maximize the instructions-per-cycle execution efficiency, optimize interrupt latency and maximize f_{MAX} performance of the processor core.

2) Nios II/s Core (Standard)

For medium-performance applications requiring only a small core while not sacrificing performance the Nios II/s core is a logical choice. In this case, execution performance is reduced in order to conserve on-chip logic and memory resources. This standard core uses roughly 20% less logic than the fast core, but at the expense of about a 40% drop in execution performance [7].

3) Nios II/e Core (Economy)

For designs needing to reduce resource utilization to a minimum while still maintaining hardware resources the Nios II/e core is designed with the smallest possible core size. This is the smallest core size available that still retains compatibility with the Nios II instruction set architecture. This economy core is about half the size of the standard core, but with significantly reduced execution performance.

NIOS II SYSTEM ON ALTERA'S DE2 BOARD

The Nios II processor and many other components such as standard peripherals and custom peripherals are used for the formation of a total system that can be integrated into a Nios II system on Altera's DE2 board .

The process of interfacing the Nios II processor and peripherals to the DE2 board chips is enabled on the Cyclone II FPGA chip. The interconnection network connecting these components in the FPGA chip is called the Avalon Switch Fabric (Fig. 6).

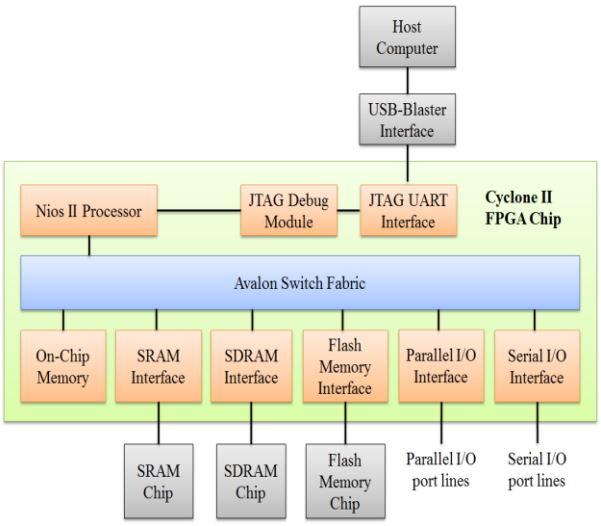

Fig. 6. Nios II system implemented on the DE2 board

III. PROPOSED DESIGN FOR THE PROJECT

A personal computer (PC), running Quartus II software with the SoPC Builder environment, and the Nios II soft-core processor will be using for developing the proposed system [11]. After the SD card is inserted into the receiving slot on the DE2 board, the program present on the Nios II processor is initialized and plays the music files—.wav formatted—on the speakers attached to it with the best possible sound quality [12]. Using a Nios II processor-based system on the FPGS, the software is configured on the development board with Nios II standard hardware system, and then executed to create the FPGA configuration file, i.e., the SRAM Object File(.sof). This file containing the Nios II standard system is downloaded to the board. The Eclipse IDE environment is here the software part will be developed in C language. The Eclipse environment has a C/C++ compiler and a set of powerful commands, utilities and scripts for building options for applications, board support packages, and software libraries. Nios II Software Build Tools for Eclipse focuses on improving software productivity for large software applications and team-based software designs.

BLOCK DIAGRAM OF THE PROPOSED SYSTEM

The block diagram provided in Fig.7 shows the implementation of the proposed application.

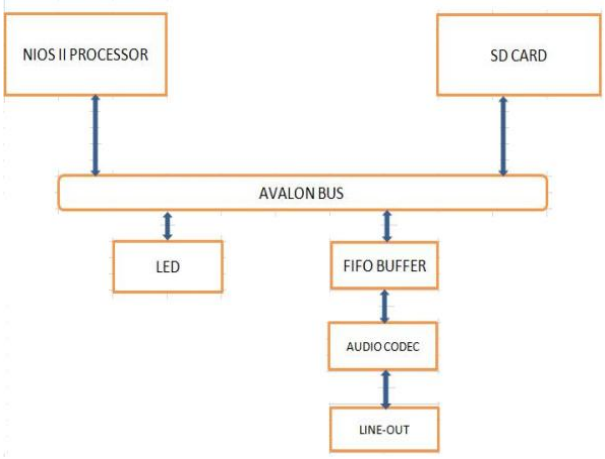

Figure 7: Block diagram

SD CARD CONTROLLER

The SD card serves as the memory for the project and interacts with the SD card controller. For this to exchange to occur, file system on the SD card must be FAT 16 formatted—meaning that the smallest data words should be 16 bits long—and that the FAT16 partitions the data into blocks of data, each of which is 512 bytes.

Fig.8. SD card

AUDIO CODEC

Audio Codec—located between the Buffer and the Line-Out—is the part of the system where digital-to analog conversion (DAC) takes place in order for the music to play on the speakers [12]. The modules included in this system are:

- FIFO Module: This module is used to bridge the Nios and DAC. With a buffer size of 256 x 16, the data stream is serialized and moved from the Nios to the buffer.

- I2C Module: This module basically controls the flow
  of data in the Audio Codec.

- PPL Module: This module generates a clock frequency of 18.4 MHz.

IV. CONCLUSION

The objective of this study is to develop a system that reads the wave files present on the Secure Data (SD) card, adjust the equalizer settings incorporated on it, and play them on the speaker with the best possible quality sound output. The programming of the board can be done with the Nios II Eclipse, where the program functions in such a way that it displays the SD CARD Player on the LCD display initially and then reads the memory location of the wave files present in the SD card [13]. A data stream of 512 bytes is moved from the SD card onto the FIFO (First-In First-Out) Buffer. This stream of data is moved into the Audio Codec where digital-to-analog (DAC) conversion takes place at a rate of 16 bits and moved onto the Line-Out of the DE2 board. The I2C controls the flow of data between the FIFO buffer and the Audio Codec and sound can be heard on the attached speakers with the best possible sound quality.

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