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Design of Flash ADC using Improved Comparator Scheme

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ABSTRACT
This Paper introduced a 4 bit Flash Analog to Digital converter. The propose ADC consist of the comparators and the MUX based decoder. Propose Comparator eliminate the use of resistor ladder in the circuit. All the input of comparators are connected to the common input node. Depending upon the internal voltage of comparator and the input voltage output may be "0" or "1" known as thermometer code. This thermometer code is converted to the binary code using the MUX based decoder .This design eliminate the limitation of TIQ (Threshold Inverter Quantization) comparator. This ADC is design using the .25um technology and show the result of the proposed circuit as expected.
Keywords **-** Flash ADC , Comparator, MUX , Standard Cell,TIQ .

I. INTRODUCTION

Analog to Digital converter (ADC) are the most important device to convert analog information to corresponding digital forms. ADC are commonly used in the application area of mobile phones, cameras, digital TVs etc. Flash and pipeline ADCs are often used for high speed application. The flash type is the faster of the two , but not benefited to the higher resolution because it increase the no. of component and hence consume more power. Many flash ADCs architecture [1] [2] are described in the literature.

To improve the design of flash type converter several architecture have been proposed such as two-stage architecture [3] [4]. But the major issue with these approach is that it uses analog component and as the technology is scaling down analog component are difficult to integrate and its performance are also degraded. This adc also require high gain differential comparators that are more complex and require resistor ladder to deliver reference voltage. Other disadvantage of this approach are the reduction in throughput and poor differential linearity. But the performance of the digital system is improve as the technology is scaling. Currently simple and faster flash type converter are proposed on the TIQ technique (Threshold Inverter Quantization) [5] [6]. This technique eliminate the use of the resistor ladder and reduce the complexity of the converter but it is process parameter dependent . This uses two cascaded digital CMOS inverter in which first act as an analog voltage comparator and the second increase the voltage gain of the comparator. Reference voltage of the comparator is change by varying the width of the transistor and keeping the transistor length constant as it is more sensitive and has a significant effect on threshold voltage. Another technique is by using CMOS LTE (CMOS Linear Tunable Transconductance Element) as a comparator which improve the PSRR (Power supply Rejection Ratio) of the circuit. This technique is also process parameter dependent.

In this paper , we propose a Flash ADC that can be fully implemented using only standard cells. This approach helps to improve the high-speed conversion rate. This allows the designer to stay within the mature digital design flow and effectively reduce the risks and time-to-market. Other benefits of using this approach include speed and simpler design approach.
The rest of the paper is divided as follows. Section 2 introduce the design of ADC and introduce the basic concept of the decoder and Section 3 reports the transistor-level simulation of the proposed ADC. Finally the conclusion are given.

II. COMPARATOR DESIGN

The proposed architecture of 4 bit flash comparator is shown in Fig. 1. It consist of a different number of NAND and Nor gates . Let us consider a 4

input NAND and Nor gate. It require total $(2^N - 2) * (2^N - 1)$ no. of comparator, where N is the no. of bits.

Lets explain the principle operation of the K- input NAND (K=1,2,3,4) whose input are connected together .As the input are connected together then the all NAND and Nor operate as an inverter but the only difference is that threshold voltage of that are different. Threshold voltage of Nor is less than that of the NAND because in NAND gate , the NMOS network is in series and the PMOS network is in parallel.

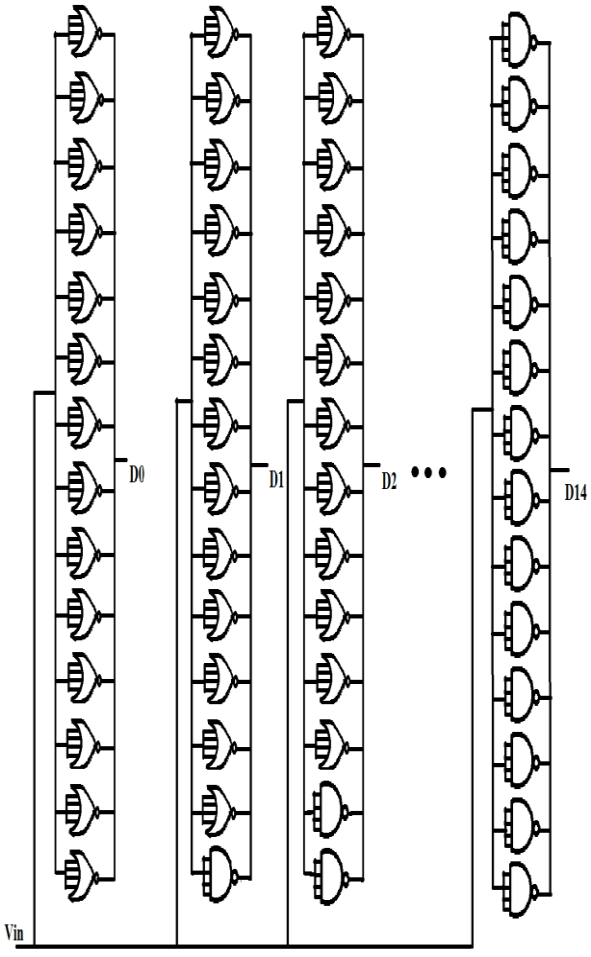

Fig 1 Proposed 4 bit flash ADC

The threshold of the NAND would be higher than that of the inverter, if the NMOS and PMOS has similar Vth and were sized to have identical μCox(W/L). This is because, as the PMOS network has parallel connection then it will generate more current and as the NMOS network has series connection it will generate less current for the same V_{GS}. For the current to be equal, the NMOS transistor would need to be higher V_{GS} which in turn increase gate threshold voltage. A similar reasoning can be applied to a NOR gate and the conclusion is that the threshold voltage is lower than that of the inverter.

Let us consider inverter, NAND and Nor and M be the number of NMOS transistor connected in parallel. Knowing the static gate are complementary , the P-network will have M transistor in series . The NMOS transistor can be replaced by a single transistor having the width M times that of the original transistor. Similarly, PMOS transistor can be replaced by the single transistor having the length M times that of the original transistor. Mathematically the threshold voltage of a gate calculated as being [7] [8]

$$V_{GTH} = \frac{V_{DD} - V_{TH} + M \cdot V_{TH}}{M+1}$$

Above Equation show that how the threshold voltage of a gate changes as a function of M. By using NAND and NOR gates with higher fan-in the value M changes which in turn changes the threshold voltage of the gate. It is therefore possible to create set of inverter having different threshold voltage to create a flash ADC using standard cells.

The DC characteristic of the comparator is shown in fig. 2 which indicate that the interval between the comparator are identical . As the interval is identical then there will be less chances of having missing code.

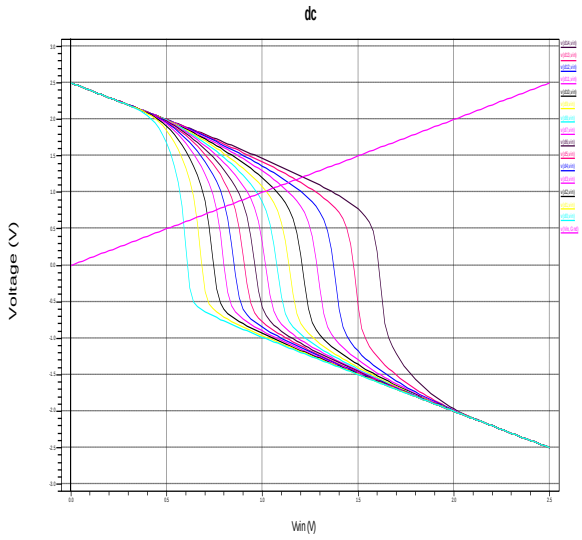

Fig 2 DC Response of Comparator

III. THERMOMETER TO BINARY DECODER

There are various type of Decoder to convert thermometer code output of the comparator to binary code. Some of the decoder are Rom Based Decoder,

Ones Counter Decoder, Fat Tree Decoder and Multiplexer based decoder.

3.1 ROM Based Decoder

Simple and straightforward implementation of thermometer to binary decoder is based on ROM – based structure [9] [10]. Thermometer code is provided to gray or binary encoded ROM. The appropriate row in the ROM m is selected by using the circuit that has the output of comparator m and the inverse of comparator m + 1 as input. The output is high if the output of comparator m is high and the output of comparator m+1 is low. The row m is selected by using a circuit say 2-input AND gate with output of comparator m & inverse of comparator m+1 as input. However multiple rows are selected if bubble error occurs. First order bubble error can be corrected using 3 input NAND gate . However advance schemes are available to reduce first & second order bubble error with reduced power consumption [11] [12]. Major disadvantage of ROM decoder is slow speed & large power consumption. Another disadvantage is that as the speed increases, more bubble errors are introduced and a more advanced bubble error correction scheme than the 3-input NAND is required. This further reduces the speed of the decoder as well as adds to the overall power consumption.

3.2 Ones Counter Decoder

The output of a Thermometer to binary decoder is the no. of digital ones on the input represented in binary code. This is similar to a bit swapping technique. Depending on the speed requirement suitable ones counter topology is selected. However for high speed implementation Wallace tree topology is the best choice. For high speed application the Wallace Tree topology in fig. 3 is a good choice. [10] [14]

The hardware cost for Wallace Tree decoder $\Gamma_{Wallace}$ in terms of 2:1 multiplexer cost Γ_{mux} is approximately [9] [15]

$$\Gamma_{Wallace} = 3 \sum_{i=1}^{N} (i - 1)\, 2^{N-I}\, \Gamma_{mux} \text{ ---------(1)}$$

Length of critical path in unit of propagation delay 2:1 multiplexer t_{Mux} is approximately [9][15]

$$t_{cpw} = (4N - 6)\, t_{Mux} \text{ ----------(2)}$$

From the above equ. Rough cost is estimated which show that the hardware cost and propagation delay of the Wallace tree decoder decreases as the resolution N decreases.

3.3 Fat Tree Decoder

A more power and delay efficient approach of converting thermometer to binary code is to use fat tree based decoder **[10]**. Fat tree structure has two stage. The first stage convert the thermometer code to the 1 out-of – 2^N – 1 code. The second stage convert the 1 out-of – 2^N – 1 code to binary code using multiple tree of OR gate. This result in reduced area and delay when compare with Wallace tree based decoder.

3.4 MUX Based Decoder

A Mux based thermometer to binary decoder is proposed in [9] [10] [14]. This decoder result in short critical path and small area. For N bit flash ADC most significant bit (MSB) of the thermometer to binary decoder output is logic one if more than half of the output in the thermometer scale is 1. Hence the MSB is same as thermometer output at level 2N - 1. To find the second most significant bit the original thermometer scale is divided into two partial thermometer scale separated by the output at level 2N-1. To find MSB-1 the appropriate partial thermometer scale must be decoded. If the value of MSB is 1 then upper partial thermometer scale is chosen otherwise the lower partial thermometer scale is chosen. The MSB-1 bit is decoded in the same as MSB i.e by assigning it the value of middle output in the selected partial thermometer scale. This decomposition is continued until all output bit are assigned the proper logic level.

As shown in fig. 3 the MSB bit is generated from thermometer output at place 2^{N-1}. This value is equal to eight for 4 bit resolution. The same output is act as a select line of MUX in the first decoder column . Hence if X_3 is 1 then upper part of thermometer scale is chosen as partial thermometer scale otherwise the lower part of scale is chosen . This is continued recursively until only one MUX is remain . this output is the LSB of the binary output of the decoder. Due to its regular structure of decoder it can be easily implemented for the higher resolution system. Fig. 3 show the implementation of MUX based decoder for 15 thermometer code input. It require less hardware and has a short critical path.

The decoder has a hardware cost [10] [15]

$$\Gamma_{\tilde{MUX}\,DECODER} = \Gamma_{MUX} \sum_{i=1}^{N-1} (2^{N-i} - 1) \text{ --------(3)}$$

The critical path in unit of t_{MUX} is [10] [15]

$t_{\_cp-MUX} = (N - 1)\, t_{MUX}$ ----------(4)

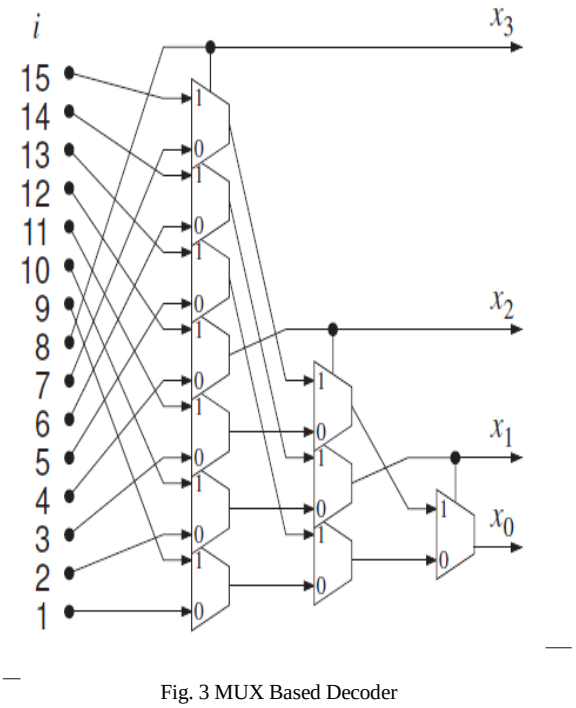

Fig. 3 MUX Based Decoder

IV. ADC DESIGN

The block diagram of the proposed flash ADC is shown in fig. 4. It consist of a Comparator , Gain Booster and MUX based Decoder block. In this the analog voltage are applied to the comparator , it compare the input voltage with the reference voltage .If the input voltage is less then reference voltage then the output of comparator is "1" otherwise "0". The series of code generated by the comparator is known as thermometer code. Then next is gain booster which increase the gain of the voltage and the output of this gain booster is given to the decoder which convert the thermometer code to the binary code.

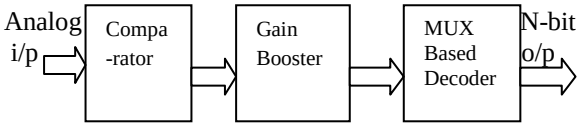

Fig. 4 Block Diagram of proposed flash ADC

V. SIMULATION RESULT

In this section simulation result of proposed 4 bit flash ADC is presented . To ensure the functionality of design, transient.

Fig 5 show the transient analysis of design and the lower plot of it show that the ramp voltage is introduced at the input for the simulation. The four upper plot show the output of ADC. The upper most plot is the most significant bit i.e the MSB bit , then lower then this is the MSB -1 below this is MSB-2 and the fourth one is the least significant bit i.e the LSB bit.

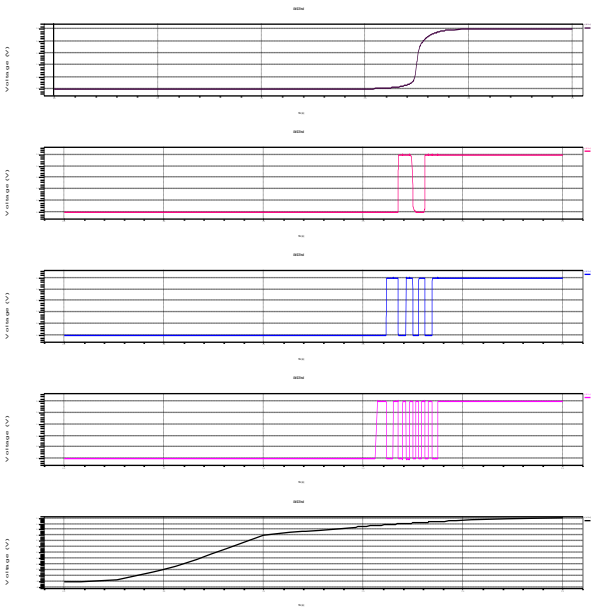

Fig.5 Transient Analysis of 4 bit ADC

VI. CONCLUSION

In this paper, we introduced a digital comparator for 4 bit flash ADC. In this fully resistive ladder reference circuit and analog comparator is removed. A comparators with different threshold voltage is obtained by using a parallel combination of NAND and Nor gate. Its implementation is fully compatible to standard digital CMOS technology. To test its functionality transistor level simulation have been done using Tanner 13 tool. Implementation of different thermometer to binary decoder shows that the MUX based decoder is more efficient. Mux based decoder require less hardware and the lower critical path when compared with others. Hence MUX based decoder is fast and compact for ADC implementation.

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