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Design of Multi-functional High frequency DDS using HDL for Soft IP core

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ABSTRACT
This work presents a highly integrated single chip multi-functional, multi- waveform signal generator which can generate various waveforms, such as sine wave, saw tooth wave, square wave, triangle wave, trapezoidal wave and so on with digital controller inside to adapt embedded and low power applications. The proposed system is composed by Spartan- II, DDS (Direct Digital Synthesis) and other peripherals. Required waveform can be generated by using DDS.Together with modern EDA tools, the system HW-SW codesign and FPGA implementation is accomplished,using typical SOPC design flow. The Avalon bus is used to connect peripheral modules (such as function switch buttons and 7-segment LED display units) to Spartan-II's bus main port (instruction and data control port). The realized system is flexible to reduce, extend, with low power consumption, and has System on Programmable Chip [SOPC] function which means the system's hardware & software is online programmable.
Keywords : DDS, SOPC, XILINX ISE, DAC

I. Introduction

A multi-functional high-efficiency generation of spectrally pure, wide-band, multi-carrier waveforms is a key objective in modern communication and radar applications. A high-efficiency signal generator is a device that can output various types of signal waveforms, such as sine wave, saw tooth wave, square wave, triangle wave, trapezoidal wave and so on. This goal can be achieved by direct digital synthesis (DDS) of high-frequency RF waveforms with high bandwidth and linearity. It would allow one to combine digitally multiple waveforms and then directly synthesize the composite RF signal. Maintaining the digital nature of the generated RF signal all the way to the power amplifier (PA) would be enabled by the use of new highly efficient high-speed semiconductor digital amplifiers.

It also would enable the implementation of digital predistortion at the RF level compensating for non-linearities of the amplifier chain. Such a Digital-RF architecture.Nowadays, there are two different approaches to implement such kind of signal generator: one approach is using Direct Digital Synthesizer (DDS) and FPGA for system control, plus high-speed D/A convertors. This method is expensive, although with good performance. The other one is using DDS designed by Hardware Description Language (HDL) or related soft IP core, plus waveform data storage memory and MCU to realize control function. In this approach, the DDS is implemented by downloading the synthesized HDL design to an FPGA chip. These methods can change traditional design flow in electronic systems by reducing separation of modules, improve speed, accuracy and reconfiguration. But there still have inconvenient and inflexible problems when adding peripheral devices such as MCUs or DDS chip, which make the system heterogeneous. [1][2] In order to design the fully digital multi-functional generator as a true SOPC system, we choose the solution using Cyclone II soft processor and Quartus II by Altera. The commonly used silicon solutions for SDR implementations are Field Programmable Gate Arrays (FPGA), Digital Signal Processors (DSP), General Purpose Processors (GPP) & Application Specific Integrated Circuits (ASIC). Shortcomings of ASIC design such as long design period, high investment, less flexibility can be removed with FPGA design. FPGA's offer best solution in IF stage because it provides high speed, high flexibility & low developmental cost, though it may have high power consumption due to insufficient use of FPGA logic elements (Slices) [5].

II. DDS Architecture

DDS architecture was first proposed by Tierney as shown in Fig. 1. The arithmetic operations required to built DDS are Phase

Accumulator which is basically a counter that increments its count value with every rising edge of clock and generates phase for sine or cosine waveforms and the increment is set by tuning word or Frequency Control Word M, Phase to Amplitude Converter PAC is implemented using Read Only Memory ROM Look Up Table approach. PAC produces a ramp whose slope is directly proportional to frequency control word.
The frequency control word is also called the jump size, the larger the jump size, the faster the phase accumulator overflows & completes its equivalent of a sine wave cycle.

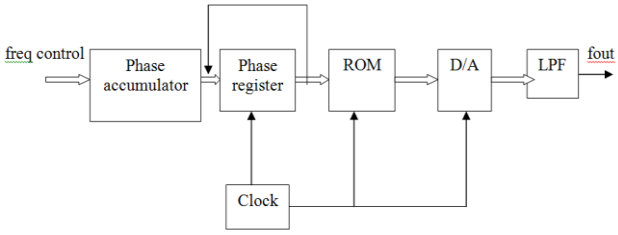

Fig.1. Basic scheme of DDS

2.1 Phase Truncation

Both frequency and phase information of DDS are completely stored in phase accumulator. The phase accumulator contents are interpreted as a portion of rotation around the unit circle & Phase to Amplitude Converter PAC produces approximated sinusoid amplitude of equivalent angles defined by the portion of circle. The simplest approach for phase to sinusoid amplitude converter is implemented as ROM LUT's. However to achieve frequency resolution requirements, a wide phase accumulator is often needed which not only requires large memory (LUT) but also large power consumption. Higher power consumption is due to large ROM size. so there is always a tradeoff to reduce the ROM Because a larger ROM size increases both access time (reduces speed) and power consumption, size without degrading the spectral performance of the DDS system.To reduce the LUT size, the number of entries in LUT is reduced by exploring the quadrant symmetry of sine function which consists of truncated N-M bits from phase accumulator, where M is the number of bits passed to LUT. However, truncation introduces spurious noise in the synthesis output. The simple equations that govern the operation of DDS where fclk is the reference clock frequency, fout is the output clock frequency & n is the width of the accumulator. Changes to the value of M results in the immediate & phase continuous changes in the output frequency. The only speed limitation to changing the output frequency of a DDS is the maximum rate at which the buffer register can be loaded & executed, thus enhancing frequency hopping capability of the DDS architecture. Phase truncation acts as a source of unwanted spur in the output spectrum. Also, the effect of DAC resolution results the spurious performance of the system. In the frequency domain, quantization distortion errors are aliased with Nyquist Band and appear as discrete spurs in DAC output spectrum.

2.2 Spurious Free Dynamic Range

Spurious Free Dynamic Range defines the ratio between the amplitude of wanted sinusoid and the amplitude of largest unwanted frequency component, is the parameter commonly used to characterize the DDS spectral purity. Phase truncation causes significant changes in the Spurious Free Dynamic Range of the output signal. Spurious performance is degraded approximately at the rate of 6dB/octave & the complete expression for

calculating SFDR is deduced as follows. Truncation of phase accumulator results in an error of the DDS output signal.
By the behavior of the truncation word, this error signal is characterized. The truncation word is the portion of phase accumulator which contains the truncated bits. SFDR is related to linearity and fault performance of a DAC. The quantization noise of the converter represents the limit on the overall dynamic range. The measurement, prediction and analysis of SFDR performance is complicated by a number of interacting factors. Even an ideal DAC can produce harmonics in a DDS system. The amplitude of these harmonics is highly dependent upon the ratio of output frequency to the clock frequency, the spectral content of the DAC quantization noise varies as this ratio varies. Thus, best SFDR can therefore be obtained by careful selection of clock and output frequencies. For the given application, the SFDR of a D/A converter needs to be specified over the full Nyquist bandwidth as well as over the band of interest. Thus, a complete picture of the converter's spectral performance and its impact to their system's performance can be obtained. Selecting a low glitch, linear converter helps to significantly reduce spurs. The source of spurious at the output of high speed DDS are of great interest to the DDS designer, since the spectral purity is one of the critical & challenging requirements in wireless applications such as Software Radios.

2.3 DAC resolution on Performance

Depending on the number of input bits , the resolution of a DAC is specified. For example, the resolution of a DAC with 10 input bits is referred to as having 10 bit resolution. The impact of DAC resolution is most realized by the sine wave reconstruction. The deviation between a DAC output signal and a perfect sine wave leads to the error introduced as a result of its finite resolution. This error is the quantization error that gives rise to the quantization distortion. The sharp edges in the DAC

output signal imply the presence of high frequency components superimposed on the fundamental. It is the high frequency components that constitute quantization distortion. In the frequency domain, quantization distortion errors are aliased within the Nyquist band and appear as discrete spurs in the DAC output spectrum. As the DAC resolution increases the quantization distortion decreases; i.e., the spurious content of the DAC output spectrum decreases. Thus, an increase in resolution results in a decrease in quantization error.

III. Proposed DDS design

The waveform may be a sine wave,. It can also be a saw-tooth wave, a triangle wave, a square wave, or any periodic waveform. We will assume that the sampling frequency *F*s is known and constant. Before proceeding with the theory of operation, we summarize methodology for DDS.

1) The tuning resolution can be made arbitrarily small to satisfy almost any design specification.

2) The phase and the frequency of the waveform can be controlled in one sample period, making phase modulation feasible.

3) The DDS implementation relies upon integer arithmetic, allowing implementation on virtually any microcontroller and digital logic for FPGA.

4) The DDS implementation is always stable, even with finite-length control words. There is no need for an automatic gain control.

5) The phase continuity is preserved whenever the frequency is changed (a valuable tool for tunable waveform generators).

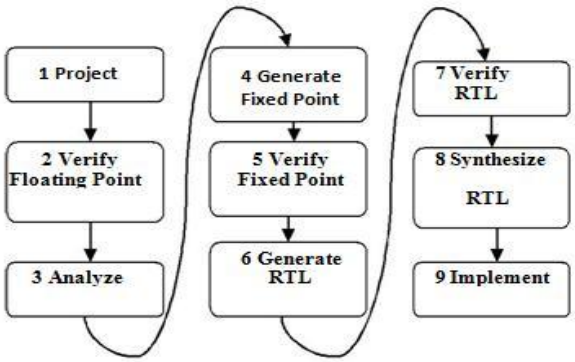

Fig.2. ISE Synthesis Design Flow

IV. Signal generation

Square wave:

The amplitude of the wave will be high for n/2 samples. Here we took high value as '127' corresponding to all ones. After n/2 cycles, the amplitude will be made low('0').

Saw tooth wave:

The amplitude should be increased to maximum for n samples and then reset to low. Maximum value is '127' and the low value is '0'. The rate of increase is inversely proportional to n value.

Triangular wave:

The amplitude has to incremented to maximum till n/2 cycles (from all zeros to all ones). After n/2 cycles, the value has to be gradually decremented to all zeros again.

Sine wave:

The generation of sine wave is the most critical part in creating a DDS signal generator. There are many methods available to generate sine wave. They are

1. Taylor series Approximation
2. Table lookup.

There are other methods available which are too complicated to implement in FPGA.

Taylor series Approximation

The Taylor series of the sine function is:

sin(x) = x - (x^3)/3! + (x^5)/5! - (x^7)/7! + ...

x is in radians. Since x value is in radians, x should be a floating value. Since we approximate the value, if we take more terms of this series, we get less error. For low values of x, we need only few terms. For higher values of x we need more terms. This kind of approach can be realized by hardware or FPGA. A serious disadvantage of this method is that it requires large no of multiplications to be done. So the hardware implementation is very large. So the cost of implementation is also high.

Look up table method

In this method, we first generate all the sine values for n samples and store it in a memory. In this method, we use the symmetric properties of sine wave. So we need to save only the values of sine wave from 0 to pi/2. This method yields very less error compared to other methods and the hardware realization is also simple

V. Memory requirement

So we chose this method to implement in the hardware. We chose n=512. Therefore we need to

store 512/4= 128 sample sine wave values. Because 2*pi/4= pi/2. So we need to store values from 0 to pi/2 only. Other values are generated by symmetric properties of sine wave. For intermediate values we can interpolate between two samples. The number of bits used to store the sample values are 8 bits. So memory needed 8x128 bits= 1024 bits = 128 bytes.

VI. Research Methodology

1. Design of RAM using Text IO
2. Design of ASync Counter
3. Write a VHDL code for waveform generation.
    1. Square wave
    2. Saw tooth wave
    3. Sine wave
    4. Triangular wave
    5. Mixture of square wave and sine wave
    6. Mixture of saw tooth wave and sine wave
    7. Mixture of triangular wave and sine wave
    8. Select entity for different wave form generation
    9. Integrate all to form a DDS.

1.Counter

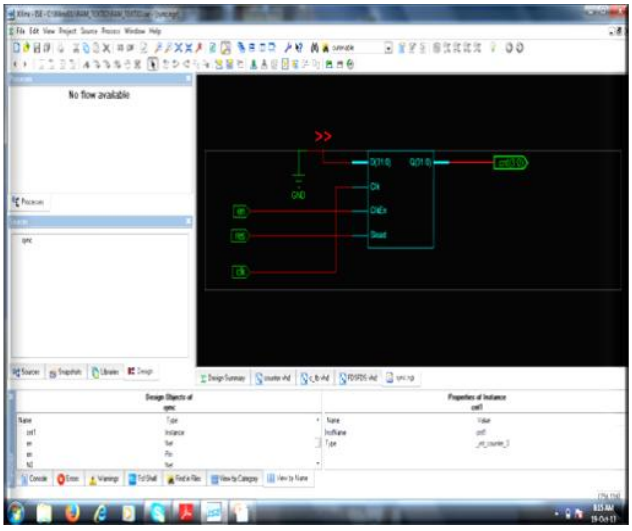

Fig. 3 RTL of Counter

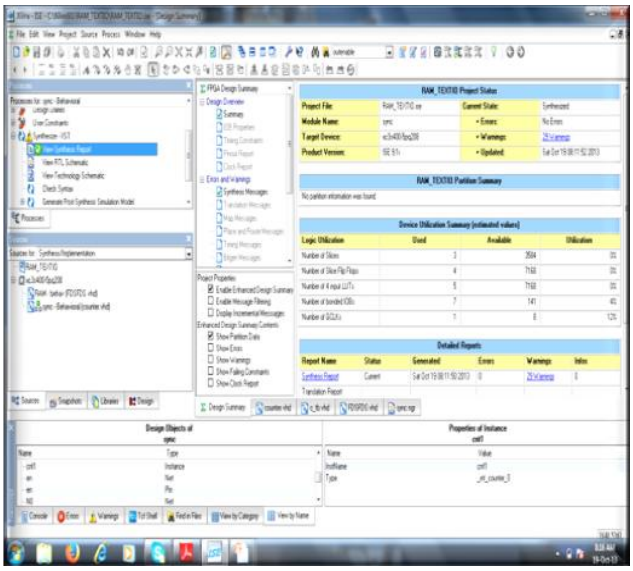

Fig. 4 Synthesis Report of Counter

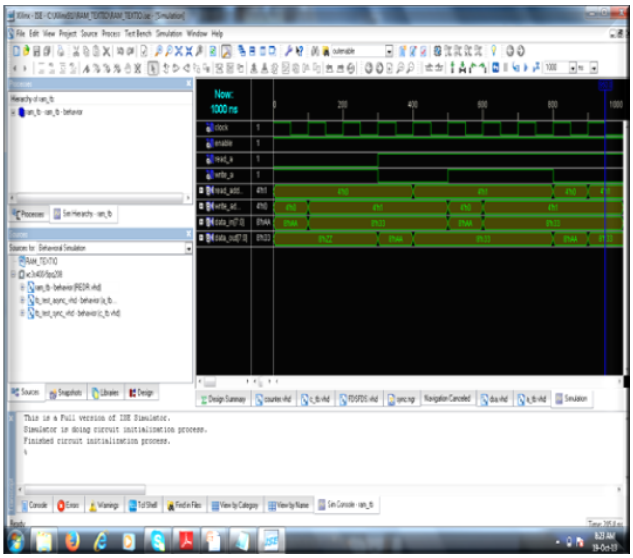

Fig. 5 Simulation of Counter

2. RAM

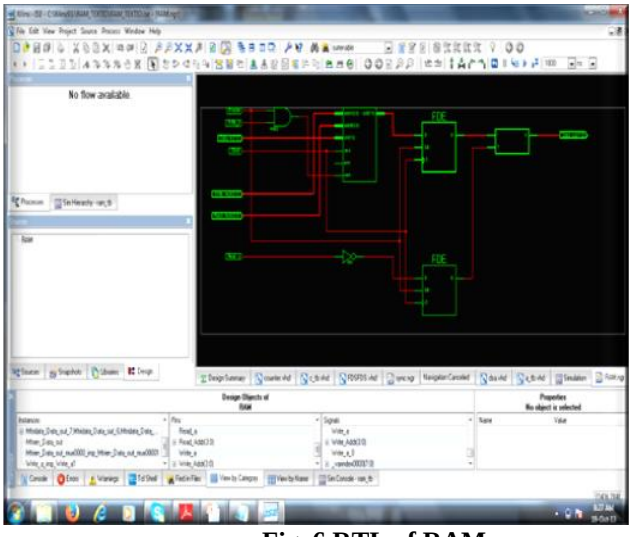

Fig. 6 RTL of RAM

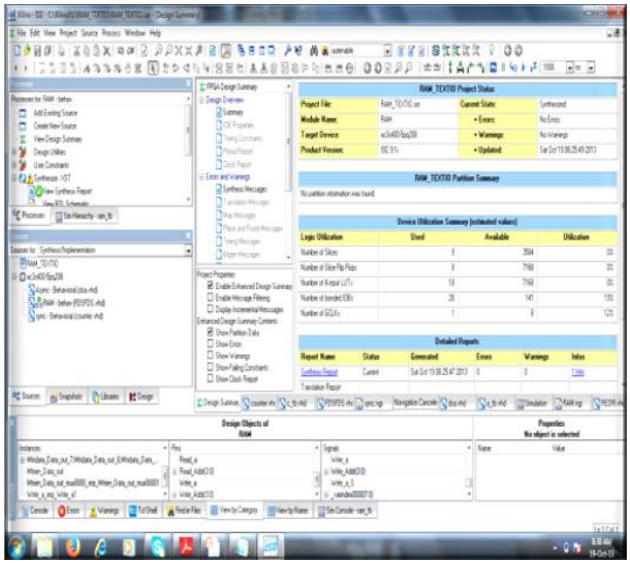

Fig. 7 Synthesis Report of RAM

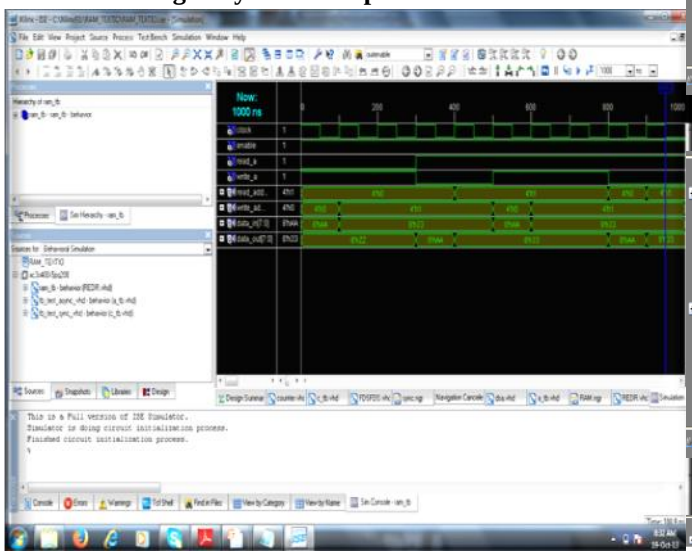

Fig. 8 Simulation of RAM using Text IO

Simulation on Modelsim environment to see wave form of individual block as Modelsim can show analog waveform. Bringing Top Level Module to Spartan-II by Xilinx for synthesis and generate RTL for an IP core. Design of Multifunctional DDS waveform generator using different logic styles and simulation of these waveforms on Xilinx ISE 9.2i Tool or Modelsim. Finally the result analysis will be carried out.

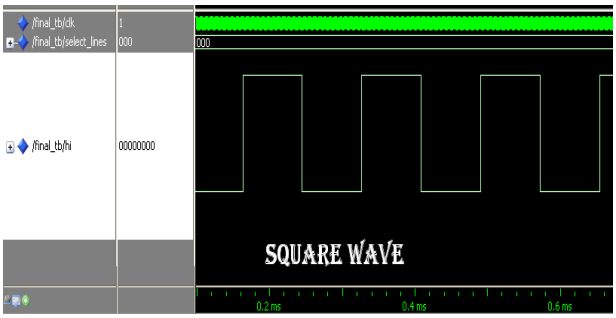

Fig. 9 Square wave

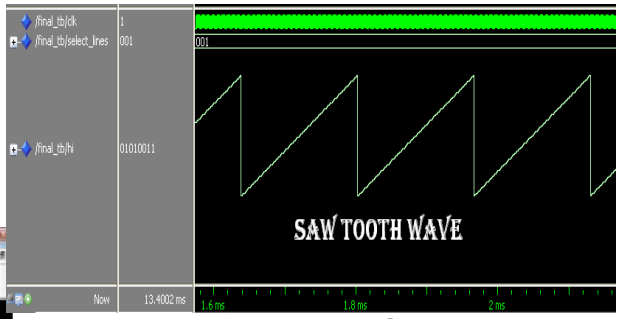

Fig. 10 Sawtooth wave

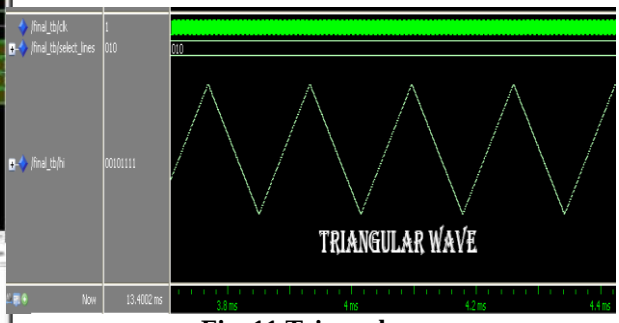

Fig. 11 Triangular wave

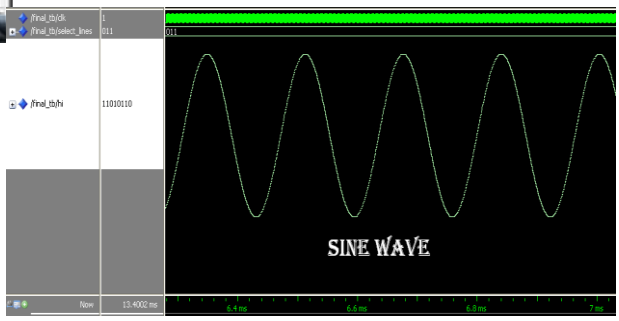

Fig. 12 Sine wave

Mixing of two signals

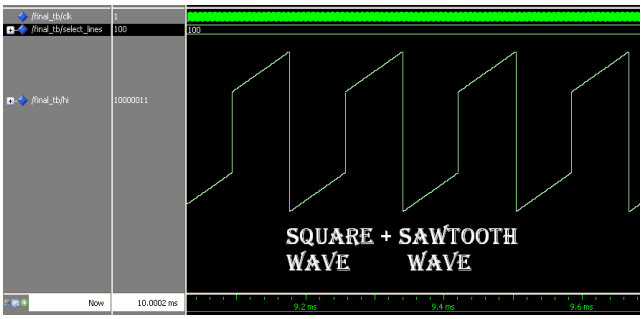

Fig. 13 Square wave + Saw tooth wave

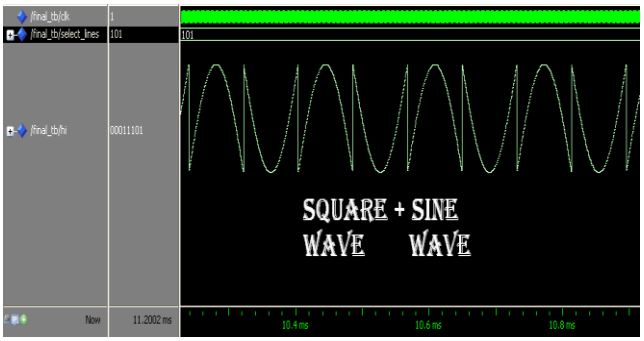

Fig. 14 Square wave + sine wave

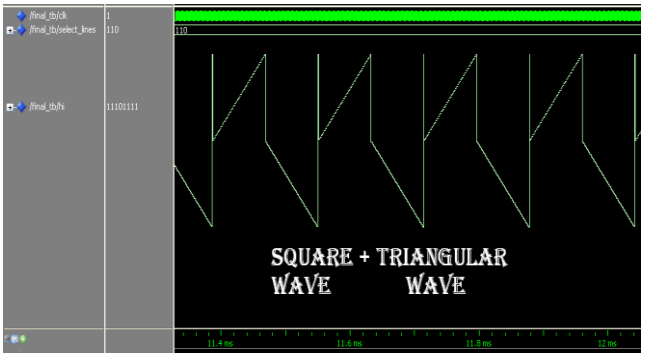

Fig. 15 Square wave + triangular wave

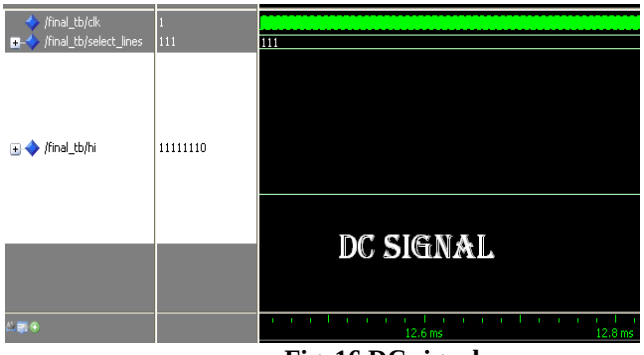

Fig. 16 DC signal

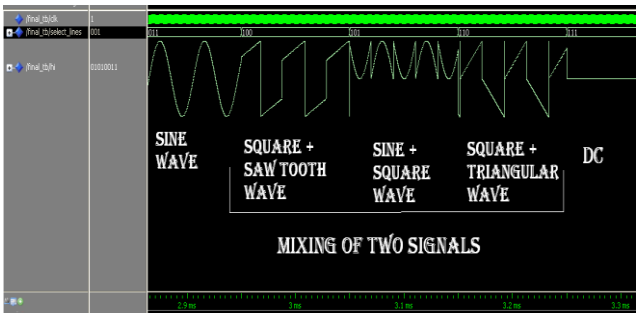

Fig. 17 Overall output

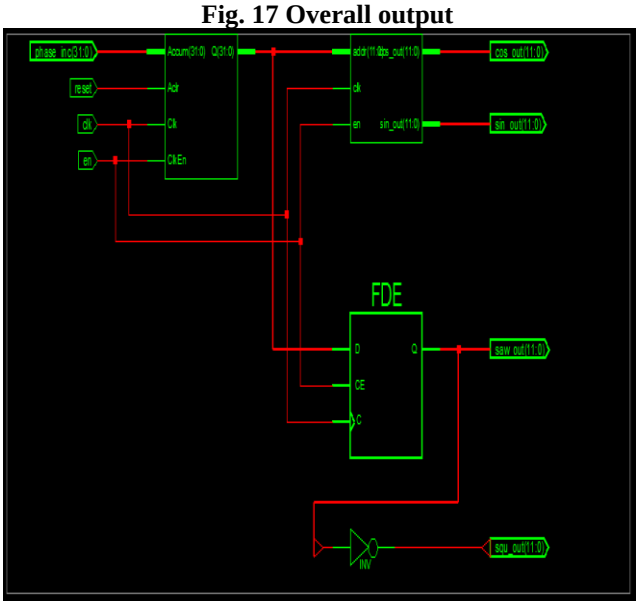

Fig. 18 RTL schematic

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	23	3584	0%
Number of Slice Flip Flops	44	7168	0%
Number of 4 input LUTs	34	7168	0%
Number of bonded IOBs	83	221	37%
Number of BRAMs	6	16	37%
Number of GCLKs	1	8	12%

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun Mar 2 15:40:14 2014	0	0	2 Infos
Translation Report	Out of Date	Sun Feb 16 08:23:09 2014	0	0	0

Fig. 18 Overall Synthesis report

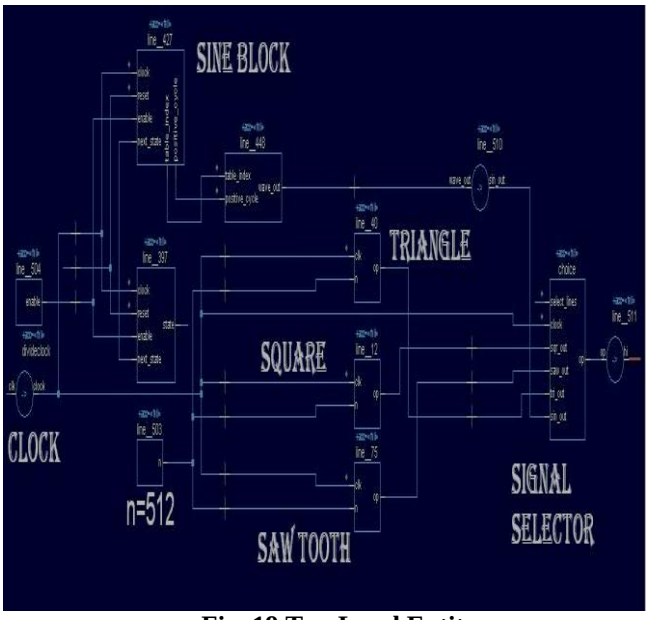

Fig. 19 Top Level Entity

Result

The work presented in this paper was implemented using VHDL and logic simulation was done using Xilinx ISE 9.2i Tool or Modelsim The waveforms for square wave, triangular wave, sawtooth wave, sinusoidal wave is as shown in figure .

Conclusion

In this paper, an efficient method is presented with proposed DDS design which supports low hardware requirements in terms of LUT's available on FPGA target device. The fully digital signal generator based on SOPC has various advantages of hardware reconfigurable and flexible, which makes the system design easy to change and carry out.

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