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CMOS Implementation of Reliable Synchronizer for Multi clock domain System-on-chip

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Abstract —
This paper presents the CMOS implementation of reliable synchronizer for multi clock domain system on chip. Reliability of synchronizer is crucial for reliability of system on chip. Whenever a signal crosses the boundary of clock domain through the synchronizer, nonzero probability of failure of synchronizer must be mitigated. Synchronizer fails when the signal changes in the metastability window. Reliable synchronizer is designed which provides synchronized output even if signal changes in the metastability window. In an architecture signal change detection in metastability window is made. There are two paralleled placed 2 flop synchronizer one receives the data directly while other receives through delay. When data changes in the window the output of delayed 2 flop synchronizer is sampled and it is controlled by synchronizer controller. CMOS layout of reliable synchronizer is designed in microwind 31 software and simulated in Tanner Tool v14. The MTBF is estimated and significant improvement is observed.
Keywords— Reliable synchronizer, Multi clock domain, data synchronization, system on chip, globally asynchronous and locally synchronous (GALS)

I. INTRODUCTION

Reliable synchronizer synchronizes data among clock domain of multiclock system. Reliable synchronizer is also required when asynchronous input enter synchronous clock domain. Synchronizer is susceptible to failure. Metastability occur when the setup and hold time of a synchronizer is not met. Synchronizer failure is said to occur if clock domain uses synchronizer output while the output is still in the metastable state. There is nonzero probability that synchronizer will not resolved its metastability state correctly within the allowed time. This problem must be mitigated This failure is becomes more sever because of increase clock speed, data rates , number of clock domain crossing (CDC) and semiconductor process variability. To design a reliable synchronizer, model describing the failure mechanism have been developed. These model express risk of metastability in terms of MTBF (Mean Time between Failures) of the synchronizer [1].

$$MTBF = \frac{e^{s/\tau}}{\mathrm{Tw.Fc.Fd}}$$

Where Fc and Fd are clock and data transition frequencies, s-predetermined time allowed for metastability resolution, τ-resolution time constant.
In determining the synchronizer MTBF ,there are intrinsic parameter varying with PVTA which include settling time constant τ_{eff}, aperture width and extrinsic parameter vary with application which include clock rate (Fc), data transition rate (Fd) and duty cycle.

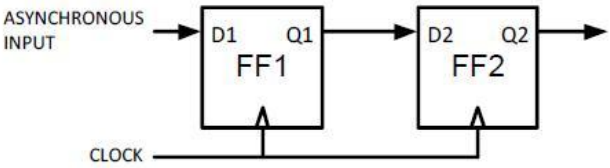


Fig 1. Two flip-flop synchronizer

A simple two-flip-flop synchronization circuit is shown in Figure 1. The first flip-flop may become Metastable. The second flip-flop samples Q1 a cycle later, hence resolution period is equal to time period of clocked frequency .Actually, any logic and wire delays are subtracted from the resolution time: S = T_C-t_{pCQ}(FF1)- t_{SETUP}(FF2)-t_{PD}(wire), etc. A failure means that Q2 is unstable and it may change later than t_{pCQ}.

[1][2][3][4][5]. Various synchronizers are proposed over the decades which include two Flip flop synchronizer, Jamb-latch synchronizer, cascaded flip-flop synchronizer, wagging synchronizer.[6][7][8][9][10] The paper is arranged as follows ,in section 2 principal of proposed architecture of reliable synchronizer is explained with help of block representation. In section 3, black box representation of synchronizer controller is explained along with its CMOS realization and
simulation result. In section 4, reliability of reliable synchronizer is discussed with emphasis on the 'τ' and its various means of finding. In section 5 conclusion and references are given.

II. Architecture of reliable Synchronizer

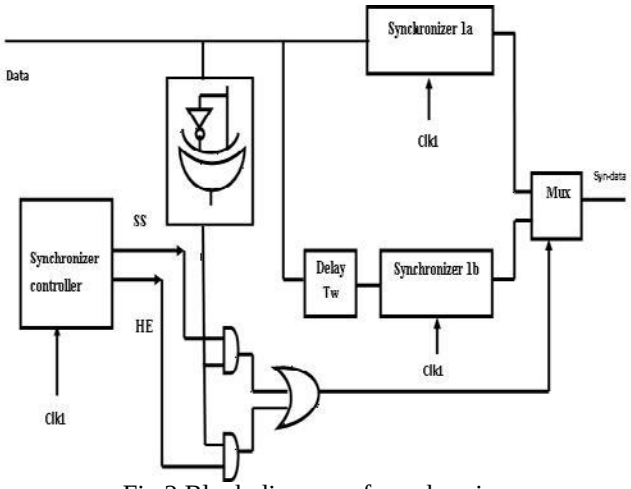


Fig 2 Block diagram of synchronizer

This architecture is taken from (1).Here effort is made to delay the data rather than any other parameter in clock domain. If the data changes in the metastability window then the output of synchronizer1a will not be taken in system, rather delayed data and synchronizer 1b will be taken. In this system, clock period is needs to be exactly calculated at input synchronizer. When clock edge is detected, delay of setup time and hold time for next clock cycle can be derived. Metastability window begin with start of setup time and ends with end of hold time shown in fig 3 . The signal 'ss' is indicating the beginning of metastability window and the signal 'HE' indicates the end of metastability window. Whenever signal 'ss' becomes high, data change detection block will poll for the data change and continue till signal 'HE' is high. If in between the data changes then data change detection block will generate control signal. This control signal is used as select line of mux as shown in Fig.4. Data will get delayed by delay Tw and then sampled by synchronizer 1b. Data will be appearing correctly at synchronizer1b whereas synchronizer 1a will enter in metastability .It will not be selected by multiplexer.

III. Architecture of synchronizer controller

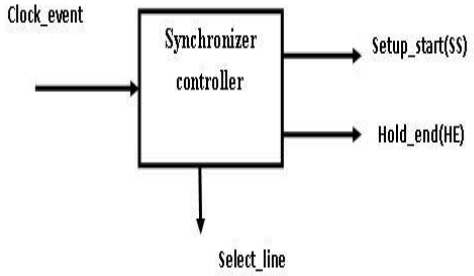


Fig 3. Black box representation of synchronizer controller

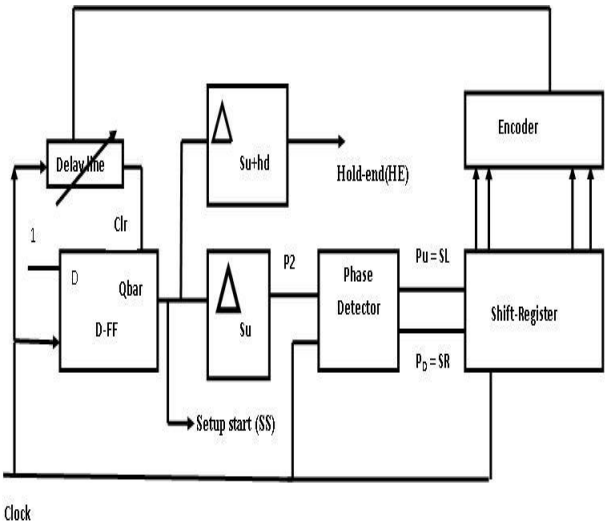


Fig 4 Circuit diagram of synchronizer controller

Synchronizer selection controller consists of Monoshot, Predetermined delay Δsu and Δsu+he, phase detector, shift register, encoder and delay line as shown in Fig 4. Monoshot is used to extend pulse width of the clock period up to setup start of the next clock edge.

Predetermined delay Δsu and Δsu+he will offer the delay equal to delay of setup time and (setup + hold) time of synchronizer. Phase detector compares the phases of reference input clock and delay output. Comparisons yields a signal proportional to phase error i.e. pump up(pu) and pump down(pd) .These signals are connected to shift left(sl) and shift right(sr) of shift register. Shift register is loaded with one bit high. This bit is shifted left or right depending on phase error. Encoder will encode the output of shift register. Encoder output is used to select the delay from delay line. As long as there is phase error, delay is adjusted. Once the phase error becomes zero, delay will get lock.

3.1 Delay-line

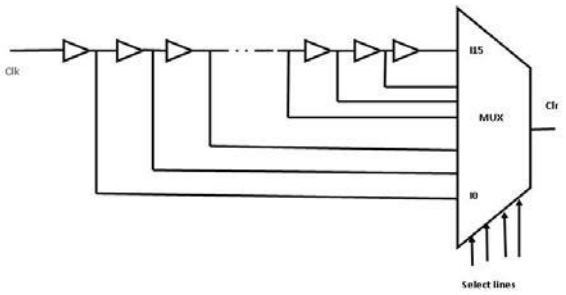


Fig 5 circuit diagram of delay line

The Delay- line consists of multiplexer 16:1 and chain of buffer as shown in fig 5. The minimum delay is selected by selection lines of multiplexer when the value of the select line is "s3s2s1s0"= "0000". The value of minimum delay is 12.77ps. The maximum delay is set by selection lines when the value of the select line is "S3S2S1S0" = "1111". The value of maximum delay is 12.77ps .Buffer of delay is set.

Buffer used in Delay line

Basic component used for delay line is buffer which is constructed using two inverter connected back to back. Fig 6 and Fig 7 shows the CMOS layout and simulation waveform of buffer circuit.The delay offered by buffer element is 6.03ps.

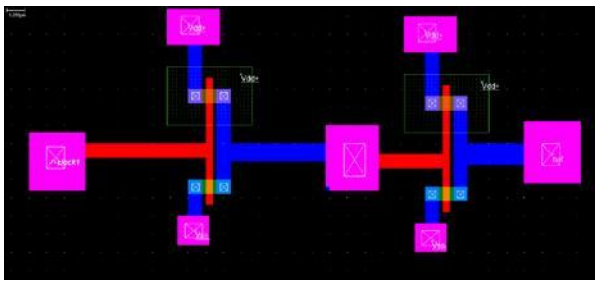
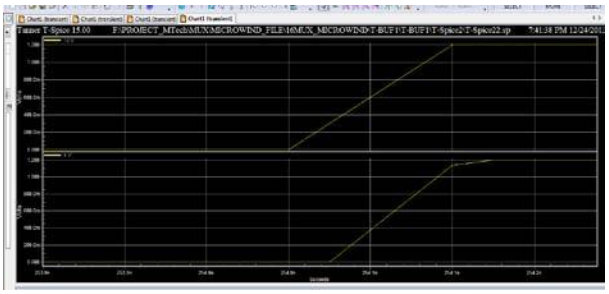


Fig 6 CMOS layout of Buffer



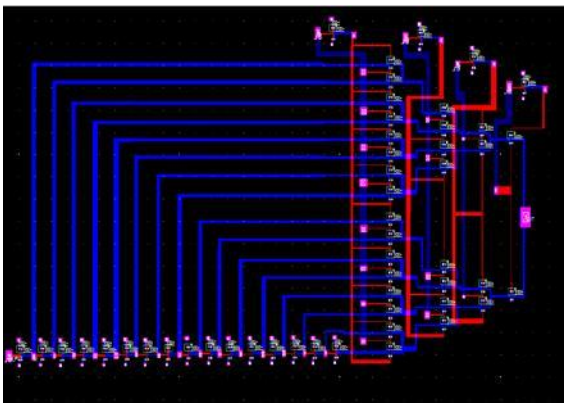


Fig 8 CMOS layout of Delay line

3.2 Mono-shot

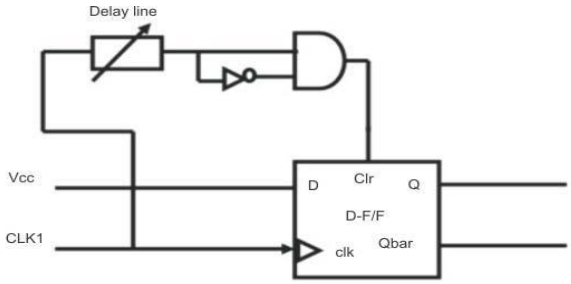


Fig 9 Circuit diagram of monoshot

As shown in fig 9, mono-shot consists of D Flip-flop and delay line. The D input of flip-flop is connected to Vcc and clear pin (clr) of D flip-flop is connected to clock through the delay line and AND gate. The delay line will provide the delay up to the beginning of setup time of next clock. The output of flip-flop is forced to zero by clr pin. The output of flip-flop is high before arrival of clr signal. The Qbar is the complement of Q output of D flipflop. The output of monoshot goes to

Δsu block of controller as an input. It indicates the beginning of setup time.

3.3 Phase detector

The output of the phase detector depends on both the phase and frequency of the inputs. It is also known as sequential phase detector .It compares the leading edge
of the output of delay Δsu and locally generated clock. A locally generated clock rising edge cannot be present without output of delay Δsu rising edge. The pulse width of output of delay Δsu and locally generated clock pulse width do not matter.

If the Rising edge of the output of delay Δsu leads the locally generated clock rising edge, the "Pump up", Pu output of the phase detector goes high, while the down Fig 12 Simulation of phase detector

output is remains low. When the locally generated clock signal leads the output of delay su, pump up (Pu) remains low while the pump down (Pd) goes high. A time equal to the phase difference between output of delay Δsu and locally generated clock.

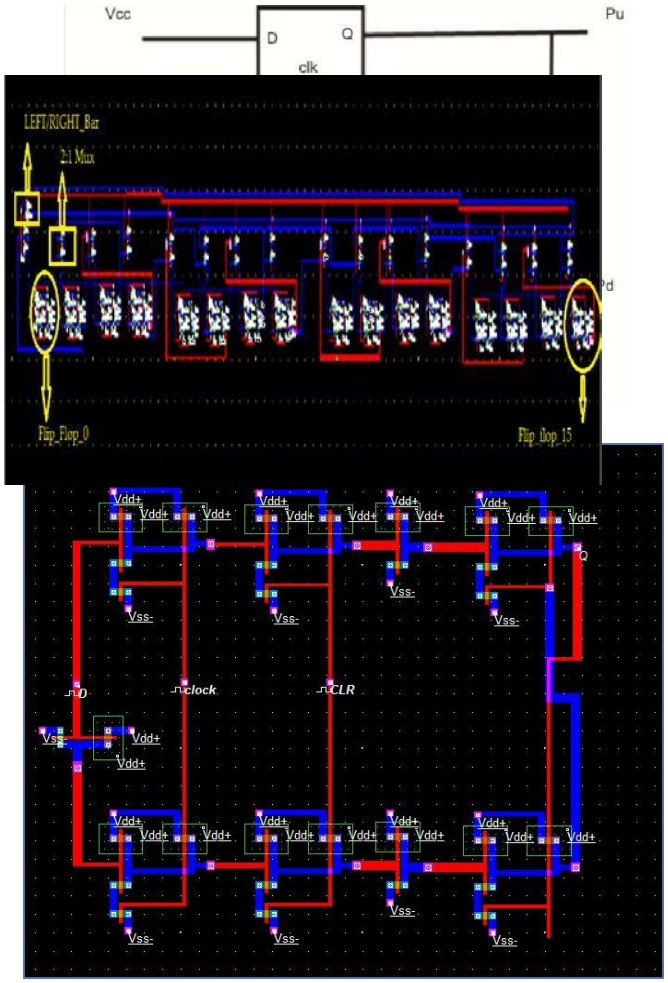
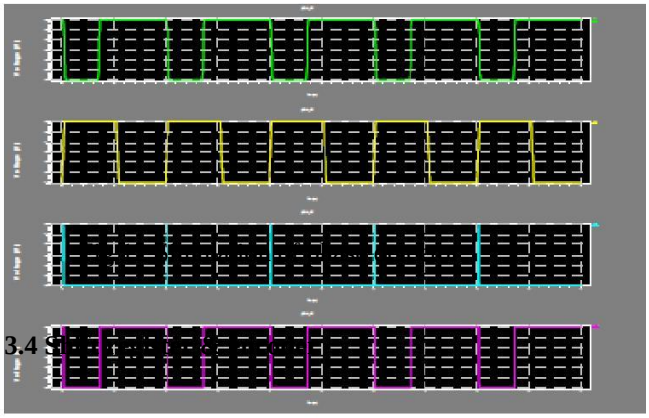


Fig 11 CMOS Layout of phase detector

Fig.11 and Fig. 12 shows the CMOS layout and simulation waveform of phase detector.



3.4 Shift register & Encoder

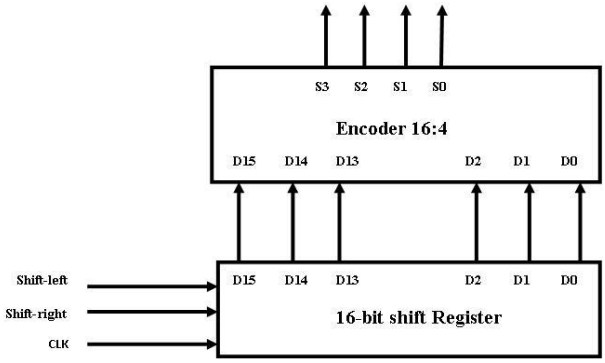


Fig13 Circuit diagram of shift register & Encoder

This shift register and encoder block consists of 16 bit shift register and 16:4 encoders as shown in fig 13. This shift register is similar to that of conventional shift register except that there are separate lines for shift left and shift right .This 16 –bit shift register has D0 to D15 lines as an output line with D0 is set initially while other bits are reset. Pump up (Pu) and Pump down (Pd) is connected to Shift left & shift right .Depending on pump up and pump down, this set bit is rotated toward left or right. The outputs of shift register are connected to encoder 16:4. It encodes the data bit. The encoded bit is appeared at S3 to S0. The output of encoder is connected to the select line of multiplexer of delay line which is used for setting the delay.

The layout of 16 bit shift register is shown in fig 14 and simulation in fig. 15

Fig 14 CMOS layout of 16 bit shift register

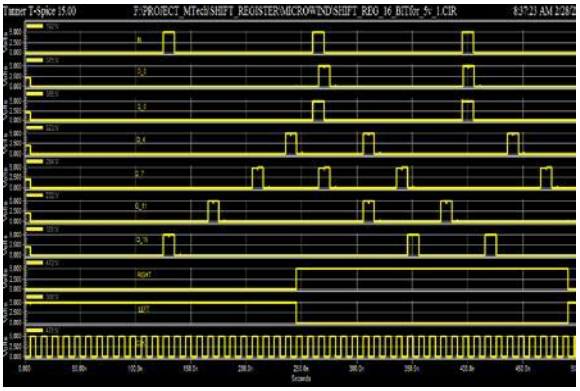
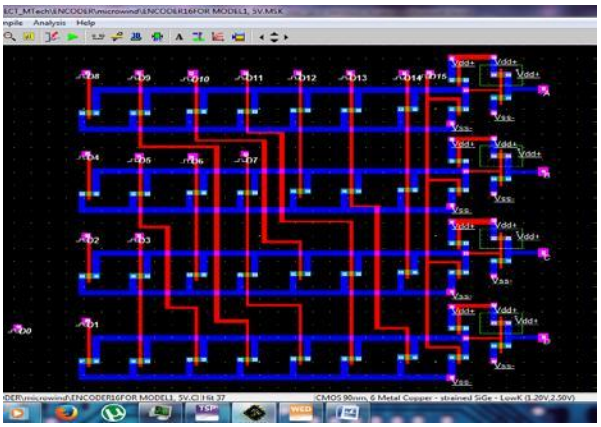


Fig.15 simulation waveform of shift register

Encoder

The encoder encodes the data at its input and provides four bit out.CMOS layout and simulation is shown in fig 16 and fig 17.



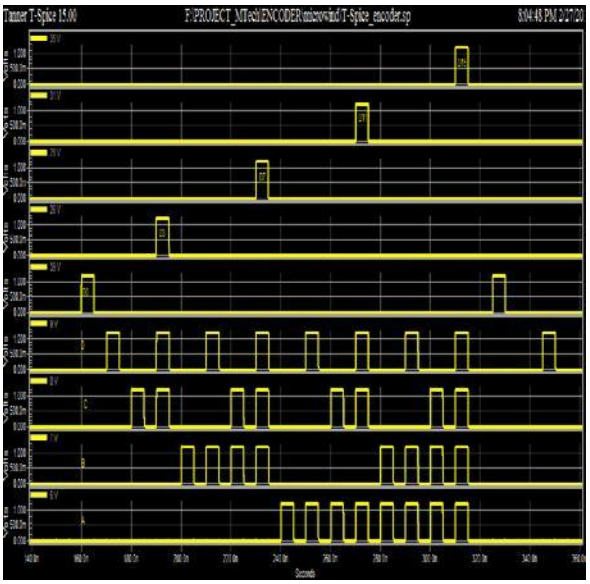


Fig 17 simulation waveform of encoder

IV. Reliability analysis of synchronizers

Reliability of two flop synchronizer is based on probability of entering metastability and exiting from metastability.

MTBF of synchronizer is estimated based on traditional model .Desirable values of MTBF depends on the application and ranges from several year upward. The parameter τ is predominant in synchronizer characterization since its effect on MTBF is exponential,

τ can be estimated by analysis method where the for specific technology of CMOS i.e For CMOS 90 nm 6 metal copper strained sig low k(1.20V ,2.5V).

τ can be determined using τ = c/gm where gm is transconductance.By guesstimate methods, one can approximate as τ is equal to twice of FO4 gate delay.FO4 gate delay is process independent delay metric, delay of an inverter 4X smaller than itself and driving an inverter 4X larger than itself. τ Can be estimated by simulation method based on the approximated slope of Vdiff across the cross coupled in the latch.

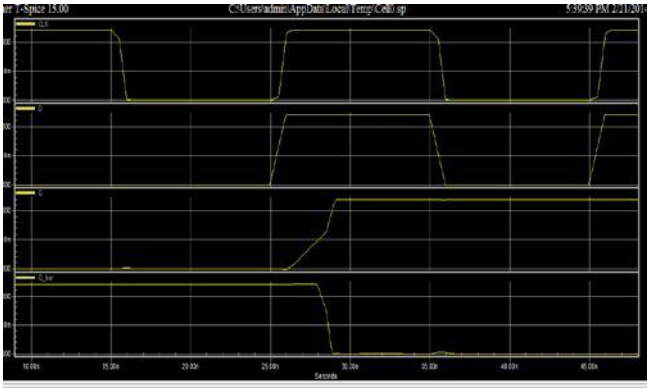


Fig18 simulation waveform of two-flop synchronizer

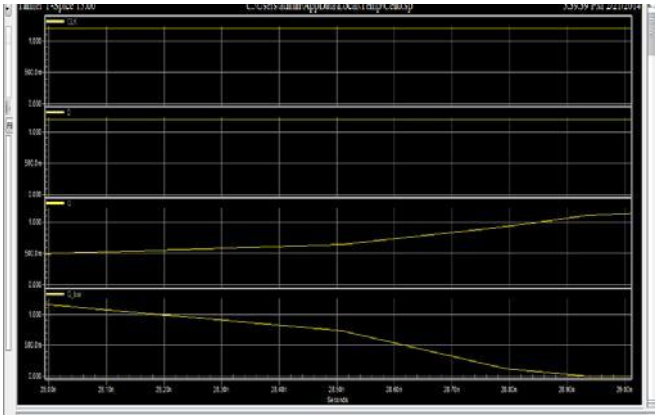


Fig 19 simulation waveform of expanded view

V. Simulation and result analysis

Fig. 20 CMOS layout of reliable synchronizer

The CMOS layout is designed in microwind and PSPICE netlist is generated. The PSPICE netlist is imported in TANNER tools and simulated on Tanner Tools.

VI. CONCLUSION

MTBF is one of the characteristics of reliable synchronizer .Non-zero probability of failure of synchronizer raises the question on the reliability of multi-clock domain system on chip. This reliable synchronizer mitigate the problem faced by data

synchronization in multiclock domain system on chip . τ is metastability time constant predominantly affect the MTBF, its way of determining must be validated by analysis means ,simulation means or measurement. The architecture of reliable synchronizer determines the setup start and hold end ,and data change detection in window and bypass the effect of metastability from entering in to synchronous domain. MTBF of two flipflop synchronizer and reliable synchronizer after CMOS implementation is carried out and substantial improvement is observed.

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