

Encoding Scheme for Power Reduction in Network on Chip Links

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ABSTRACT

In network on chip the links are the main element for the power dissipation. In this paper we are proposing encoding scheme to reduce the self switching and the cross talk in the network on chip. Network on chips structure makes a fitting replacement for system on chip designs in designs incorporating large number of processing cores. In network on the major source of power dissipation is the network on chip links. If compared the power ratio between the network on chip links and router links are more power hungry than router. The dynamic power dissipation in links is major contributor to the power consumption in network on chip. This is due to the self switching and the second factor is cross coupling capacitance. In the proposed encoding technique the first self switching is reduce by checking the switching transition and then the coupling between the links is checked and ensured that the power consumption is reduced. This encoding technique is incorporated with the wormhole routed network. The end to end scheme incorporating the encoding technique to reduce power in the wormhole routed network on chip. The encoder and decoder of the proposed scheme with wormhole router are described in the RTL level in verilog HDL.

Keywords –crosstalk;lowpower;network on chip links;self switching;uniform power reduction

I. INTRODUCTION

The Network on chip is an emerging approach for the implementation of on chip communication architecture. The system on chip designs incorporating large no. of processing cores and modular structure of Network on chip makes a fitting replacement for system on chip. Network on chip is intended to solve the shortcomings of these, by implementing a communication network of switches, micro routers and resources.[7] System on chips are not containing IP cores only and traditional methods for communication such as bus are not suitable solution for future System on chips. The Network-on-Chip has emerged as underlying infrastructure for communication between Intellectual Property cores. Network on chip is solution for communication architecture of future System on chips that are composed of switches and IP cores where communicate among each other through switches. Between IP cores data move in the form of packet. As the technology shrinks the power ratio between link and router increase making link more power hungry than routers.[10]

A network on chip communication gives flexibility in the topology, in support to that the flow control,

Advance routing algorithms, self switching techniques guarantying the quality of service. Network on chip is an approach to design the communication subsystem between intellectual property cores in a system on chip. The communication strategy in system on chip uses dedicated buses between communicating resources. This will not give any flexibility since the needs of the communication, in each case, have to be thought of every time a design is made. Another possibility is the use of common buses, which have the problem that it does not scale very well, as the number of resources grows.[6]

Different encoding techniques are proposed to reduce the power in reference to the bus based architecture. Bus invert method can be applied to encode the randomly distributed patterns. While the [1],[4],[8] and[11] deals with the reduction of switching activity in the serial link caused due to the serialization of parallel data. Some encoding technique considers the contribution of cross talk. [6] Proposed the partial bus invert coding as link level power encoding technique.

This encoding scheme is developed by taking the both factor self switching and the cross talk into consideration. The encoder and decoder are placed in the network interface of the wormhole routed network. The first stage rearranges the data stream in such way that the transition in each link is reduced while in the second stage the inverting of data of depends upon the contribution of the cross couple activity in power dissipation of the link, The proposed encoding scheme can be applied to the wormhole routed network as the interleaving of flits are not allowed.

The rest of paper organized as follows- In section II the overview of proposal is discussed. In the Section III encoding technique incorporated for power reduction is discussed. The working block of the encoder and decoder is discussed in the Section IV. In Section V the simulation result of encoder and decoder is there. Section VI is reference.

II. OVERVIEW OF PROPOSAL

The general scheme of proposed work is given in Fig 1. The basic concept is to apply the encoding technique in end-to- end links in resource network interface of wormhole routed network on chip. The most suitable switching technique for on chip communication is wormhole switching.

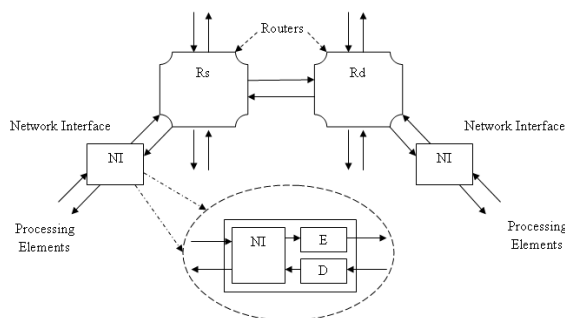


Fig. 1. General Scheme of proposed approach [4]

The pipeline nature is the basic concept for the wormhole switching. The links of the routing path are cross by the same sequence of flits, the encoding scheme ensure the same switching behavior in each routing path. As shown in the Fig. 1 the encoder and decoder blocks are incorporated in the network interface. The encoder encodes the outgoing flit in the packet in such a way that the power dissipated is minimized by inter router point to point links which form the routing path.

III. PROPOSED SCHEME

The dynamic power in the link is given by:

$$P = [T_{0 \rightarrow 1}(C_s + C_l) + T_c C_c] V_{dd}^2 f. \quad (1)$$

Where C_s is self capacitance, C_l is the load capacitance, C_c is the coupling capacitance, $T_{0 \rightarrow 1}$ and T_c are the average no. of transition for C_s and C_c , F_{clk} is clock frequency, V_{dd} is supply voltage. $T_{0 \rightarrow 1}$ counts the $0 \rightarrow 1$ consecutive transition in the bus. T_c counts the correlated switching between the adjacent links. In the proposed technique the two techniques are incorporated first the self switching is reduced and then cross coupling effect is reduced. [5]

3.1. Self Switching reduction

The equation (1) shows that the dynamic power dissipation in the link is directly proportional to self switching activity. The switching transition in the link increases when n bit parallel data is serialized. To reduce the no. of transition encoding schemes arrange the data prior to serialization to reduce the power consumption. The scheme works in the following way:

1. t -bit parallel data ($t=2^m, m>1$) $Q(t)$.
2. Before serialization the N -bit are checked for no. of transition.
3. If $N_0 > N_T$, $Q(t) = Q_s(t)$ else $Q(t) = Q(t)$, where N_0 is no. of transition, N_T refers to threshold value, $Q_s(t)$ is obtained by interchanging even and odd bits.
4. The threshold for the first stage is calculated by the formula.

$$N_T = t/2 - 1, \text{ where } t = 2^m \text{ for } m=2$$

$$N_T = t/2, \text{ where } t = 2^m \text{ for } m=3$$

$$N_T = t/2 + 2(m-4) + 1 \text{ where } t = 2^m, \text{ for } m = 4, 5, 6 \quad (2)$$

3.2. Cross coupling effect elimination

TABLE I
CHANGE IN TRANSITION [5]

Time	Normal Coding	Inverted Coding
T-1	00 00 11 11 Type1	00 00 11 11 Type1
T	01 10 01 10	01 10 01 10
T-1	01 10 Type2	00 11 Type3
T	10 01	11 00

T-1	00 11	Type3	01 10	Type2
T	11 00		10 01	
T-1	00 01 10 11	Type4	00 01 10 11	Type4
T	00 01 10 11		00 01 10 11	

From the above transition table there are four types. Type1 when one link switches while other remains unchanged. Type2 when one line switches from high to low and other switches from low to high. Type3 is when both lines switches simultaneously. Type4 when both the links remains unchanged. T_c is the weighted sum of different type of coupling transition contribution.

$$T_c = T_1 k_1 + T_2 k_2 + T_3 k_3 + T_4 k_4 \quad (3)$$

Here the T_j , $j = 1, 2, 3, 4$, are the average number of transition for type j and k_j are weights. According to [6] it is assumed $k_1 = 1, k_2 = 2$ and $k_3 = k_4 = 0$. That is, k_1 is assumed as reference for other types of transition. The effective capacitance in Type II transition is usually twice that of a Type I transition. In Type III transition, as both signal switch simultaneously. Finally, in Type IV transition there is no dynamic charge distribution over C_c . Based on this, equation (1) can be expressed as follows:

$$P = [T_{0-1}(C_s + C_l) + (T_1 + 2T_2)C_c]V_{dd}^2 F_{clk} \quad (4)$$

To eliminate the cross coupling effect link and adjacent link, are considered. Each two bit word represents status of link z and $z+1$ respectively at specified time. It can be observed that if we invert the bits entering link $b+1$, the type II transition gets

converted to type III and vice versa. After inversion equation (3) can be written as:

$$T_c' = T_1 k_1 + T_2' k_2 + T_3' k_3 + T_4 k_4 \quad (5)$$

Where $T_2' = T_3, T_3' = T_2$. Hence in (3) if $T_2 > T_3$, the data bits of the particular link is inverted. As $k_3 = 0$, from (5) and (3) $T_c' < T_c$, as $T_2' < T_2$. This scheme can be applied along with the first scheme as inverting does not alter the effect of shuffling of bits. [5]

IV. ARCHITECTURE

From the Fig.1 the encoder and decoder is placed in the network interface level of the network in chip. As shown in the Fig 2. The $P=64$ bit data is arranged in the matrix manner the data from the packet is sent according to the scheme proposed. Additional $P/Q+1$ (where Q stands for number of links, in this design assumed to be 8) bits are added as control bits and data packet enters stage II. Here alternate links (four odd links) are inverted or send as they are after comparison with adjacent links as per encoding scheme. Power reduction acquired in the first stage remains intact as inverting ensures same number of switching transition. Data bits (P bits) and $(P/Q+1+P/2Q)$ control bits are converted to $(P/Q+P/4Q)$ bits by a serializer. Control bits are sent through $P/4Q$ links. First link consist of P/Q control bits of first stage. The extra bit $P/2Q$ control bits generated in stage 2 constitute extra link. [5]

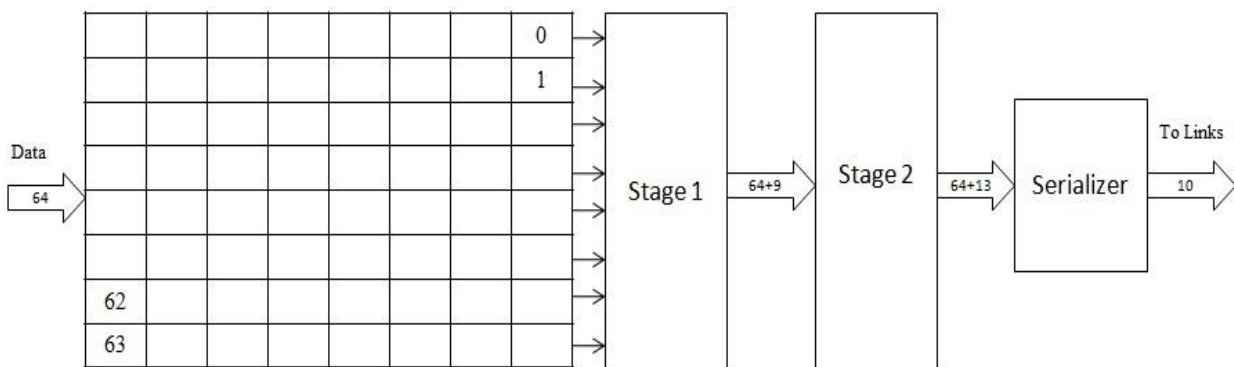


Fig. 2 Encoder for proposed scheme[5]



Fig. 3. Decoder for proposed scheme[5]

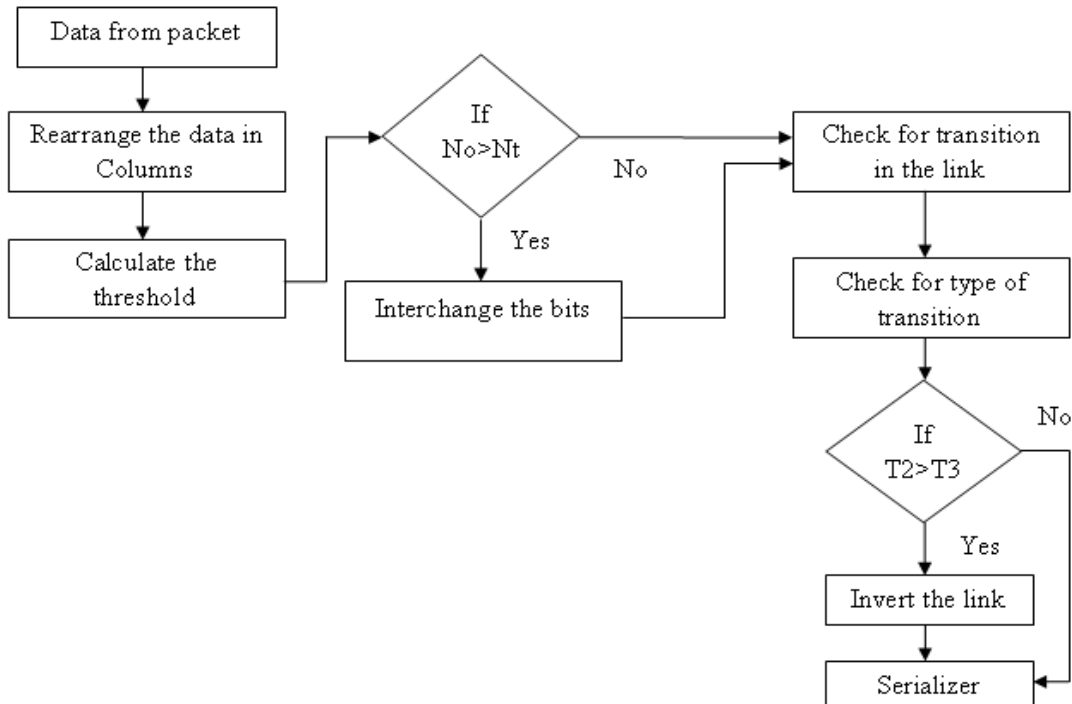


Fig. 4 Flow graph for proposed Encoder

V. SIMULATION RESULTS

Fig. 5 shows the simulation waveform for the encoder as proposed in the paper. The input data is given to the input of the encoder. In Encoder the stage 1 counts the number of 0 to 1 transition, if the number of transition is greater than the threshold value which is calculated as per the Section III A. If the transition is greater than threshold then the even and odd bits are shuffled as per the encoding scheme. The output of the stage 1 encoder is given to the input of the stage II encoder along with some extra control bits of stage 1. In stage II the coupling activity of the data in the links are checked according to the transition table and data is changed as per the transition from type II to type III. The output is then given to the serializer. The data given to the encoder as shown in Fig.6 has total 39 transitions from 0 to 1 and at the output of the serialize the transition reduce to 26 and there is no coupling activity in links of Type II.

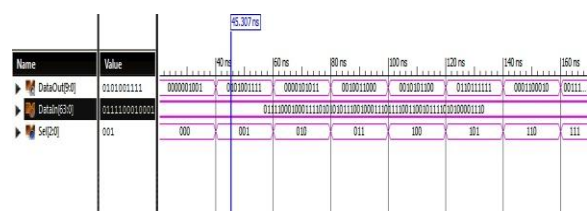


Fig. 5. Simulation Waveform for proposed Encoder

Fig. 6. Shows the simulation waveform for the Silent coding encoder. The same input is given to the silent coding encoder, In the silent coding the first link remains as it is and the next link is grey coded with the previous link. The data given to the encoder has total no. of transition from 0 to 1 is 39 and at the output of the encoder the 0 to 1 transition reduce to the 32. But as compare to the output of the proposed encoder the silent encoding has some coupling activity of Type II.

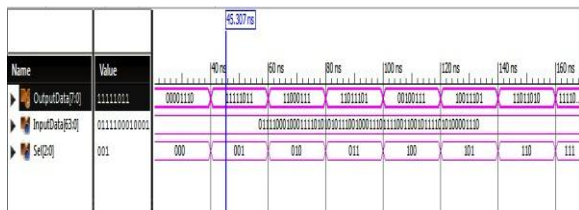
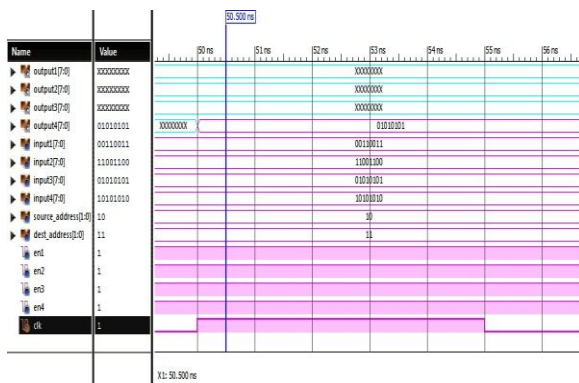


Fig. 6. Simulation Waveform for Silent coding Encoder

Fig.7 shows the output waveform of the crossbar used in wormhole router. The enable signal allows the flow of data from one port to another depending upon the value of source and destination address. As shown in the waveform at the positive edge of clock the source address is 10 and the destination address is 11, from the waveform the data of input 3 is available at the output 4.



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