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"Design and Implementation of Orthogonal Code Convolution Using Enhanced Error Control Technique"

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ABSTRACT
When data is stored, compressed, or communicated through a media such as cable or air, sources of noise and other parameters such as EMI, crosstalk, and distance can considerably affect the reliability of these data. Error detection and correction techniques are therefore required. Among other techniques such as Cyclic Redundancy and Solomon Codes; orthogonal coding is one of the codes which can detect errors and correct corrupted data in an efficient way. In this propose work a high efficient combined error detection and correction technique based on the Orthogonal Codes Convolution, Closest Match, and vertical parity. This method will be experimentally simulated using Xilinx software and implement using Field Programmable Gate Array (FPGA).The propose technique will detects 99.99% of the errors and corrects as predicted up to (n/2-1) bits of errors in the received impaired n-bit code.

Keywords: Error detection and correction, FPGA, Orthogonal Code Convolution.

I. INTRODUCTION

Information and communication technology has brought enormous changes to our life and turned out to be one of the basic building blocks of modern society. With the increase of data transmission and hence sources of noise and interference, Engineers have been struggling with the demand for more efficient and reliable techniques for detecting and correcting error in received data and data reliability in transmission is still problem.

Error detection and correction techniques are therefore required. Some of those techniques can only detect errors, such as the Cyclic Redundancy Check (CRC) [1-2]; others are designed to detect as well as correct errors, such as Solomon Codes [3, 4], Hamming Codes [5], and Orthogonal Codes Convolution (OCC) [6, 7]. However, the existing techniques cannot achieve high efficiency in error detection and correction as well as meet bandwidth requirements, especially with the increase in the quantity of data transmitted.

In this propose work a high efficient combined error detection and correction technique based on the Orthogonal Codes Convolution, Closest Match, and vertical parity (OCCMP). Among above methods, orthogonal code is one of the code which can detect errors and correct corrupted data in an efficiently with increased quantity of data transmitted. Generation of 16 bit orthogonal code plays very important role in this project.

1.1 Orthogonal Code

Orthogonal codes are binary valued, and they have equal number of 1's and 0's. An n-bit orthogonal code has n/2 1's and n/2 0's; i.e., there are n/2 positions where 1's and 0's differ [7, 8]. Therefore, all orthogonal codes will generate zero parity bits. The concept is illustrated by 8-bit orthogonal codes as shown in Fig. 1. It has 16 orthogonal codes and 16 antipodal codes for a total of 32 bi-orthogonal codes. Antipodal codes are just the inverse of orthogonal codes; they have the same properties.

Before transmission, m-bit data set is mapped into a unique n-bit orthogonal code. For example, a 5-bit data set is represented by a unique 16-bit orthogonal code, which is transmitted without the parity bit. When received, the data are decoded based on code correlation. It can be done by setting a threshold between two orthogonal codes.

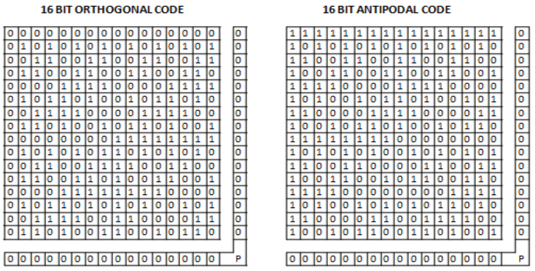


Fig.1: Illustration of 16-bit orthogonal codes.

This is set by the following equation: d_{th}=n/4 .Where *n* is the code length and *dth* is the threshold, which is midway between two orthogonal codes. Therefore, for the 16- bit orthogonal code (Fig. 2), we have *dth=16/4=4*. for a possible match.A counter is used to count the number of 1's in the resulting signal. For example, for 16-bit orthogonal code, the operation will lead to sixteen counter results. If one of the results is zero, it means there is no error. Otherwise, the code is corrupted. The corrected code is associated with the minimum count. If the minimum count is associated with one combination, the received and corrected code will be this combination. However, if the minimum count is associated with more than one combination of the orthogonal codes

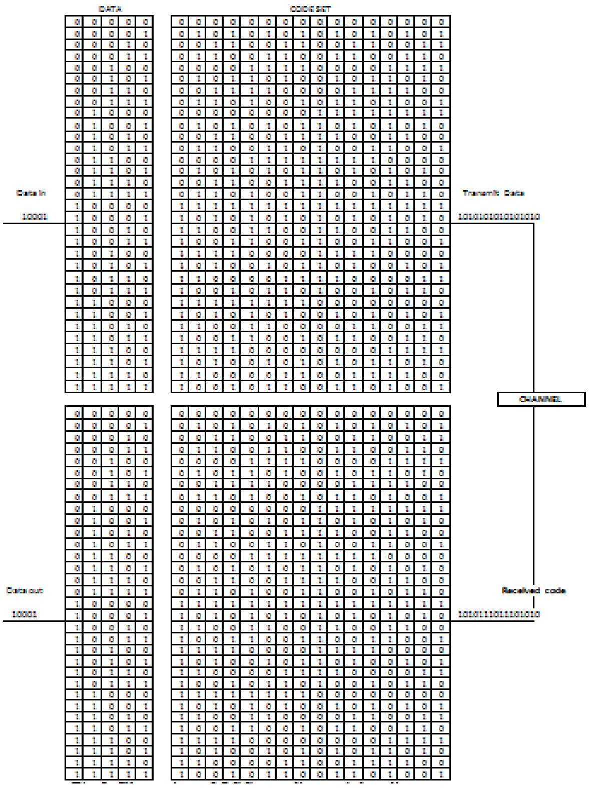


Fig2.:Illustration of OCC encoding and decoding

This paper deals with an enhanced technique (OCCMP).That combines Orthogonal Codes Convolution with Closest Match and vertical parity. Project expectations are that, the proposed technique should enhance both error detection and correction capabilities of Orthogonal Codes Convolution with a detection rate of 99.99%, and (n/2-1) bits correction capability in the received impaired n-bit code. For Designing and implementation purpose we are supposed to use 16 bit orthogonal convolution code.

This paper is organized as follows: review of previous work for performance of cyclic redundancy-check codes of 16-bit Redundancy, high-speed reed-solomon decoder for correction of both errors and erasures, Improved hamming code for error detection and correction, Error Control Coding based on Orthogonal Codes convolution(OCC) and OCCM is covered in Section2. In Section 3, we describe modeling of an enhanced technique (OCCMP) will use that combines Orthogonal Codes Convolution with Closest Match and vertical parity. In Section 4, we provide the comparison of detection and correction capabilities of different techniques ; Section 5 concludes the paper.

II. REVIEW OF DIFFERENT CODES (OCC, OCCM)

Hamming code is well known for its single-bit error detection & correction capability. To provide such a capability, it introduces 4 redundancy bits in a 7-bit data item. In the paper [1] improvement the redundancy bits will be appended at the end of data bits. This eliminates the overhead of interspersing the redundancy bits at the sender end and their removal at the receiver end after checking for single-bit error and consequent correction, if any. Further the effort needed in identifying the values of the redundancy bits is lower.

CRC codes with 16 check bits are investigated in [2]. All non-equivalent polynomials of degree16 which are suitable to be generator polynomials of CRC codes are checked. For the codes generated by these polynomials, properness, minimum distance and undetected error probability are determined for code lengths between 18 and 1024. With small exceptions, all the standard codes performance is not satisfactory in comparison with the best ones. Perhaps it is not acceptable to replace current standards with new polynomials from economical point of view. Single bit error correction can be employed in paper [3] of CRC-16 efficiently using FPGA. This approach is efficient both in terms of hardware and speed. The additional hardware required. But it corrects only one error.

Paper [7] shows the results of the orthogonal code implementation. This technique improved the error detection from 50% to 93% for 8-bit orthogonal code and gives 1 bit error correction. OCCM technique given in paper [8] combines the OCC and a technique Closest Match using Field Programmable Gate Array (FPGA), has led to the improvement of the detection capabilities of the 16 bit OCC from 71.88% to 93.57% .and gives the error correction of 3 bit.

An enhanced technique (OCCMP) used in [9] that combines Orthogonal Codes
Convolution with Closest Match and vertical parity. The results show that the proposed technique enhances both error detection and correction capabilities of8 bit Orthogonal Codes Convolution with a detection rate of 99.99%, and (n/2-1) bits correction capability in the received impaired n-bit code.and gives the error correction capability of 3 bit for 8 bit OCC.

III. MODELLING

To enhance the detection and correction capabilities of the OCCM technique, an improved method, OCCMP, based on Closest Match and vertical parity is proposed. This technique allows the transmission of several successive codes (16 codes in this paper) followed by their vertical parity byte. Because of the closure property of orthogonal codes, this parity byte, which is the exclusive sum (XOR) of sixteen orthogonal codes, is also an orthogonal code, and thus, the same technique used to detect and correct errors of each code in the block of data can be used to detect and correct errors in the parity byte. As soon as a byte is received, the system checks and corrects errors if the code is corrupted using the Closest Match technique. Once the receiver has checked and corrected the received 17 bytes, it calculates the vertical parity byte corresponding to the 16 data bytes and compares the new byte to the received parity byte in order to detect and correct more errors.

3.1 Transmitter

The transmitter includes four blocks: an encoder, a memory, a vertical parity generator and a shift register. The encoder encodes a k-bit data to n= 2^{k-1} bit orthogonal code using the look-up table (Fig. 2). After encoding, the code is stored in a memory and a parity byte is generated representing the columns; for each column, a parity bit is appended. In order to transmit the information, a shift register is used to convert these parallel bits in serial data .Fig.3 shows the block diagram of the implemented transmitter.

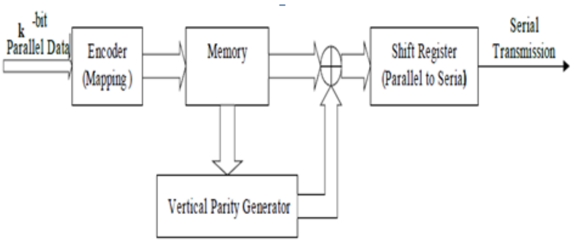


Fig.3: Block diagram of Transmitter

3.2 Receiver

As shown in Fig. 4, as soon as a block of n-bit code is received, the Closest Match technique is used to detect and correct a one bit error or multi-bit errors in the received code by comparing this received code with each code in the look-up table. A counter is used to calculate the number of 1's in the resulting signal. This number, rather than zero, shows an error or errors in the received code and the closest match code is used to correct it if only one bit error is detected. However, if the minimum count is associated with more than one combination of the orthogonal codes, the received code is left as it is and a flag is made for this code. Since the parity byte is also an orthogonal code, the same method is used in the received parity byte to detect and correct an error or errors.

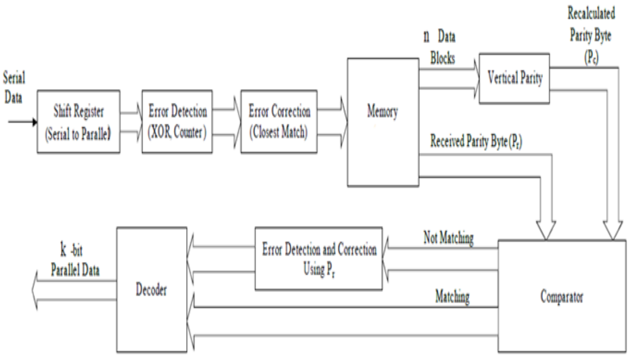


Fig.4:Block diagram of Reciever

After correcting the received sixteen codes, a new parity byte (Pc) is calculated for these corrected codes and "XOR" performance is conducted between the new and corrected received parity byte (Pr). The 1's in the resultant signal show the column with an odd number of error or errors. With the help of the flag made for the block of the corrupted code, the location of the error or errors is easily found. Decoding is performed after correcting the error or errors, and these 256 corrected bits are decoded to eight 5 bit data in order

3.3 Transmitter Simulation

After simulating encoder,Memory,vertical parity bit generator and parallel to shift register, the transmitter is simulated and results are shown in figure 7. The transmitter reset, using the reset signal „reset‟ . This resets the transmitter to the default value "00000". The encoder encodes a k-bit data set to n=2k-1 bits of the orthogonal code.After encoding code is store in memory and a parity byte is generated representing columns for each column parity byte is generated.then shift register transforms this code to a serial data in order to be transmitted. The transmitter is then enabled using the signal „data_rdy‟. This signal is HIGH when the data is ready. For example, the 5- bit data "00001" is encoded to "0101010101010101" 16-bit orthogonal code. The generated orthogonal code is then transmitted serially using a shift register with the rising edge of the clock. The bits are outputted through a signal „data_out‟ . The signal „data_out_rdy‟ is using to indicate the availability of output data. This signal is HIGH when the output data is ready.

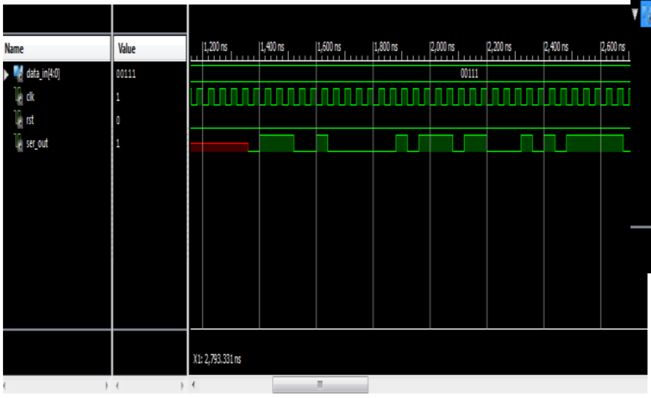


Fig.5:Simulated result of transmitter

3.4 Receiver Simulation

The receiver is simulated with its components such as serial to parallel converter and counter; and results are shown in figure 10. The receiver reset, using the reset signal „reset‟ . This resets the receiver to the default value "00000". The receiver is then enabled using the signal „data_rdy‟ . This signal is HIGH when the data is ready. For example, if the 16-bit data is "0101010101010101", is XORed with each combination of 16-bit orthogonal codes in the lookup table. The resulting 16-bit data is given as an input to counter. The counter counts the number of 1‟ s in each 16-bit XORed output. The minimum count value is "00000" for the orthogonal code is "0101010101010101". Therefore the associated 5-bit data is "00001". Another example, if the 16-bit data is "0101010101011101", is XORed with each combination of 16-bit orthogonal codes in the lookup table. The resulting 16-bit data is given as an input to counter. The counter counts the number of 1‟ s in each 16-bit XORed output.then by using closest match technique 16 combinations are taken out,and given to the memory addresses.vertcal parity (pc)is recalculated and XOR ed with the data obtained by receiving the vertical bit pariy from memory.then by using comparator check whether that Xo ring is matching or not.if matching then 16 bit data goes for decoding.otherwise we can detect and correct the errors by xo ring the the output of comparator with the 16 bit input parallel data.that will the original orthogonal code which will give to the decode.For Ex. for the orthogonal code is "0101010101010101". Therefore the associated 5-bit data is "00001".

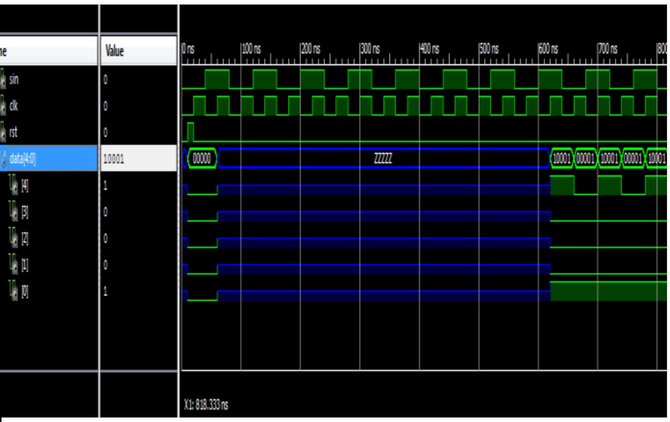


Fig.6: Simulated result of Reciever

3.5 Transmitter and Reciever Simulation

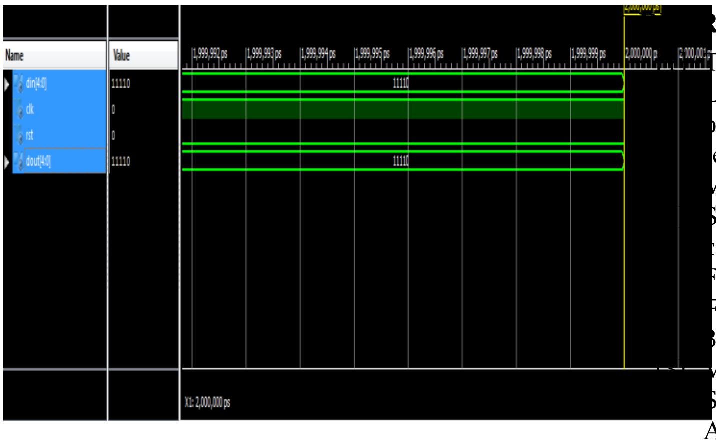
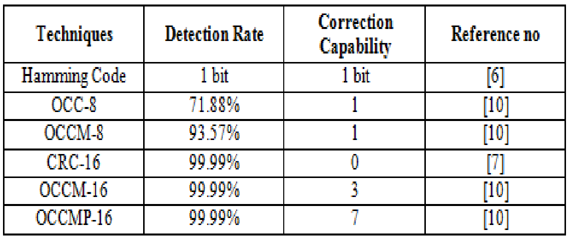


Fig.7 :Simulated result of Trans Reciever

IV. Comparison of detection and correction of different techniques



Techniques	Detection Rate	Correction Capability	Reference no
Hamming Code	1 bit	1 bit	[6]
OCC-8	71.88%	1	[10]
OCCM-8	93.57%	1	[10]
CRC-16	99.99%	0	[7]
OCCM-16	99.99%	3	[10]
OCCMP-16	99.99%	7	[10]

The detection rate for *k* block of n-bit code is

$$\frac{2^{kn} - Z}{2^{kn}} .100\% \qquad (1)$$

This will give for OCCMP-16 a detection rate of 99.99 %

V. CONCLUSION

In this method, propose work will compare an enhanced technique (OCCMP) With OCC, OCCM and combine with vertical parity using FPGA. Which will improve the Error correction and detection capability of convolution code up to 99.99% and correct up to (n/2-1)-bit of errors for n-bit orthogonal codes. With this method, the transmitter does not have to send the parity bit since the parity bit is known to be always zero. Therefore, if there is a transmission error, the receiver will be able to detect it by generating a parity bit at the receiving end. Finally, this work has the future scope of further improvement in orthogonal coding for large digital data processing.

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