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# Performance Study of Multiphase Multilevel Inverter

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**ABSTRACT**
Multi-phase motor drives are typically supplied from two-level voltage source inverters (VSIs). It is thus necessary to develop pulse width modulation (PWM) schemes for inverter control in order to utilize the benefits offered by multiphase motor drives. This paper presents a multiphase multilevel diode clamped inverter using sinusoidal pulse width modulation(SPWM) techniques as the control strategy. By increasing the level of inverter performance of the five phase inverter in terms of THD of voltages and current and DC offset voltages improved.

**Keywords –** Five phase inverter, Diode clamped inverter(DCI), THD, SPWM

## I. INTRODUCTION

Multiphase machines are AC machines characterized by a stator winding composed of a generic number "n" of phases. In today's electric drive and power generation technology, multiphase machines play an important role for the benefits compared to traditional three-phase ones. Earlier multiphase motor where not used widely because of the drawback that the supply for the multi phase motor was not available. But now a day's motor are not connected directly to the supply, they derive their excitation from power electronic converter most commonly voltage source or current source, the input stage of which is connected to the supply. The power electronic converters do not pose any limit on their number of legs. The number of output phases in an inverter is same as their leg. Hence, adding an additional leg to an inverter increases the number of output phases. Multi-level inverter technology has emerged recently as a very important alternative in the area of high-power high-voltage energy control.. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave[1]. Multilevel inverters can improve the voltage quality and reduce the voltage stress on the power electronic devices. The various topologies are used for the multilevel inverters. Among this the most commonly used topologies are neutral-point-clamped (NPC), flying capacitors (capacitor clamped),cascaded H-bridge. For three phase the above multilevel topologies are studied. In this paper we basically study the five phase diode clamped inverter having different levels and its comparison.

## II. FIVE PHASE INVERTER

Five phase inverter is used to fed the five phase drive. In five phase inverter, five legs are present each having two switches. Each phase is shifted by $72^0$ [2]. Conduction period of each switch is $180^0$.

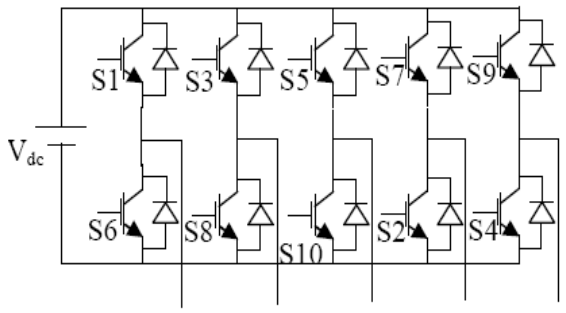



Fig. 1 Circuit diagram of five phase inverter

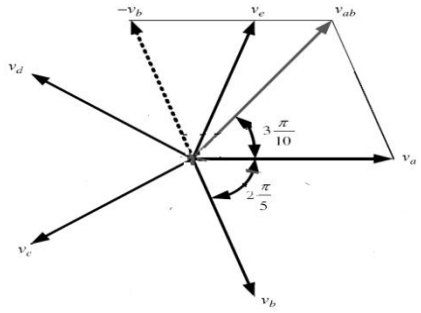
The basic circuit topology of five phase inverter is shown in fig 1 above. The five phases of inverter are denoted as A, B, C, D, E respectively. In five phase inverter three switches from the upper leg and two switches from the lower leg are turned on at a time and vice versa. The two switches from same leg of the inverter are complimentary to each other for example when one switch is on another switch is off so as to avoid short circuit. The switching sequence and mode of operation of five phase inverter are shown below:

| Mode | Switches ON | Terminal polarity |
|---|---|---|
| 9 | 1,7,8,9,10 | $A^+B^-C^-D^+E^-$ |
| 10 | 8,9,10,1,2 | $A^+B^-C^-D^-E^+$ |
| 1 | 9,10,1,2,3 | $A^+B^+C^-D^-E^+$ |
| 2 | 10,1,2,3,4 | $A^+B^+C^-D^-E^-$ |
| 3 | 1,2,3,4,5 | $A^+B^+C^+D^-E^-$ |
| 4 | 2,3,4,5,6 | $A^-B^+C^+D^-E^-$ |
| 5 | 3,4,5,6,7 | $A^-B^+C^+D^+E^-$ |
| 6 | 4,5,6,7,8 | $A^-B^-C^+D^+E^-$ |
| 7 | 5,6,7,8,9 | $A^-B^-C^+D^+E^+$ |
| 8 | 6,7,8,9,10 | $A^-B^-C^-D^+E^+$ |

Fig. 2 Mode of operation of five phase inverter

In five phase inverter we have adjacent and non-adjacent voltages. Relationship between line and phase voltages are as follows:

1.1 Adjacent phase voltages

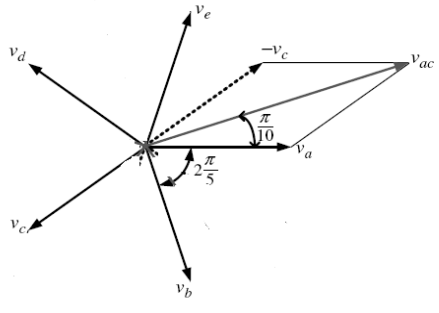



$$V_{ab} = V_a - V_b$$

$$V_L = 2 * \cos\left(3\frac{\pi}{10}\right) * V_a$$

$$V_L = 1.1756\, V_{ph}$$

1.2 Non-adjacent phase voltages




$$V_{ac} = V_a - V_c$$

$$V_L = 2 * \cos\frac{\pi}{10} V_a$$

$$V_L = 1.9025 V_{ph}$$

Some advantages of five-phase inverter are multiple of fifth harmonics are absent i.e. higher order harmonic gets eliminated, as number of phases are increased current in each phase is reduced therefore stress on each switch is less so life of switch get increased**.** The high phase order drive is likely to remain specialized applications where high reliability is demanded such as electric/hybrid vehicles, aerospace applications, ship propulsion and high power applications[3].

## III. CARRIER- BASED PWM SCHEME

This explains the principles of carrier-based PWM that are used for multilevel inverter. One of the most straightforward methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms. There are three alternative PWM strategies with differing phase relationships:

3.1 Phase disposition (PD)- All carrier waveforms are in phase.
3.2 Alternate phase disposition (APOD) – every carrier waveform is in out of phase with its neighbour carrier by $180^0$ .
3.3 Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are$180^0$ out of phase with those below zero.

## IV. MULTILEVEL INVERTER TOPOLOGIES

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. In general for a N level diode clamped inverter, for each leg 2 (N-1) switching devices, (N-1)*(N-2) clamping diodes and (N-1) dc link capacitors are required[4]. Here two-level, three-level and five-level diode clamped inverter are compared.

1.3 Two level inverter: In two level DCI, N=2 therefore two switching devices for each leg, no clamping diodes and one dc link capacitor are required.

1.4 Three level diode clamped inverter: In three level DCI we require four switching devices, two clamping diodes and two dc link capacitors for each leg of inverter.

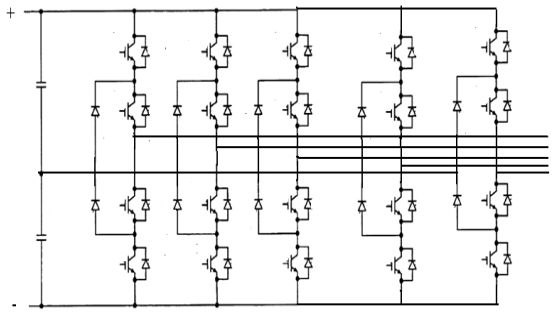


Fig. 3 Circuit diagram of three level DCI

1.5 Five level diode clamped inverter: In five level, we require eight switching devices, twelve clamping diodes and four dc link capacitors.

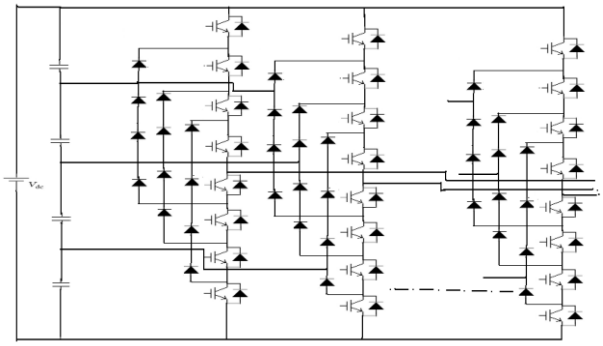


Fig.4 Circuit diagram of five level diode clamped inverter

## V. SIMULATION RESULTS

Table I
PARAMETER

| | |
|---|---|
| DC voltage | 100V |
| R-L load with p.f. | 0.8 |
| Capacitor | 0.3mF |
| Frequency | 50Hz |
| Carrier frequency | 2.1KHz |

1.6 Two level inverter

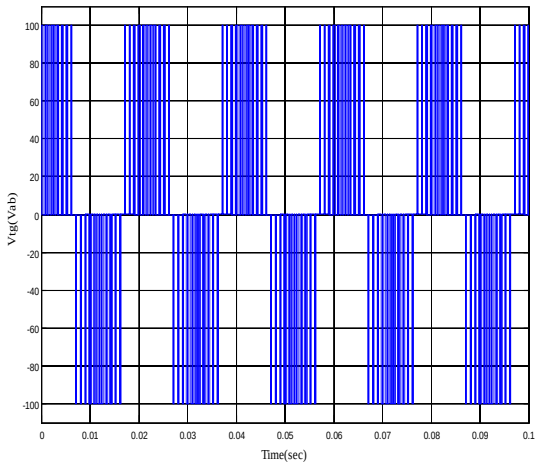



Fig. 5 Adjacent line voltage

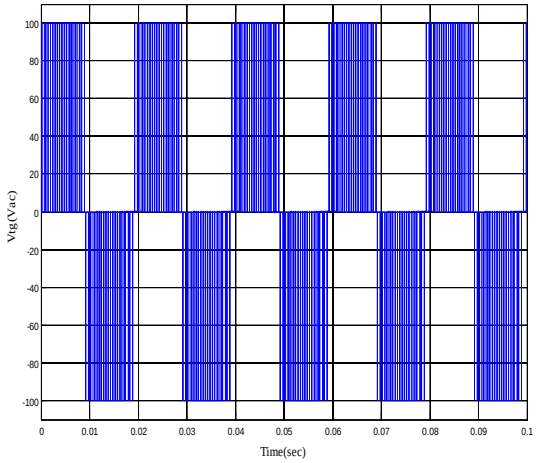



Fig. 6 Alternate line voltage

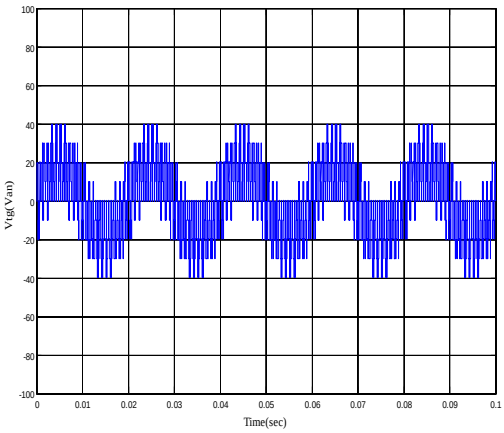



Fig. 7 Phase voltage

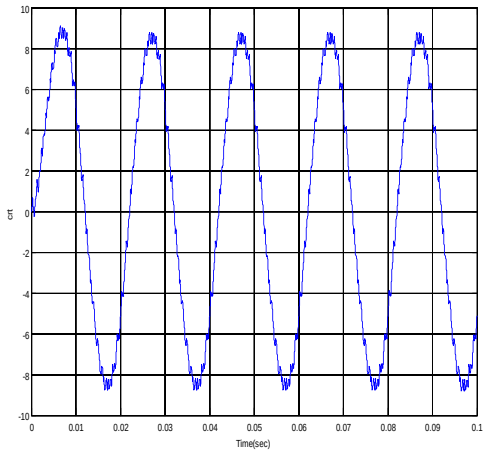



Fig.8 Line current

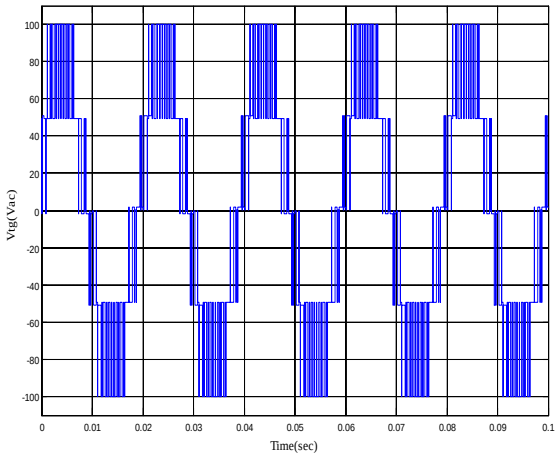



Fig. 11 Alternate line voltage

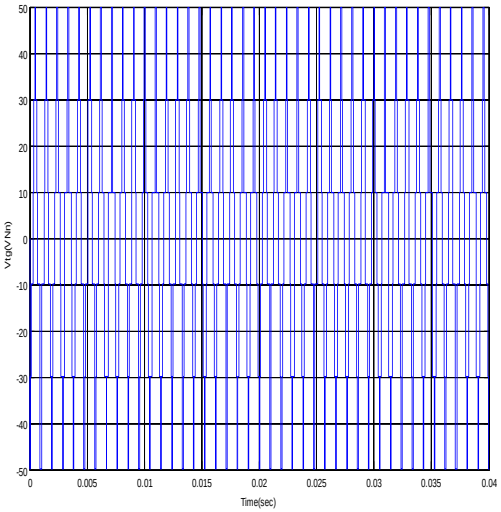



Fig.9 DC offset voltage

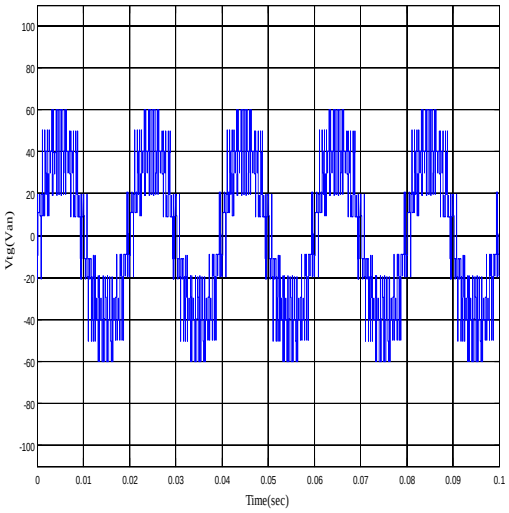



Fig. 12 Phase voltage

1.7 Three level diode clamped inverter

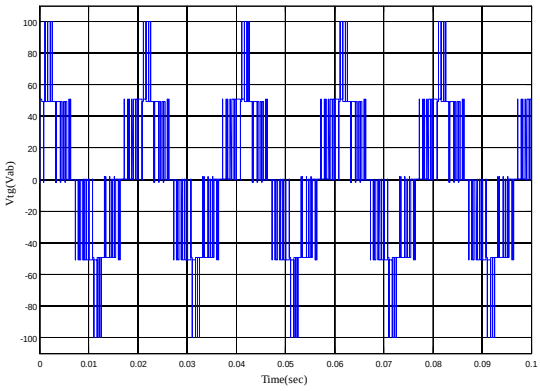



Fig. 10 Adjacent line voltage

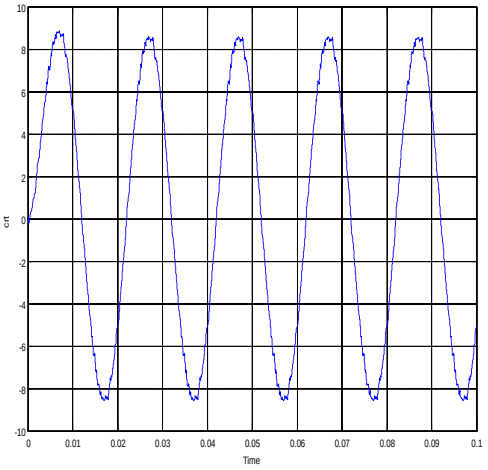



Fig.13 Line current

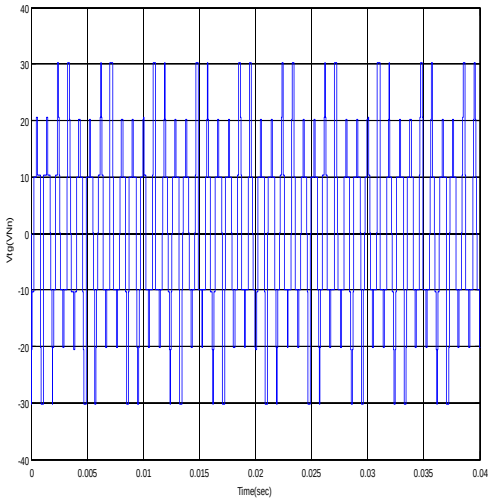



Fig.14 DC offset voltage

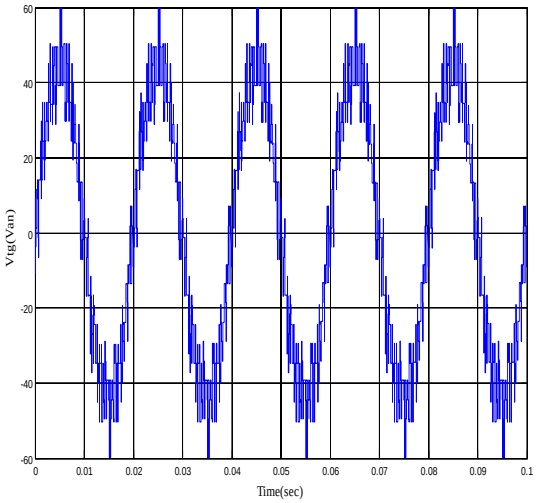



Fig. 17 Phase voltage

1.8 Five level diode clamped inverter

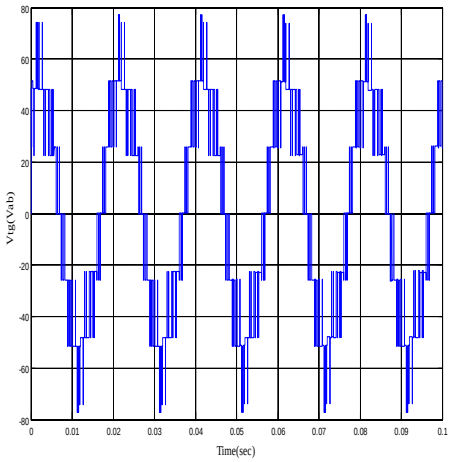



Fig.15 Adjacent line voltage

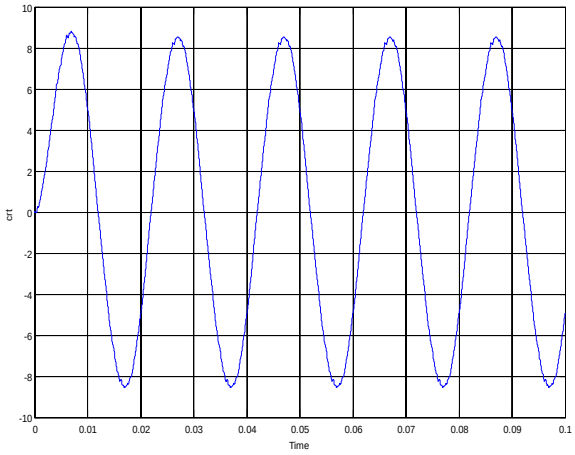



Fig.18 Line current

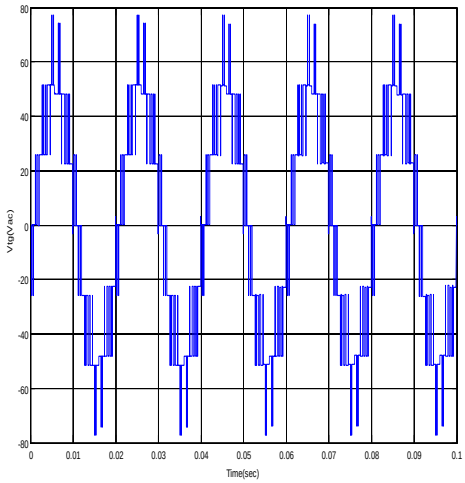



Fig.16 Alternate line voltage

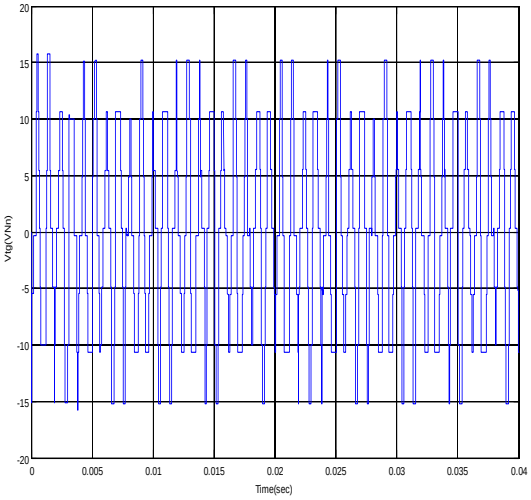



Fig.19 DC offset voltage

## VI. COMPARISON OF 2-LEVEL, 3-LEVEL AND 5-LEVEL DIODE CLAMPED INVERTER

Comparison is done on the basis of results obtained above.

Table II

| **THD** | **2-level** | **3-level** | **5-level** |
|---|---|---|---|
| Adjacent Line Voltage | 117.94% | 49.28% | 25.89% |
| Alternate Line Voltage | 70.25% | 36.40% | 24.95% |
| Phase Voltage | 86.23% | 40.27% | 20.36% |
| Line Current | 14.94% | 13.59% | 13.52% |

Table III

| **DC offset voltage** | **2-level** | **3-level** | **5-level** |
|---|---|---|---|
| | 50V | 30V | 15V |

## VII. CONCLUSION

Hence in this paper it is concluded that in five level diode clamped inverter, THD of line voltage, phases voltage and line current is decreased by 23.39%, 19.91%, 0.07% respectively as compared to three level diode clamped inverter. As it is seen that DC offset voltage get reduced in five level diode clamped inverter which increases life of insulation and improves reliability of motor.

## VIII. ACKNOWLEDGEMENTS

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