Realization of Reversilbe Full Adder & Reversible Full Subtractor using RPLA

D. Sarvani[1] and Y. Syamala[2]
Department of Electronics and Communication Engineering
Gudlavalleru Engineering College
Gudlavalleru, India

Y. Ratna Babu
Department of Electronics and Communication Engineering
Vignan's Lara Institute of Technology and Science
Vadlamudi, India

Abstract—*Reversible logic gates are very much in demand for the future computing technologies as they are known to produce Zero power dissipation.. Reversible logic circuits are of interests to power minimization having applications in low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. In recent years, reversible logic has emerged as a promising computing paradigm having application in low power CMOS and optical computing. The classical set of gates such as AND, OR, and EXOR are not reversible. In this paper, the authors have proposed the synthesis of combinational circuits using RPLA. Furthermore, the application is shown by implementing the full adder and full subtractor functions through it and the performance parameters are compared with the previous work.*

Keywords—Reversible logic; CMOS; Nanotechnology; RPLA

I. INTRODUCTION

This section provides an effective background of reversible logic with its definition and the motivation behind it.

A. Definitions

Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost generateskTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Furthermore, voltage-coded logic signals have energy of Esig = ½CV2 and this energy gets dissipated whenever switching occurs in conventional (irreversible) logic implemented in modern CMOS technology. It has been shown that reversible logic helps in saving this energy using charge recovery process [10]. Reversible circuits are those circuits that do not lose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. Thus, an NXN reversible gate can be represented as

Iv= (I1, I2, I3, I4 …IN)

Ov= (O1, O2, O3 ….ON).

Where Iv and Ov represent the input and output vectors respectively. Classical logic gates are irreversible since input vector states cannot be uniquely reconstructed from the output vector states. There are a number of existing reversible gates such as Fredkin gate [3, 4, 5], Toffoli Gate (TG) [3, 4] and Feynman gate [6].

B. Proposed Contribution and Motivation behind the Work

The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design [7], optical computing [8], quantum computing [9] and nanotechnology [10]. The most prominent application of reversible logic lies in quantum computers.

A quantum computer can be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performs an elementary unitary operation on one, two or more two–state quantum systems called quits. Each quit represents an elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible, hence quantum networks effecting elementary arithmetic operations such as addition [12] multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, Quantum Arithmetic must be built from reversible logic components [10]. Furthermore, programmable logic arrays (PLAs) have a number of medical and industrial applications, such as ultrasonic flaw detection. The reasons stem from the fact that PLAs are considerably faster than high end DSPs. They provide the cost effective solution to the exponentially increasing needs of industrial electronics. Thus, seeing the benefits of programmable logic array and reversible logic in industrial electronics and applications, the authors propose the reversible programmable logic array (RPLA) designed using

reversible gates. In order to demonstrate the proposed architecture of RPLA, a 3 input RPLA which can perform any 2^8 functions using the combination of 8 min terms (2^3) is also designed [9].

II. BASIC REVERSIBLE GATES

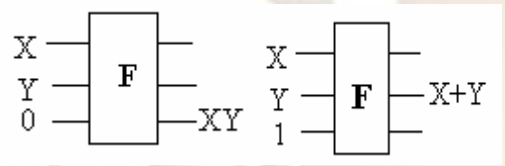
There are a number of existing reversible gates in literature. Fredkin [3, 4, 5] and Feynman gates [3] are used to construct the reversible PLA. A brief description of the gates is given below [1].

A. Fredkin Gate

Fredkin gate [3, 4, 5], is a (3*3) conservative reversible gate originally introduced by Petri [4, 5]. It is called 3*3 gates because it has three inputs and three outputs. The input triple(x1, x2, x3) associates with its output triple (y1, y2, y3) as follows:

$$y_1 = x_1$$
$$y_2 = (\neg x_1 \wedge x_2) \vee (x_1 \wedge x_3)$$
$$y_3 = (x_1 \wedge x_2) \vee (\neg x_1 \wedge x_3)$$

Figure 1.a and Figure 1.b show the implementation of the Fredkin gate as OR and AND functions respectively.



(a) (b)

Fig. 1. Fredkin gate as (a) OR function (b) AND function

B. Toffoli Gate

Toffoli [3, 4] gives constructions for an arbitrary reversible or irreversible function in terms of a certain gate library. However, his method makes use of a large number of temporary storage channels, i.e. input-output wire-pairs other than those on which the function is computed (also known as ancillary bits). Sasao and Kinoshita show that any conservative function (f (x) is conservative if x and f (x) always contain the same number of 1s in their binary expansions) has an implementation with only three temporary storage channels using a certain fixed library of conservative gates, although no explicit construction[5] .

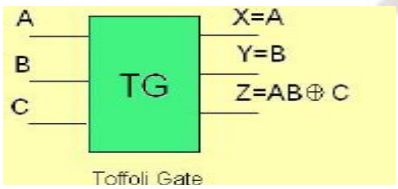


Fig. 2. Toffoli gate

C. Feynman Gate

Feynman gate [3] is a 2*2 one-through reversible gate shown in Figure 2. It is called 2*2 gate because it has 2 inputs and 2 outputs. One through gate means that one input variable is also the output. The input double (x1, x2) associates with its output double (y1, y2) as follows.

y1=x1;

y2=x1 ⊕ x2;

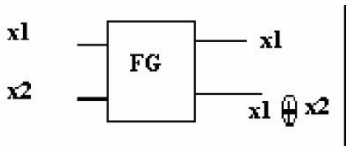


Fig. 3. Feynman gate

Figure (3a) shows the implementation of Feynman gate for copying the input and Figure (3b) shows the implementation of it for generating the complement of the input.

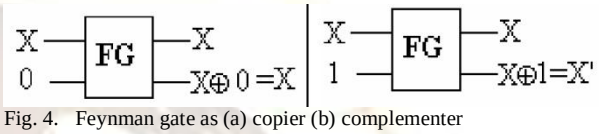


Fig. 4. Feynman gate as (a) copier (b) complementer

III. PROPOSED REVERSIBLE PROGRAMMABLE LOGIC ARRAY

In this paper, the authors have proposed the architecture of reversible PLA called RPLA [10]. The architecture of reversible PLA is shown in Figure 4. The RPLA consists of reversible AND array designed from reversible Toffolli gate and Feynman gate, in which the Feynman gates are used to avoid the problem of fan-out and for generating the complement of the inputs. The reversible AND array realizes the selected product terms of the input variables. The reversible OR array designed from reversible Fredkin gates is used to generate various possible functions of the product terms (outputs of reversible AND array).

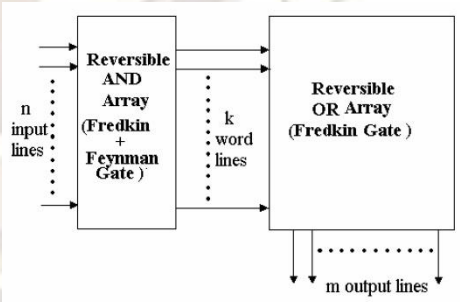


Fig. 5. Proposed Reversible PLA (RPLA) Architecture

IV. DESIGN OF THREE INPUT REVERSIBLE PLA

In order to demonstrate the actual design of the proposed reversible PLA (RPLA), a 3 input RPLA is shown in Figure 4 In Figure 4, the AND functions required to realize the AND array are implemented using reversible Fredkin gates. The application of Fredkin gate as an AND and OR gate has already been discussed in the previous section. In the AND array,

the complement of the inputs are required and moreover fan-out is not allowed in reversible logic, thus Feynman gates are used to complement and replicate the signals when required. The designed 3 input reversible AND array will generate 8 product terms as outputs, which are combined using the reversible OR array designed using the Fredkin gate, to generate the required output functions.[8]

A. Applications of the designed 3 Input RPLA

The designed 3 input RPLA is used to implement the 1 bit full adder and 1-bit subtractor. The 1-bit full adder as shown in Figure 5 is implemented using the 3 input RPLA by generating the product terms in the full adder truth table through the AND array, and then appropriately combining the product terms through the reversible OR array to finally generate the required SUM and CARRY output functions. Similarly, the 1-bit subtractor as shown in Figure 8 is implemented to generate the Difference and Borrow output functions. Figure 5 shows the full adder using reversible PLA and its quantum depth is shown in fig. 6. Figure 7 shows the quantum representation of fig. 5. Reversible full subtractor is analyzed in fig. 8 and fig. 9.

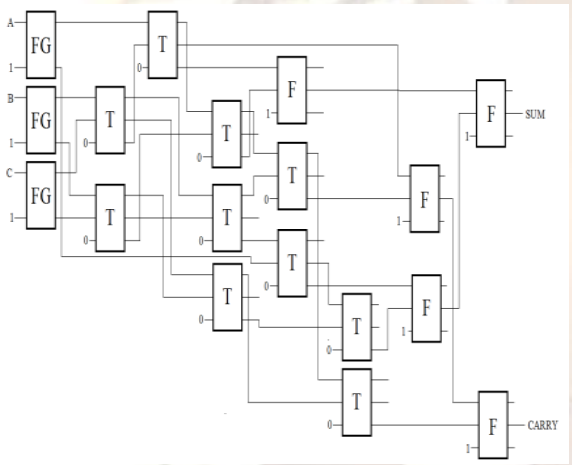


Fig. 6. Full adder using RPLA

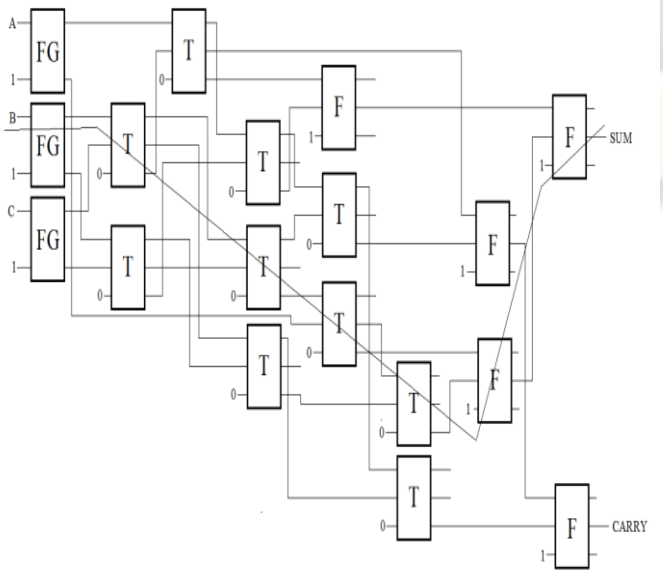


Fig. 7. Quantum depth of Reversible Full adder

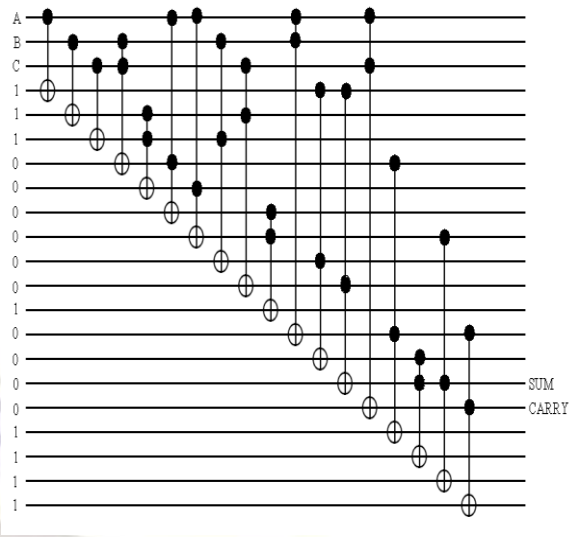


Fig. 8. Quantum diagram of Reversible Full adder using RPLA

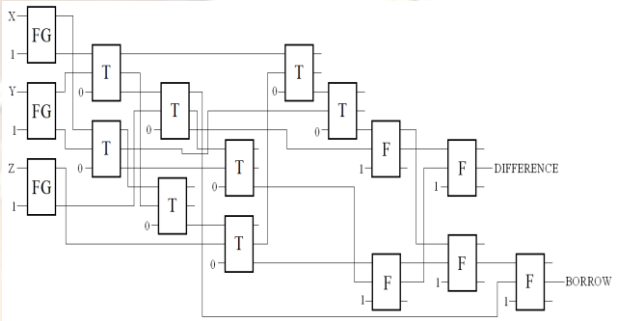


Fig. 9. Full subtractor using RPLA

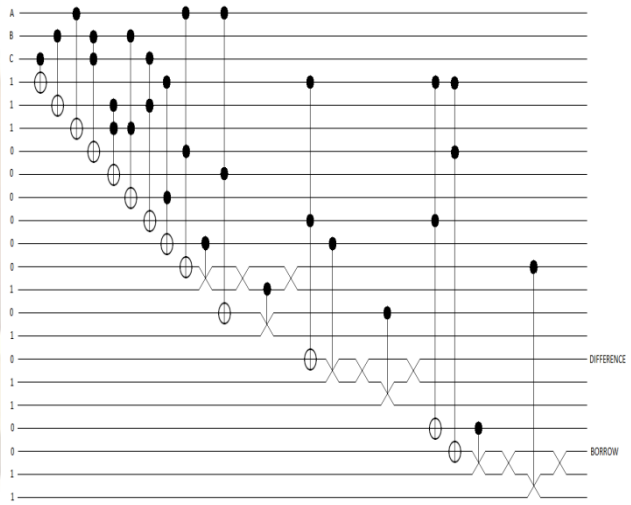


Fig. 10. Quantum diagram of reversible full subtractor using RPLA

V. RESULTS

The proposed reversible full adder and full subtractor circuits are compared in terms of quantum parameters in table 1 and table 2 respectively.

TABLE I. COMPARISON OF QUANTUM PARAMTERS FOR REVERSIBLE FULL ADDER USING RPLA

Quantum Parameter	Existing Design	Proposed Design
Gate Count	70	18
Quantum Cost	170	78
Garbage Outputs	74	19
Constant Inputs	70	18
Quantum Depth	29	31
Logical Calculation	95α+145β+25γ	23α +30β +5γ

TABLE II. COMPARISON OF QUANTUM PARAMTERS FOR REVERSIBLE FULL SUBTRACTOR USING RPLA

Quantum Parameter	Existing Design	Proposed Design
Gate Count	70	16
Quantum Cost	170	78
Garbage Outputs	74	17
Constant Inputs	70	16
Quantum Depth	29	31
Logical Calculation	95α+145β+25γ	23α +30β +5γ

CONCLUSION

The focus of this paper is on the proposal of reversible programmable logic array (RPLA) using reversible gates. The 3 input RPLA which can generate any 2^8 functions using the combination of 8 min terms (2^3) is also successfully designed. Finally, the application of the RPLA is demonstrated by implementing the reversible 1-bit full adder and subtractor. It is also demonstrated that the proposed design is highly optimized in terms of number of reversible gates and garbage outputs. It is expected that the proposed work will provide to a new paradigm to the arena of reconfigurable computing. In the existing design there are so many unused lines ,the circuit is modified by removing those unused lines .Gate count is decreased there by these circuits are used for Low Power Consumption and garbage outputs are abruptly reduced as shown in the previous section.

The basic goals in reversible logic are to minimize the number of reversible gates and garbage outputs. Thus, the proposed RPLA is designed in an optimal manner.

REFERENCES

[1] R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp. 183 -191, 1961.

[2] C.H. Bennett, "Logical Reversibility of Computation", IBM J. Research and Development, pp. 525-532, November 1973.

[3] E. Fredkin, T Toffoli, "Conservative Logic", International Journal of Theory. Physics, 21(1982), pp.219 -253.

[4] T. Toffoli., "Reversible Computing", Tech memo MIT/LCS/TM -151, MIT Lab for Computer Science (1980).

[5] Alberto LEPORATI, Claudio ZANDRON, Giancarlo MAURI," Simulating the Fredkin Gate with Energy{Based P Systems", Journal of Universal Computer Science, Volume 10,Issue 5,pp 600 -619.

[6] Himanshu Thapliyal and M.B Srinivas, "Novel Reversible "TSG" Gate and Its Application for Designing Reversible Carry Look Ahead Adder and Other Adder Architectures", Tenth Asia-Pacific Computer Systems Architecture Conference (ACSAC05), Singapore, October- 26, 2005, pp 805-817.

[7] GSchrom, "Ultra Low Power CMOS Technology", PhD Thesis, Technischen Universidad Wien, June 1998.

[8] E. Knil, R. Laflamme, and G.J Milburn, " A Scheme for Efficient Quantum Computation with Linear Optics", Nature, pp 46 -52, Jan 2001.

[9] M. P. Frank, "Introduction to reversible computing: motivation, progress, and challenges", In Proceedings of the 2nd Conference on Computing Fron-tiers, pages 385–390, 2005.

[10] Himanshu Thapliayal and Hamid R.Arabnia"center for vlsi and Embedded System Technologies,RPLA Using Fredkin and Feynman Gates For industrial Electronics and Applications" In the Proceedings of the 3rd conference on computing Frontiers -pages 250-255,2001.

[11] M. Nielsen and I. Chaung, "Quantum Computation and Quantum Information", Cambridge University Press, 2000. R.C. Merkle, "Two Types of Mechanical Reversible Logic", Nanotechnology,4:114 -131,1993.

[12] Vlatko Vedral, Adriano Bareno and Artur Ekert, "Quantum Networks for Elementary Arithmetic Operations", arXiv:quant-ph/9511018 v1, nov 1995.