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A Novel Low-Power Charge Pump Architecture Based On Charge Sharing And Multistep Charging

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ABSTRACT—In electronic applications, due to need for continuous power reduction, charge pumps are widely used in integrated circuits (ICs). In this paper a new power saving concept for classical four-phase charge pump is introduced. This new charge pump architecture is based on concepts of multi-step charging and the charge sharing. Both the concepts are capable of reducing the overall power dissipation by 18.27% compared to the classical four-phase charge pump with 11V output voltage. The charge pump based upon the above concepts has been designed and simulated using Mentor Graphics Pyxis Schematic using 2.5 V supply voltage and 180 nanometer (nm) technology.
Keywords—Charge pump, EEPROM, NVMs, charge sharing

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I. INTRODUCTION

Charge pump is a circuit which is used to charge upwards to produce DC voltages that are greater than the applied voltage. Nowadays, many ICs require multiple voltages which can be easily generated using a charge pump. Therefore, such circuits are applied to the non volatile memories (NVMs), such as flash memory and electrically erasable programmable read-only memory (EEPROM) for erase or write functions on various devices.

Classical charge pumps are based on the oldest architectures of Cockcroft and Walton voltage multiplier. But in case of Cockcroft Walton multiplier, chip monolithic integration is difficult to achieve. Therefore, to overcome this limitation, Dickson voltage multiplier uses diode associated MOSFETs. But it has inferior conversion efficiency due to drops in threshold voltage across the charge transfer device. Due to this, many configurations were developed to reduce the effect of the V_{TH} on the conversion efficiency of the charge pump by nullifying the cause of the body effect. Charge pump architecture which employs a four-phase clock and boost capacitors on the switch transistor to decrease the influence of V_{TH} has been developed.

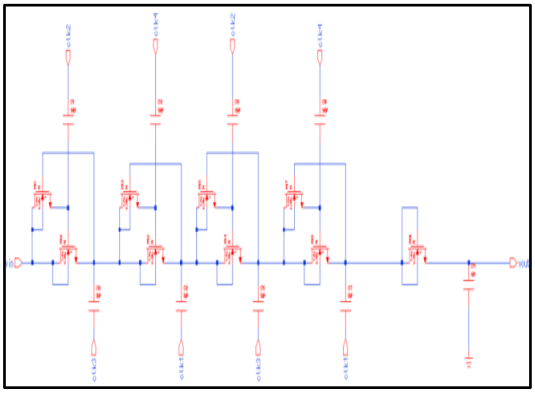

Fig. 1 A conventional charge pump

Now, to reduce the overall power consumption and without affecting the final output voltage level i.e. not degrade the conversion efficiency of the desired charge pump ,the concepts of charge sharing and combination of charge sharing and multistep charging have been proposed in this paper. The above mentioned concepts are applied to the conventional four phase boosted charge pump whose circuit has been shown in Fig. 1. CLK3 and CLK4 are two overlapped clocks. During charge transfer, two non overlapped clocks CLK2 and CLK4 are used to increase the gate voltage of the charge transfer device thereby reducing the body bias effect.

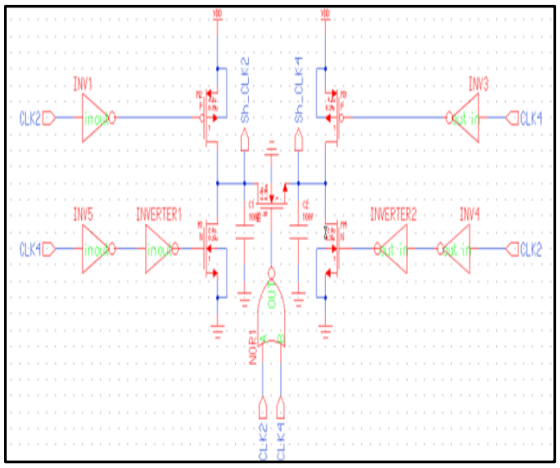

Fig. 2 Charge sharing clock generator with two new overlapped clocks CLK2 and CLK4.

The remaining part of the paper is described as follows; Section II gives the brief overview of charge sharing concept, in the III section, the multi-step concept is discussed. In Section IV, simulation results are shown and conclusion of the work is given in Section V.

II. CHARGE SHARING CHARGE PUMP

Conventional four phase charge pump is improved by using the technique called charge sharing. It is a phenomenon in which after charging of capacitor, charge is reused to charge another capacitor in a circuit. It is also called charge reuse. As designed charge pump has four stages therefore charge is transferred from one stage to another to increase the output voltage. Therefore each capacitor of every stage is charged to VDD during first half clock cycle and at the end of operation all capacitors are discharged to ground. After that, remaining charge is used for further charging of another capacitor. By increasing the charging steps we can reduce the power consumption of charge pump.

In conventional charge pump, charging and discharging are done in one step and to increase the number of steps, two new clocks are designed which charges and discharges in two steps. For this CLK2 and CLK4 of conventional charge pump are used to generate two new clock signals.

The working operation of charge sharing clock generator is described as follows: As shown in Fig. 2 charge sharing clock generator consists of two tristate drivers, one NMOS transistor, one NOR gate and two capacitors for charge sharing. When CLK 2 is at logic 1 whereas CLK 4 is at logic 0, then the NOR gate is OFF and capacitor c1 is charged but c2 is grounded. When CLK 2 goes to logic 0 and CLK 4 remains at logic 0, then NOR gate is ON due to this all the charge from c1 is transferred to c2.When CLK 2 still at logic 0 and CLK 4 is at logic 1, NOR gate is OFF and c1 is discharged to ground and c2 is fully charged as all the charge is transferred to it. As the two new clocks are applied on the conventional charge pump, the new architecture formed and it's named as modified charge pump-I. The only difference between these designs is in number of the charging steps as in conventional charge pump, capacitors charges in single step but in modified charge pump-I, capacitor charges in two steps. But both the charge pumps have the same architecture for improved output voltage.

III. MULTISTEP CHARGING

Multistep charging as the name suggests, charging of capacitor in multiple steps. Before this, the charge sharing technique was applied to conventional four phase charge pump which charges the pump capacitor in two steps and because of this power is relatively reduced. For further reducing the power of conventional charge pump, charge sharing technique is combined with multistep charging. When both of these concepts are applied to conventional charge pump then the new configuration is introduced and it's named as modified charge pump-II and in this design, power is greatly reduced.

When an ideal capacitor is charged from 0 to VDD volts, then it acts like a voltage source. But only half of the energy is actually stored by the capacitor which is given by ½.C.VDD². Thus, half of this energy is lost in the switch resistance. Many strategies have been devised to save this energy out of which multistep charging is one of the popular techniques.

It has been derived mathematically that if the capacitor is charged using P voltage steps, then the total energy delivered by the voltage source is given by P+1/2.P .C.V² and the total dissipated energy is equal to1/P .C.V², so that the total energy saving, in percentage, is equal to P-1/2.P.

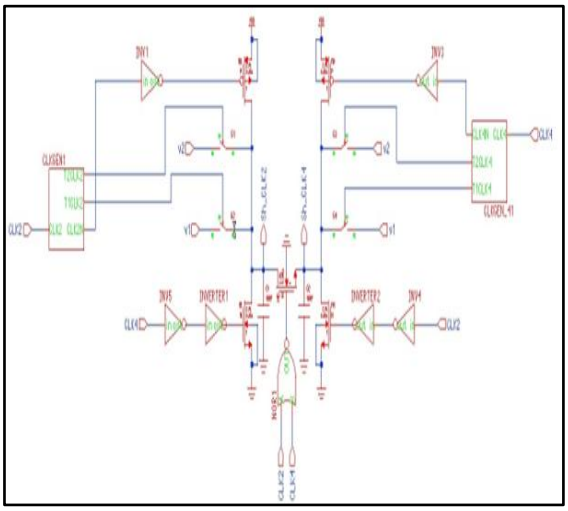

Fig. 3 Multi-step charging clock generator

It can be inferred that using more number of steps results into less energy dissipation. But this theoretical inference is difficult to achieve in practice

since a circuit designed to charge with a higher number of voltage steps leads to more power losses as more number of voltage sources and control switches are required. Therefore, three steps are chosen so that the total energy saved is more compared to charging using a single step. In this context, if the three step charging technique is applied to the charge sharing concept, the subsequent charge pump will be capable of reducing more power compared to the modified charge pump-I.

The circuit shown in Fig. 3 describes the generation of the two clock signals which are used to charge and discharge pump capacitors in three steps. The clock generation scheme is similar to the circuit shown in Fig. 2 but in this case additional signals are required to charge the capacitors. These are external voltages given by V1=1.9V and V2=2.2, C1clk2, and C2clk2 , and C1clk4 and C2clk4.

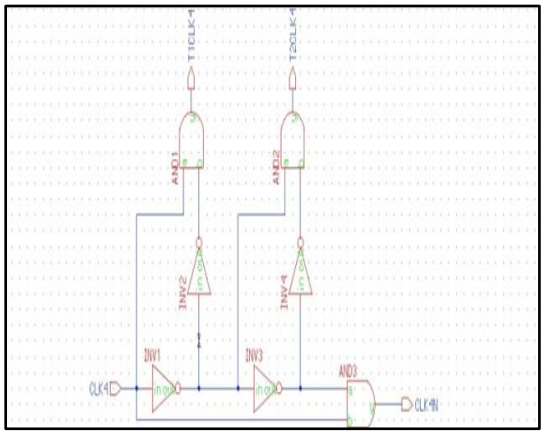

Fig. 4 Generation of clocks CLK_DLY and CLK_DLY2

Fig. 4 shows a non-overlapping clock generator which is used to produce the delay signals CLK_DLY and CLK_DLY2 from an input clock signal CLK. These signals are used to produce further two new clock signals which are then used to charge the pump capacitor in three steps. Fig. 14 shows the waveforms of the signals .It can be seen that to reach the final voltage a total of 3 steps have been used.

IV. SIMULATION RESULTS

In this paper, power consumption of conventional charge pump is reduced by designing the two clock generators. These can be used to obtain the two new configurations of charge pump. Comparisons among these designs are simulated using Mentor Graphics Pyxis Schematic tool.

Table I summarizes the design parameters of the charge pump.

Table I
Design Parameters

Design Parameters	Values
Technology	350 nm
Stage Number N	4
Clock Frequency f	16.67 MHz
Load Capacitance C_L	10 pF
Pumping Stage Capacitance C_P	5 pF
Boost Stage Capacitance C_B	100 Ff

Fig. 5-8 shows the simulation waveforms of conventional charge pump.

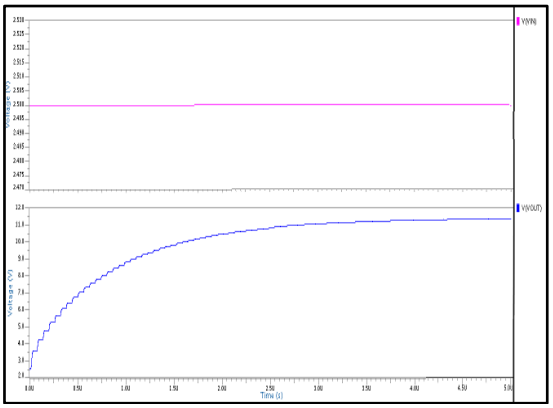

Fig. 5 Transfer characteristics of conventional charge pump

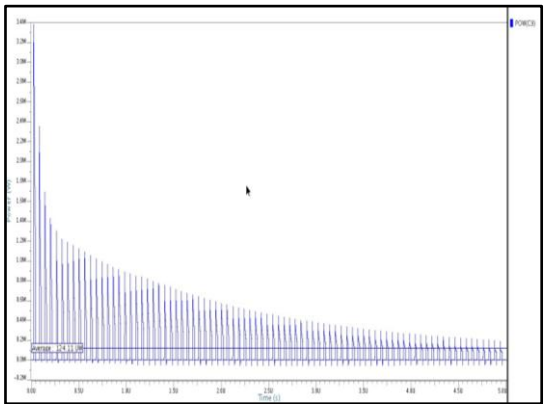

Fig. 6 Power dissipation of conventional charge pump

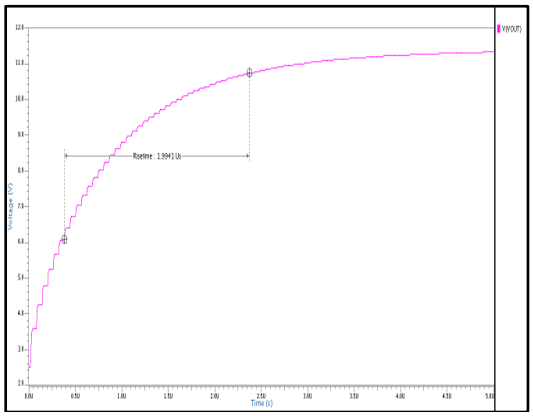

Fig.7 Risetime of conventional charge pump

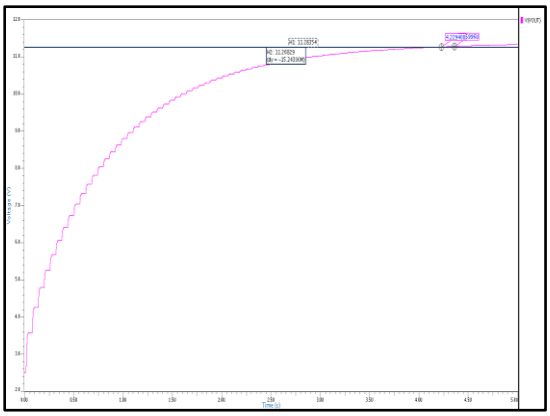

Fig. 8 Ripple voltage of conventional charge pump

Fig. 9 shows the waveforms of two new clocks Sh_CLK2 and Sh_CLK4 generated by the charge sharing clock clock generator. These two clocks charges the capacitor in two steps. Fig. 10-13 shows the simulation waveforms of modified Charge Pump-I.

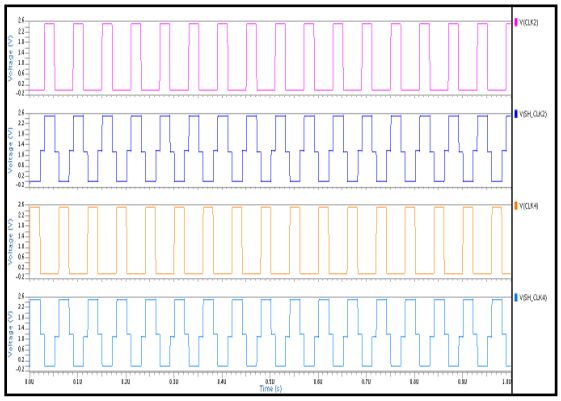

Fig. 9 Sh_CLK2 and Sh_CLK4 are two new clocks for charging the pump capacitors

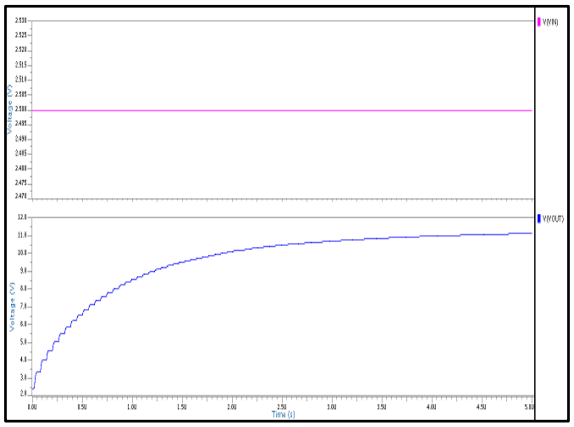

Fig. 10 Transfer characteristics of modified charge pump-I

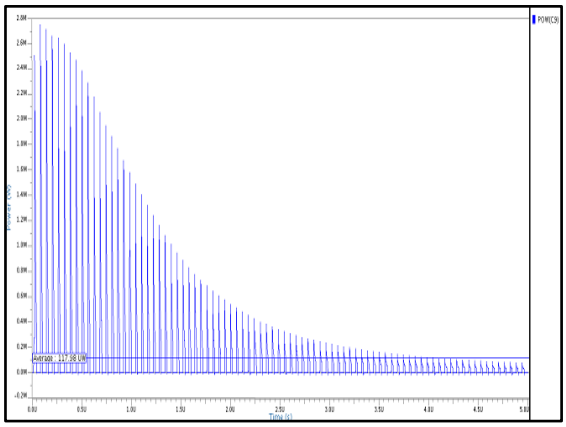

Fig. 11 Power Dissipation of modified charge pump-I

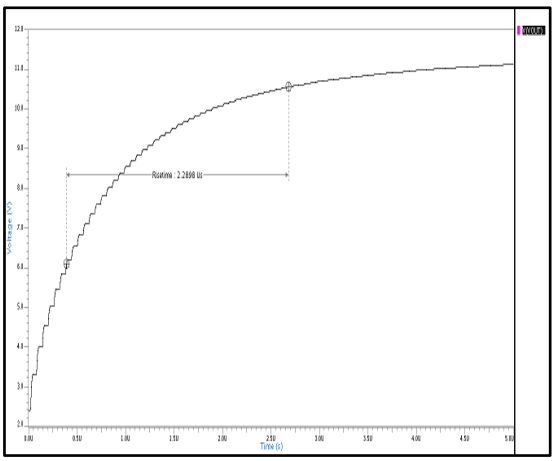

Fig. 12 Risetime of modified charge pump-I

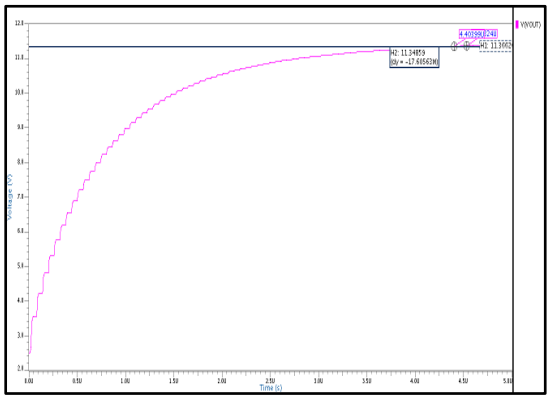

Fig. 13 Ripple voltage of modified charge pump-I

The input voltage to charge pump is 2.5 V and the intermediate voltages used in case of multi-step charging are V1=1.9 V and 2.2 V respectively.

Fig. 14 shows the new waveforms of clocks Sh_CLK2 and Sh_CLK4 which charges the capacitor in three steps. These clocks are further used to reduce overall power consumption of charge pump. Fig. 15-18 shows the simulation waveforms of three steps charging and power results of modified charge pump-II.

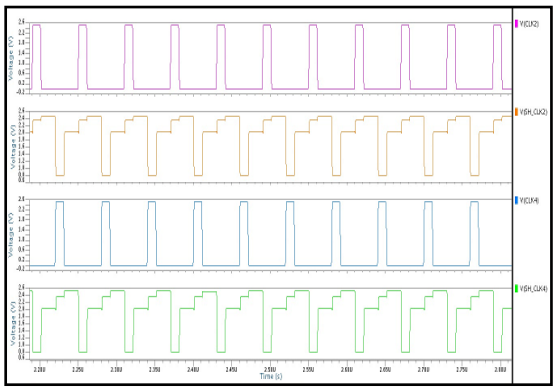

Fig. 14 Sh_CLK2 and Sh_CLK4 are two new clocks for charging the pump capacitors

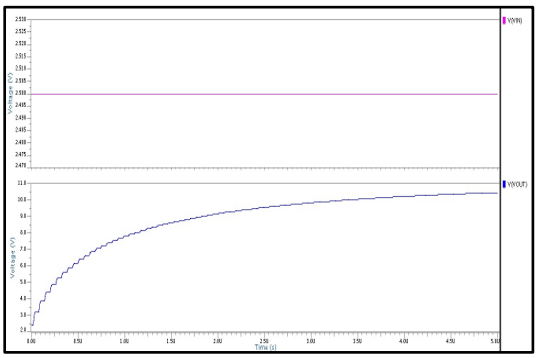

Fig. 15 Transfer characteristics of modified charge pump-II

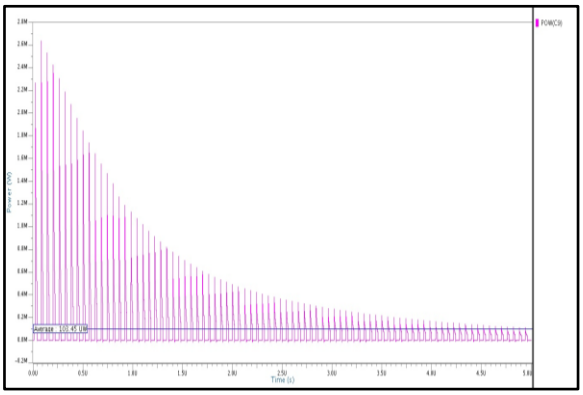

Fig. 16 Power Dissipation of modified charge pump-II

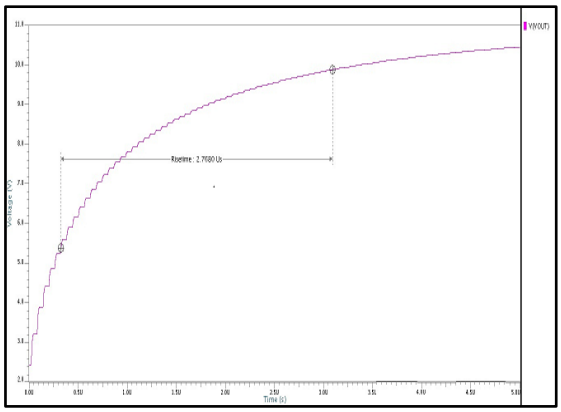

Fig. 17 Risetime of modified charge pump-II

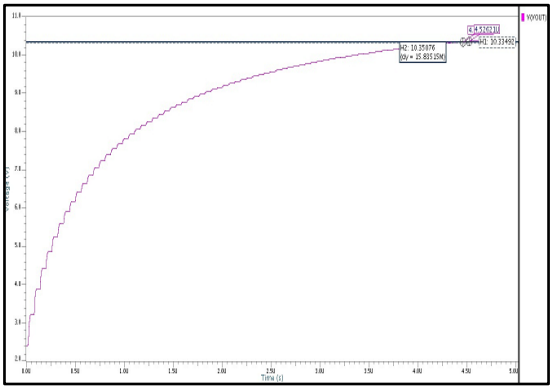

Fig. 18 Ripple voltage of modified charge pump-II

For an input voltage of 2.5V, the pumped up output voltage is approximately 11 V for 4 stages. The specifications of the conventional charge pump have been compared against the modified charge pump-I and the modified charge pump-II and the results have been summarized in the following table.

Table II
Charge Pump Configurations Comparison

Parameters	Conventional Charge Pump	Modified Charge Pump-I	Modified Charge Pump-II
Output Voltage (V)	11	11	10.7
Power Dissipation (µW)	124.11	117.98	103.45
Ripple(mV)	15.243	17.6	15.83
Rise Time (µs)	1.9941	2.289	2.768

V. CONCLUSION

In this work, a new architecture for reducing the power dissipation in the charge pump has been proposed. By using charge sharing, capacitance charging is done in two steps instead of one. And by combining this concept with the multi-step charging, additional power minimization can be achieved by charging the capacitance in multiple steps. Power dissipation has been reduced by 18.27% compared to the conventional charge pump architecture.

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