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Window Based Stereo Image Depth Mapping On Fpga

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ABSTRACT
The human eye structure is like that it can recognize the depth of an object in front of them. They combine two images known as stereo images into a single image which helps to identify the depth of an object. From the stereo images, we can find a disparity image used for 3D image reconstruction. The disparity image generation is also possible through MATLAB and embedded platform, but there is one issue to generating disparity image is a low frame rate. To overcome that issue FPGA having better features like high clock frequency, parallel processing and re-programmable device.
Keywords – Disparity image, FPGA, Sum of Absolute Difference (SAD)

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I. INTRODUCTION

Stereo vision is a research area in computer vision, so it used in many applications. Usually, the stereo vision system has two cameras to capture two different images. A stereo matching is one of the main concepts in the stereo vision system. The main purpose of stereo matching is to find a disparity between stereo images [1][2][3]. Stereo matching obtains the depth information from a pair of an image in which corresponding pixels have displacement.

(a) (b)

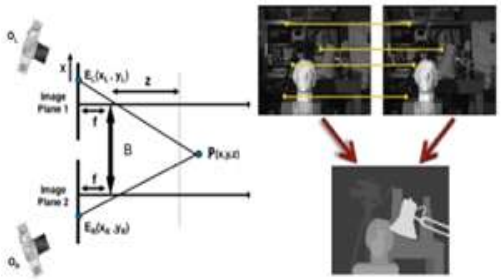


Fig.1. (a) Stereo vision camera setup (b) Disparity map from stereo image

The general process of extracting depth information from the stereo image is pixel shifting from corresponding images and calculate their disparity [see also Fig.1(b)]. In the stereo image system, two cameras are placed almost in the same horizontal line with some distance between them, similar to human eye position. The camera setup in Fig.1(a), the distance to point P (x, y, z) can be estimated. The two points denoted as E_L (X_L, Y_L) and E_R (X_R, Y_R) on the same horizontal line. The point E_L of the left image is shifted some distance as point E_R of the right image in same horizontal line. The shifted point decides that disparity of that point or pixel.

Stereo matching methods having three types (1) pixel or window matching, (2) semi-global method such as the Dynamic Time Warp (DTW) algorithm and (3) global method based on the graph cut algorithm. Window base algorithm of stereo matching is to search the best matching pixel block along the raster scan line. Implementing the stereo matching algorithm in FPGA hardware using the window-based algorithm is possible. Mathematically SAD (Sum of Absolute Differences) can be calculated using the following Eq.1. Therefore, we focus here only on the window-based method which sequentially searches the SAD (Sum of Absolute Differences) for stereo matching along the raster scan line.

$$\text{SAD} = \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} |R(i,j) - L(i,j)| \qquad (1)$$

II. LITERATURE SURVEY

The stereo image used for generating a disparity image and disparity image used for 3D image reconstruction. The dedicated hardware architecture for generating disparity image is implemented on FPGA using the window based stereo algorithm is possible. For best window matching, we used the SAD (Sum of Absolute Difference) algorithm which generates disparity pixel.

2.1 Window Based Stereo Matching Algorithm:

The window-based algorithm for stereo matching is the best matching pixel block along the raster scan line. The reference image (left image) to a given pixel block is scan along the raster scan line on the target image (right image) with the same pixel block. Fig.2. shows that window size of 3 x 3 used for window matching using the SAD algorithm. The Sum of Absolute Difference (SAD) algorithm used to match two window blocks which are position at (i, j) of a left image I_L and (i, j-k) of a right image I_R.

SAD (i, j) = $\min_{k \in R} r(i, j, k)$ (2)

The minimum locator compares all SAD value and generates disparity pixel value at (i, j) location.

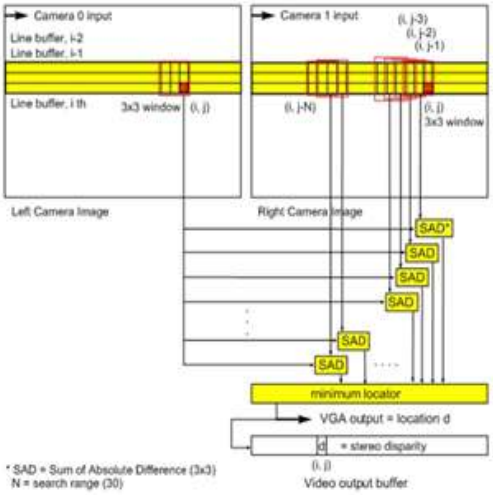
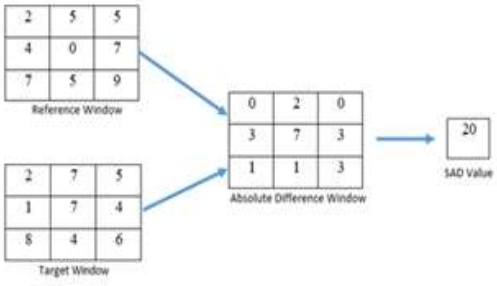


Fig.2. FPGA architecture of stereo matching to calculate disparity pixel 'd'.

2.2 Sum Of Absolute Difference (Sad) Algorithm:

In digital image processing, the Sum of Absolute Differences (SAD) is a measure of the similarity between image blocks. It is calculated by taking the absolute difference between each pixel in the original block and the corresponding pixel in the block being used for comparison. The windows are comparing namely reference window and target windows. Absolute difference window gets after a magnitude difference between each pixel. The summation of all pixel value makes SAD value.

Fig.3 SAD algorithm



III. PROPOSED SYSTEM

The proposed system designed such that it can generate a disparity image from stereo images. For this design, required two images stored in BRAM memory with 256 x 256 in resolution. The design system is designed using the concept know as window based stereo matching algorithm. To improved previous window matching algorithm speed of execution, this design is useful.

3.1 HARDWARE ACCELERATION OF FPGA

The stereo matching algorithm implementation on FPGA is one of the challenging tasks. For stereo matching required two images namely target image (right image) and the reference image (left image). Both images having the size of 256 x 256 which stored in BRAM. The address controller required to generate an address for BRAM having the stereo image for processing and disparity image for storing. The data controller module is main block for generating stereo to disparity image. For window matching having two module namely left and right data window having size 1 x 3 and 1 x 32 respectively. The window matching block compare window using Sum of Absolute Difference (SAD) module and best matching data forward to disparity map block. Using the best matching data disparity map generate disparity pixel value. The disparity value stored in disparity image RAM with respective address.

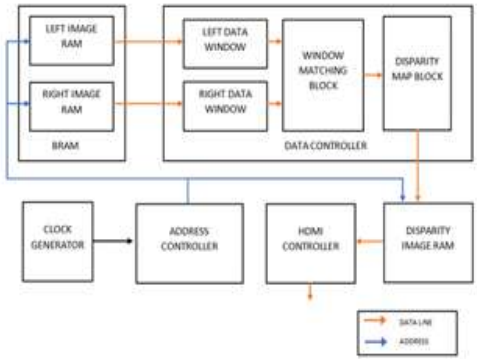


Fig.4 Block diagram of proposed system

3.2 PROCEDURE METHODOLOGY

The proposed method required a stereo image for a disparity image. The image which is in the format of (.png or .jpg) are format resize in 256 x 256 resolution and convert it into text format (.txt) by MATLAB tools. In future, if configure two cameras to FPGA according to stereo image specification then we can get disparity image in real time. For this proposed method, we focus on the stored image to get a disparity image. These stereo images are ideal images which are used in many researchers to work in stereo images. The text format images having each pixel in 8-bit size such as two bits for blue and three bits for red and green. The text format images are again converted in (.coe)

format simply by renaming. This format is used to stored images in FPGA having memory called BRAM (Block RAM).

As shown in Fig.4, the address controller generates an address to BRAM to extract images and load into the data window. The data window stored a number of pixels for further processing. The data window is nothing but a shift register. In the proposed system, data window shift pixel value on each clock cycle. Each clock cycle left data window compares with right data window parallelly. For window matching, we used the Sum of Absolute Differences (SAD) algorithm. As shown in Fig.5, the SAD algorithm matches all windows and gives their output to a disparity map block. Disparity map block finds minimum SAD value and generates disparity pixel value. Disparity pixel value generates after comparing the position of minimum SAD value. This proposed system generates each disparity pixels on each clock cycle. It may be improved the speed of generating disparity images and get a solution on low frame rates. For more research in future, it will improve the accuracy and sharpness of disparity images. For high-resolution images required more clock cycle and it reduces the performance of the disparity generation in real time. This Proposed system will improve the performance of the disparity generation.

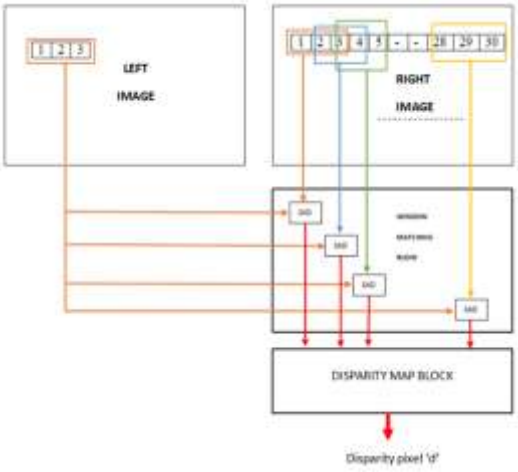


Fig.5 FPGA architecture of calculating disparity pixel value 'd'

IV. RESULTS

As shown in Fig.6 and Fig.7, are simulation waveform in VIVADO software. In Fig.6 shows that first disparity pixel of first horizontal line generates after 32 pixels load in both data windows. It required two more clock cycle to generates disparity output. On each clock cycle generates disparity pixel value. In Fig.7 shows that last disparity pixel of last disparity pixel of first horizontal line.

Fig.6 Simulation waveform (first disparity pixel of first horizontal line).

Fig.7 Simulation waveform (last disparity pixel of first horizontal line).

From Table.1, the comparison between FPGA with MATLAB tools and embedded platform in terms of a number of frames per second. The FPGA is a reprogrammable and dedicated hardware device which improve frame rate.

System Used for Disparity Generation	Maximum Frame Rate
MATLAB tools	20 frames/sec
Embedded Systems	30 frames/sec
FPGA	50-60 frames/sec

Table.1. Comparison between MATLAB vs Embedded system vs FPGA

As shown in Fig.8 and Fig.9, is proposed system input and output images. The disparity image shows that depth information of that object. If the object is near from camera shown by red color shades and the object is far from the camera shown by blue color shades.

(a) (b) (c)

Fig.8 Proposed system input and output images (Teddy) (a) left images (b) right images (c) disparity images

(a) (b) (c)

Fig.9 Proposed system input and output images (Cones) (a) left images (b) right images (c) disparity images

V. CONCLUSION

The proposed system design generates a disparity image from a stereo image. The window-based stereo matching algorithm is implemented on the FPGA board. The design used for generating a disparity image reduces the number of the clock cycle for execution. It will directly improve the performance in real time conversion of disparity image. This design increased the frame rate up to 50-60 frames per second. The stereo vision is a research area in computer vision therefore if we implement advanced concept on FPGA then we can improve our disparity image.

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