RESEARCH ARTICLE OPEN ACCESS

CMV analysis of 5-level Cascaded H-Bridge MLI with equal and unequal DC sources using Variable Frequency SPWM Techniques

Mohd Esa*, Mohd Abdul Muqeem Nawaz** and Naheed***
**(Electrical Engineering Department, MJCET, Hyderabad-34*
*** (Electrical Engineering Department, MJCET, Hyderabad-34*
**** (Electrical Engineering Department, MJCET, Hyderabad-34*
Corresponding Author : Mohd Esa

ABSTRACT
This paper, investigates the Common Mode Voltage (CMV)between neutral point of the star connected RL load and system ground.CMV also known as zero sequence voltage results in adverse effects like bearing currents, shaft voltages and electromagnetic interference.CMV also causes premature failure of bearings of induction motor and is necessary to reduce. In this paper, Variable Frequency Sinusoidal Pulse Width Modulation (VFSPWM) techniques are used to investigate CMV in Cascaded H-Bridge Multilevel Inverter (CHB-MLI). Comparison of 5-level CHB-MLI with equal and unequal DC sources in terms of CMV is also presented. Simulation of circuit is carried out in MATLAB environment.
Keywords–CMV, CHB-MLI, VFSPWM

Date of Submission: 25-08-2018 Date of Acceptance: 08-09-2018

I. INTRODUCTION

Three phase inverters are normally used for high power applications. The main function of the inverter is to generate an ac voltage from a dc source voltage [1].In recent years multi-level inverters are used in high power and high voltage applications.The multilevel inverter output voltage has fewer harmonics compared to the conventional inverter.

Multilevel inverters include an arrangement of semiconductors devices and dc voltage sources to generate a stepped output voltage waveform. Multilevel inverters have drawn incredible interest in power industry due to their advantages such as higher efficiency, less common mode voltage, less voltage stress on power switches, less dv/dt ratio, no EMI problems and its suitability for high voltage and high current applications [2].

The operations, power ratings, efficiency &applications of multilevel inverter depends majorly on its topology. The most commonly known multilevel inverter topologies are Diode clamped Multilevel Inverter [3], Flying capacitor Multilevel Inverter [4], Cascaded-bridge Multilevel Inverter [5].Fig.1 shows classification of multilevel inverters. By combining these topologies with one another, hybrid inverter topologies have also been developed. In order to control MLI's, SPWM technique is used. In SPWM technique, triangular shaped high frequency carrier signal is compared with three phase sinusoidal reference signal to generate gating signals for triggering switches of inverter circuit.

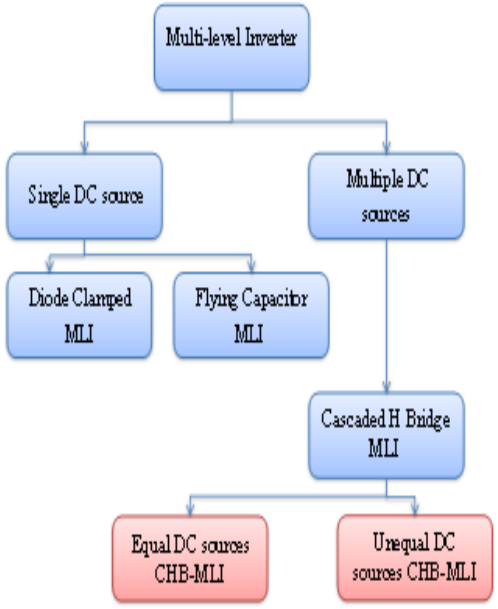

Fig.1. Classification of Multilevel Inverters

The frequency of reference signal determines the inverter output frequency & amplitude of reference signal controls the modulation index and in turn the rms output voltage [6]. The classification of SPWM techniques is shown in fig.2.In Multicarrier PWM technique for MLI, (m-1) triangular carriers are compared with sinusoidal modulating signal. Where m is output level of inverter. Thus for five level inverter four carriers are required.

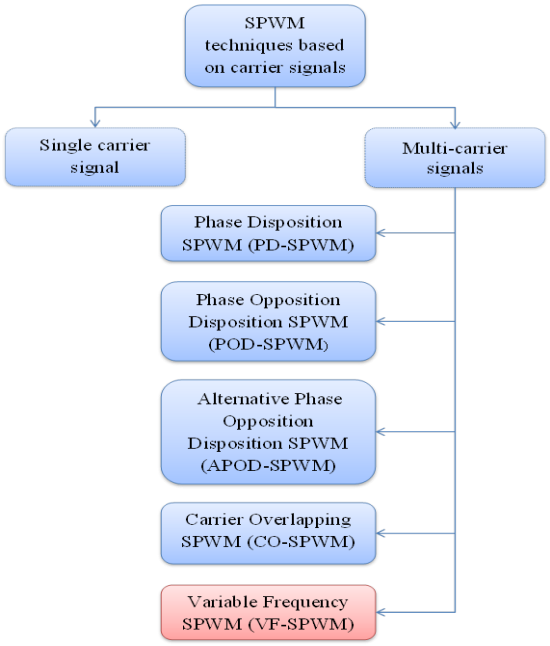

Fig.2. Classification of SPWM Techniques

The main drawback of conventional two level inverter is higher common mode voltage which can be reduced by using multilevel inverters. The voltage between system ground and load neutral is CMV.Equation (1) shows mathematical form of CMV [7], [8].

$$CMV=\frac{V_{ag}+V_{bg}+V_{cg}}{3} \quad (1)$$

Where V_{ag}, V_{bg}, V_{cg} are phase voltages

$$CMV=\frac{1}{3}\sum_{x=a}^{c} V_{xg}$$

PWM inverter produces high frequency and high amplitude CMV, which induces 'shaft voltages' on the rotor. Thus CMV is responsible for premature failure of bearing of induction motor when supplied from fast switching power components, so it is necessary to reduce CMV by selecting specific method [9].

In this paper, CMV is investigated in 5-level CHB-MLI using VF-SPWM Techniques. Load of R=100 Ohms and L=50e-3 Henry is considered.

II. CASCADED H-BRIDGE MLI

Cascaded H-Bridge multilevel inverter is also known as multi-cell inverter. In this topology, H-bridges with separate DC sources are connected in series. For m level inverter number of cells required is (m-1)/2.This topology requires less number of components as there are no extra clamping diodes or capacitors. The CHB-MLIs are best suited for medium and high power applications, this is possible because these MLIs has better harmonic spectrum at low switching frequencies.

The source of bridges HB_1, HB_3 and HB_5 is V_{dc1}.The source of bridges HB_4, HB_6 and HB_2 is V_{dc2}.when magnitude of voltage source given to HB_1, HB_3, HB_5, HB_4, HB_6 and HB_2 are equal then $V_{dc1}=V_{dc2}=V_{dc}$.The principle of operation for Phase A is shown in table 1.

Table 1: Switching states and output voltage for leg-1 of three phase 5-level CHB-MLI with equal voltage sources

Switching States HB1				Switching States HB2				V_{ao}
S11	*S18*	*S15*	*S14*	*S12*	*S17*	*S16*	*S13*	
1	0	0	1	1	0	0	1	$2V_{dc}$
1	0	0	1	0	0	1	1	V_{dc}
1	0	0	1	1	1	0	0	
0	0	1	1	1	0	0	1	
1	1	0	0	1	0	0	1	
0	0	1	1	0	0	1	1	0
0	0	1	1	1	1	0	0	
1	1	0	0	0	0	1	1	
1	1	0	0	1	1	0	0	
1	0	0	1	0	1	1	0	
0	1	1	0	1	0	0	1	
0	1	1	0	1	1	0	0	$-V_{dc}$
0	1	1	0	0	0	1	1	
0	0	1	1	0	1	1	0	
1	1	0	0	0	1	1	0	
0	1	1	0	0	1	1	0	$-2V_{dc}$

When magnitude of voltage source given to HB_1, HB_3, $HB_5$is greater than HB_4, HB_6 and HB_2 then $V_{dc1}>V_{dc2}$.When magnitude of voltage source given to HB_1, HB_3, HB_5 is lesser than HB_4, HB_6 and HB_2 then $V_{dc1}<V_{dc2}$. In such cases CHB-MLI is said to be supplied from unequal DC source. Switching pulses are given in similar manner as given in case of CHB-MLI with equal sources. In this paper, both CHB-MLI with equal and unequal DC sources are compared in terms of CMV.

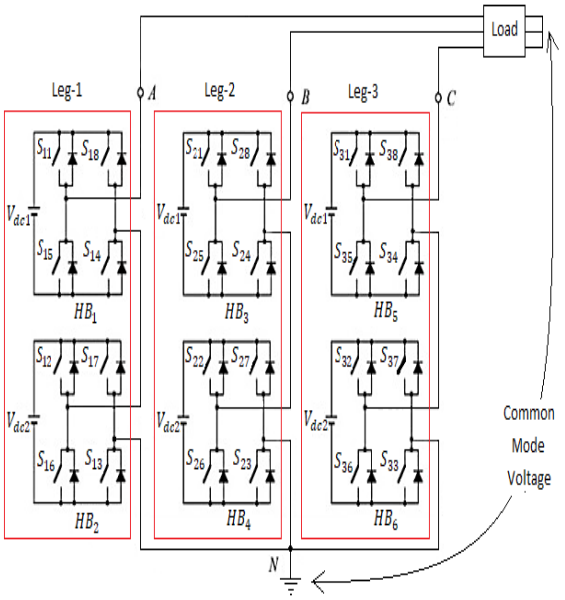

Fig.3. Three phase 5-level CHB-MLI

III. VARIABLE FREQUENCY SPWM TECHNIQUES

3.1 VFSPWM-A Technique

In VFSPWM-A technique, the frequency of triangular carrier signals which generates pulses when compared with reference sine wave to trigger switches S11, S15, S17 and S13 is 2000 Hz and the frequency of triangular carrier signals which generates pulses when compared with reference sine wave to trigger switches S18, S14, S12 and S16 is 1000 Hz. Principle is same to generate pulses for triggering switches of other two phases. Modulation Index is 0.9.Modulation Index is calculated mathematically from equation (2)

$$M.I=\frac{A_m}{A_{cr(m-1)}} \quad (2)$$

Where A_m is amplitude of modulating signal and A_{cr} is amplitude of carrier signal.

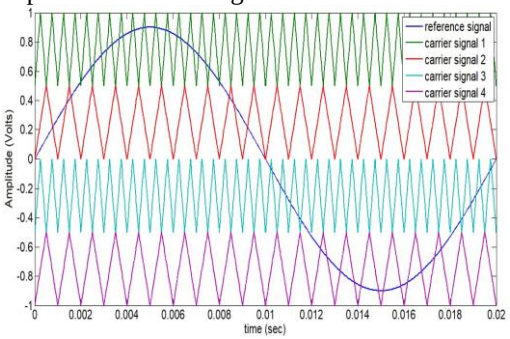

Fig.4. Carrier arrangement for VFSPWM-A controlled 5-level CHB-MLI

3.2 VFSPWM-B Technique

In VFSPWM-B technique, the frequency of triangular carrier signals which generates pulses when compared with reference sine wave to trigger switches S18, S14, S12 and S16 is 2000 Hz and the frequency of triangular carrier signals which generates pulses when compared with reference sine wave to trigger switches S11, S15, S17 and S13 is 1000 Hz. Principle is same to generate pulses for triggering switches of other two phases.Fig.5 shows carrier arrangement for VFSPWM-B controlled 5-level CHB-MLI

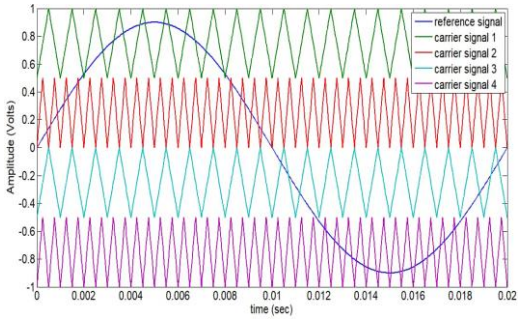

Fig.5. Carrier arrangement for VFSPWM-B controlled 5-level CHB-MLI

3.3 VFSPWM-C Technique

In VFSPWM-C technique, the frequency of triangular carrier signals which generates pulses when compared with reference sine wave to trigger switches S11, S15, S12 and S16 is 2000 Hz and the frequency of triangular carrier signals which generates pulses when compared with reference sine wave to trigger switches S18, S14, S17 and S13 is 1000 Hz. Principle is same to generate pulses for triggering switches of other two phases.Fig.6 shows carrier arrangement for VFSPWM-C controlled 5-level CHB-MLI.

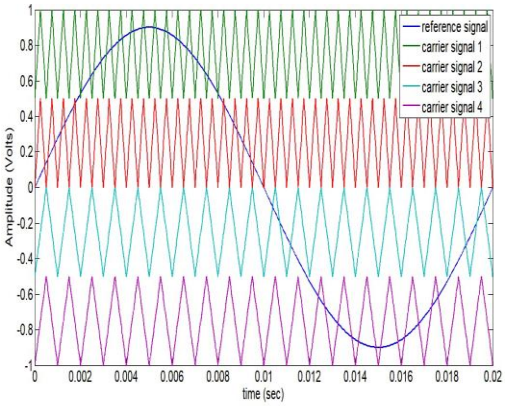

Fig.6. Carrier arrangement for VFSPWM-C controlled 5-level CHB-MLI

3.4 VFSPWM-D Technique

In VFSPWM-D technique, the frequency of triangular carrier signals which generates pulses when compared with reference sine wave to trigger switches S18, S14, S17 and S13 is 2000 Hz and the frequency of triangular carrier signals which generates pulses when compared with reference sine wave to trigger switches S11, S15, S12 and S16 is 1000 Hz. Principle is same to generate pulses for triggering switches of other two phases.Fig.7 shows carrier arrangement for VFSPWM-D controlled 5-level CHB-MLI.

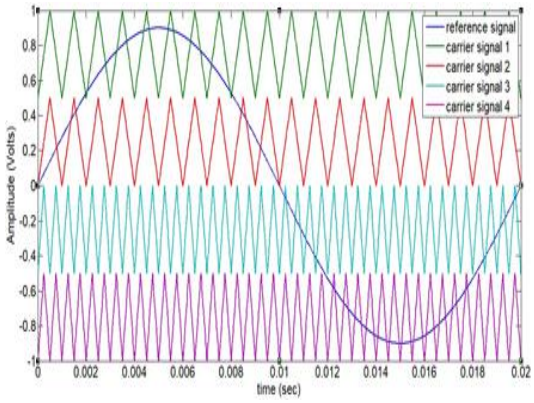

Fig.7. Carrier arrangement for VFSPWM-D controlled 5-level CHB-MLI

IV. SIMULATION RESULTS

4.1 Simulation results of VFSPWM-A controlled 5-level CHB-MLI

VFSPWM-A controlled 5-level CHB-MLI is simulated in Matlab/Simulink.Fig.8 shows phase voltage and CMV for VFSPWM-A controlled 5-level CHB-MLI with equal and unequal DC sources. The rms value of CMV is 32.43 V, 32.99 V and 35.92 V when supply DC sources are $V_{dc1} = V_{dc2}$,$V_{dc1} < V_{dc2}$ and$V_{dc1} > V_{dc2}$ respectively.

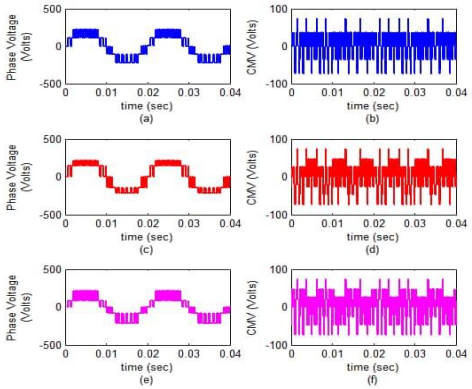

Fig.8.VFSPWM-A controlled five level CHB-MLI (a) phase voltage for CHB-MLI with equal DC sources i.e. $V_{dc1} = V_{dc2}$ (b) CMV for CHB-MLI with equal DC sources i.e. $V_{dc1} = V_{dc2}$ (c) phase voltage for CHB-MLI with unequal DC sources i.e. $V_{dc1} < V_{dc2}$ (d) CMV for CHB-MLI with unequal DC sources i.e. $V_{dc1} < V_{dc2}$ (e) phase voltage for CHB-MLI with unequal DC sources i.e. $V_{dc1} > V_{dc2}$ (f) CMV for CHB-MLI with unequal DC sources i.e. $V_{dc1} > V_{dc2}$

4.2 Simulation results of VFSPWM-B controlled 5-level CHB-MLI

VFSPWM-B controlled 5-level CHB-MLI is simulated in Matlab/Simulink.Fig.9 shows phase voltage and CMV for VFSPWM-B controlled 5-level CHB-MLI with equal and unequal DC sources. The rms value of CMV is 32.54 V, 33.24V and 35.84 V when supply DC sources are $V_{dc1} = V_{dc2}$,$V_{dc1} < V_{dc2}$ and $V_{dc1} > V_{dc2}$ respectively.

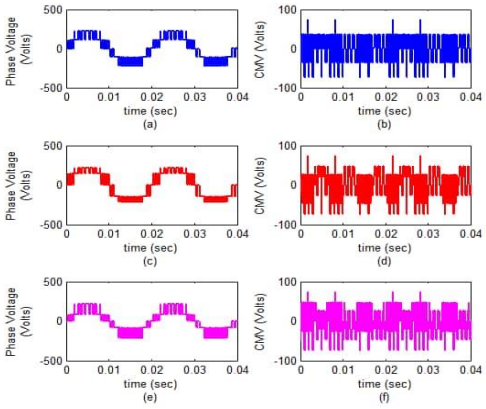

Fig.9.VFSPWM-B controlled five level CHB-MLI (a) phase voltage for CHB-MLI with equal DC sources i.e. $V_{dc1} = V_{dc2}$ (b) CMV for CHB-MLI with equal DC sources i.e. $V_{dc1} = V_{dc2}$ (c) phase voltage for CHB-MLI with unequal DC sources i.e. $V_{dc1} < V_{dc2}$ (d) CMV for CHB-MLI with unequal DC sources i.e. $V_{dc1} < V_{dc2}$ (e) phase voltage for CHB-MLI with unequal DC sources i.e. $V_{dc1} > V_{dc2}$ (f) CMV for CHB-MLI with unequal DC sources i.e. $V_{dc1} > V_{dc2}$

4.3 Simulation results of VFSPWM-C controlled 5-level CHB-MLI

VFSPWM-C controlled 5-level CHB-MLI is simulated in Matlab/Simulink.Fig.10 shows phase voltage and CMV for VFSPWM-C controlled 5-level CHB-MLI with equal and unequal DC sources. The rms value of CMV is 33.15 V, 33.71V and 36.48 V when supply DC sources are $V_{dc1} = V_{dc2}$,$V_{dc1} < V_{dc2}$ and $V_{dc1} > V_{dc2}$ respectively.

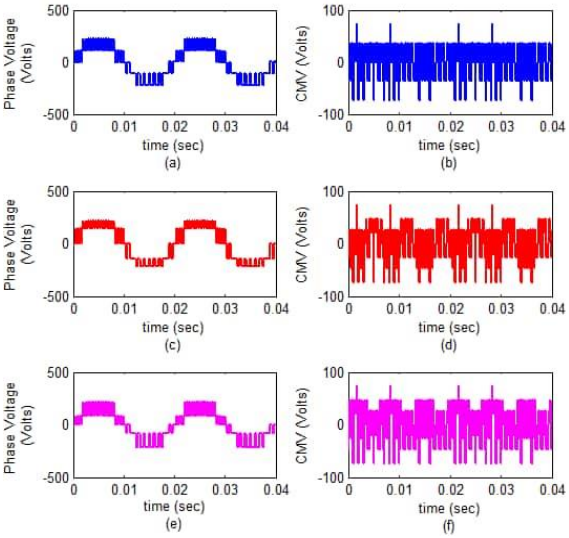

Fig.10.VFSPWM-C controlled five level CHB-MLI (a) phase voltage for CHB-MLI with equal DC sources i.e. $V_{dc1} = V_{dc2}$ (b) CMV for CHB-MLI with equal DC sources i.e. $V_{dc1} = V_{dc2}$ (c) phase voltage for CHB-MLI with unequal DC sources i.e. $V_{dc1} < V_{dc2}$ (d) CMV for CHB-MLI with unequal DC sources i.e. $V_{dc1} < V_{dc2}$ (e) phase voltage for CHB-MLI with unequal DC sources i.e. $V_{dc1} > V_{dc2}$ (f) CMV for CHB-MLI with unequal DC sources i.e. $V_{dc1} > V_{dc2}$

4.4 Simulation results of VFSPWM-D controlled 5-level CHB-MLI

VFSPWM-D controlled 5-level CHB-MLI is simulated in Matlab/Simulink.Fig.11 shows phase voltage and CMV for VFSPWM-D controlled 5-level CHB-MLI with equal and unequal DC sources. The rms value of CMV is 29.39 V, 30.32V and 33.26 V when supply DC sources are $V_{dc1} = V_{dc2}$,$V_{dc1} < V_{dc2}$ and$V_{dc1} > V_{dc2}$ respectively.

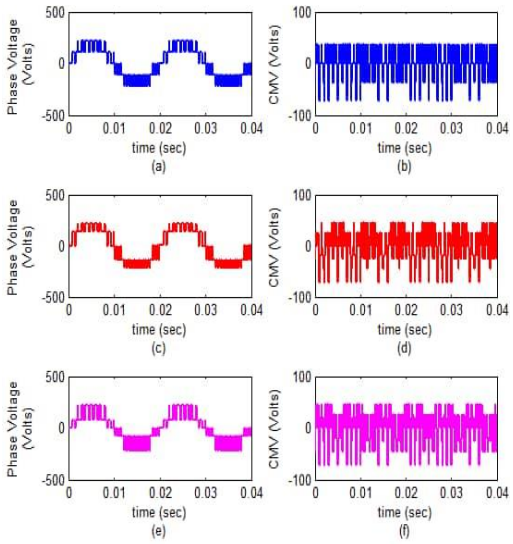

Fig.11.VFSPWM-D controlled five level CHB-MLI (a) phase voltage for CHB-MLI with equal DC sources i.e. $V_{dc1} = V_{dc2}$ (b) CMV for CHB-MLI with equal DC sources i.e. $V_{dc1} = V_{dc2}$ (c) phase voltage for CHB-MLI with unequal DC sources i.e. $V_{dc1} < V_{dc2}$ (d) CMV for CHB-MLI with unequal DC sources i.e. $V_{dc1} < V_{dc2}$ (e) phase voltage for CHB-MLI with unequal DC sources i.e. $V_{dc1} > V_{dc2}$ (f) CMV for CHB-MLI with unequal DC sources i.e. $V_{dc1} > V_{dc2}$

Table 2: CMV for VFSPWM controlled 5-level CHB-MLI

DC input sources	CMV in volts for Various VFSPWM techniques			
	A	*B*	*C*	*D*
V_{dc1}=110 V V_{dc2}=110V (equal DC sources)	32.43	32.54	33.15	29.39
V_{dc1}=80 V V_{dc2}=140 V (unequal DC sources)	32.99	33.24	33.71	30.32
V_{dc1}=140V V_{dc2}=80V (unequal DC sources)	35.92	35.84	36.48	33.26

V. CONCLUSION

A five level CHB-MLI has been simulated in Matlab/Simulink software using VFSPWM-A, VFSPWM-B, VFSPWM-C and VFSPWM-D Techniques**.** CHB-MLI with equal and unequal DC voltage source are compared and obtained CMV values are tabulated. From table 2 it can be clearly viewed that CMV is lesser in case of VFSPWM-D technique when compared with other techniques discussed. It can also be evident from table 2 that CMV is lesser in case of CHB-MLI with equal voltage sources when compared to CHB-MLI with unequal voltage sources.

REFERENCES

Journal Papers:

[1]. Mohd Esa and Mohd Abdul Muqeem Nawaz, "THD analysis of SPWM & THPWM Controlled Three phase Voltage Source Inverter", International Research Journal of Engineering and Technology (IRJET), vol. 04, no. 10, pp. 391-398, 2017.

[2]. Mohd Esa and J.E.Muralidhar, "Common Mode Voltage reduction in Diode Clamped MLI using Alternative Phase Opposition Disposition SPWM Technique", International Journal of Creative Research Thoughts (IJCRT), ISSN: 2320-2882, Volume.6, Issue 2, Page No pp.579-587, April-2018.

[3]. Mohd Esa and J.E.Muralidhar, "Investigation of Common Mode Voltage in 5-level Diode Clamped MLI using carrier based SPWM Techniques", International Journal of Creative Research Thoughts (IJCRT), ISSN: 2320-2882, Volume.6, Issue 1, Page No pp.395-399, February 2018.

[4]. Mohd Esa, Mohd Abdul Muqeem Nawaz and Syeda Naheed, "Harmonic Analysis of Three level Flying Capacitor Inverter", International Research Journal of Engineering and Technology (IRJET), vol. 04, no. 10, pp. 1687-1694, 2017.

[5]. G. Prem Sunder, B. Shanthi, A. Lamehi Nachiappan and S. P. Natrajan, "Performance Analysis of modified CHB MLI using various carrier modulation schemes", IJESA, vol. 3, no. 5, (2013), pp. 310-316.

[6]. B.P.Mcgrath and D.G Holmes "Multi carrier PWM strategies for multilevel inverter" IEEE Transaction on Industrial Electronics, Volume 49, Issue 4, Aug 2002, pp. 858-867

Proceedings Papers:

[7]. A. V. Jadhav, P. V. Kapoor and M. M. Renge, "Reduction of common mode voltage in motor drive application using multilevel inverter," 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS), Chennai, 2017, pp.721-724.

[8]. A. V. Jadhav and P. V. Kapoor, "Reduction of common mode voltage using multilevel inverter," 2016 International Conference on Energy Efficient Technologies for

Sustainability (ICEETS),Nagercoil, 2016, pp. 586-590.doi: 10.1109/ICEETS.2016.7583822

[9]. M. Esa and J. E. Muralidhar, "Common Mode Voltage reduction in Diode Clamped MLI using Phase Disposition SPWM Technique," 2018 4th International Conference on Electrical Energy Systems (ICEES), Chennai, India, 2018, pp. 279-289. doi: 10.1109/ICEES.2018.8442411

Mohd Esa "CMV analysis of 5-level Cascaded H-Bridge MLI with equal and unequal DC sources using Variable frequency SPWM Techniques "International Journal of Engineering Research and Applications (IJERA) , vol. 8, no.9, 2018, pp 36-41